Application Report
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TUSB1046A-DCI Configuration Guidelines

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ABSTRACT

The TUSB1046A-DCI is a linear redriver that supports both USB3.1 Gen 2 up to 10 Gbps and DisplayPort 1.4 up to 8.1 Gbps over a USB Type-C interface. At these higher data rates, signal integrity issues place limitations on system trace length. The TUSB1046A-DCI supplies several levels of receive linear equalization to compensate for cable and board loss due to inter-symbol interference (ISI). This document provides general guidelines on how to use the TUSB1046A-DCI in a Host (Source) application. The information in this document can also be applied to the TUSB546A-DCI.

Trademarks

1 Introduction

The TUSB1046A is a Type-C linear redriver mux intended for Type-C source applications. The TUSB1046A multiplexes between DP1.4 lanes and USB3.1 to a single Type-C receptacle. Both DisplayPort and USB standards define a minimum eye height and width at the end of a channel in which a compliant receiver must operate. Longer trace lengths and cables add ISI contributing to the loss of the channel which closes the eye such that the eye height and width are no longer compliant and the receiver cannot reliably recover the data on that channel. The TUSB1046A provides equalization gain to compensate for the board trace and cable loss due to ISI.

2 Equalization Selection

The TUSB1046A used in a host application enables the system to pass both transmitter electrical compliance and receiver jitter tolerance compliance testing for USB3.1 Gen1/2 and DisplayPort 1.4. The TUSB1046A recovers incoming data by applying equalization that compensates for the channel loss. The equalization should be set based on the amount of insertion loss of the channel before the TUSB1046A receivers. The EQ value of each channel should be set independently based on the loss of the channel, the equalization selection is performed by configuring the EQ[1:0], SSEQ[1:0] and DPEQ[1:0] pins, or through programming the equivalent registers if the device is configured for I2C operation. The equalization values (For USB3.1 Gen2 and DisplayPort HBR3 data rates) are detailed in Table 1. Typical FR-4 trace losses are given in Table 2.

Table 1. TUSB1046A Equalization Values

Equalization Setting #	USB3.1 DOWNSTREAM FACING PORTS			USB 3.1 UPSTREAM FACING PORT			ALL DISPLAYPORT LANES		
	EQ1 PIN Level	EQ0 PIN Level	EQ GAIN at 5 GHz (dB)	SSEQ1 PIN Level	SSEQ0 PIN Level	EQ GAIN at 5 GHz (dB)	DPEQ1 PIN Level	DPEQ0 PIN Level	EQ GAIN at 4.05 GHz (dB)
0	0	0	-3.9	0	0	-1.8	0	0	1.0
1	0	R	-1.7	0	R	0.2	0	R	3.3
2	0	F	-0.1	0	F	1.7	0	F	4.9
3	0	1	1.4	0	1	3.2	0	1	6.5
4	R	0	2.4	R	0	4.2	R	0	7.5
5	R	R	3.5	R	R	5.3	R	R	8.6
6	R	F	4.4	R	F	6.1	R	F	9.5
7	R	1	5.2	R	1	7.0	R	1	10.4
8	F	0	5.9	F	0	7.7	F	0	11.1
9	F	R	6.6	F	R	8.3	F	R	11.7
10	F	F	7.1	F	F	8.8	F	F	12.3
11	F	1	7.6	F	1	9.3	F	1	12.8
12	1	0	8.0	1	0	9.7	1	0	13.2
13	1	R	8.5	1	R	10.1	1	R	13.6
14	1	F	8.8	1	F	10.4	1	F	14.0
15	1	1	9.2	1	1	10.8	1	1	14.4

Table 2. 100 Ω Differential FR-4 PCB Trace Loss

4-mil Wide FR-4 PCB Trace Length	Loss at 2.5 GHz (0.4902 dB/inch) (dB)	Loss 4.05 GHz (0.7342 dB/inch) (dB)	Loss at 5 GHz (0.8691 dB/inch) (dB)
1	0.5	0.7	0.9
2	1	1.5	1.7
3	1.5	2.2	2.6
4	2	2.9	3.5
5	2.5	3.7	4.3
6	2.9	4.4	5.2
7	3.4	5.1	6.1
8	3.9	5.9	7
9	4.4	6.6	7.8
10	4.9	7.3	8.7

3 EQ Configuration Example

Figure 1 is an example configuration of host system using a USB3.1 Gen 2 Host operating at 10 Gbps, and a DisplayPort GPU source operating at 8.1 Gpbs.

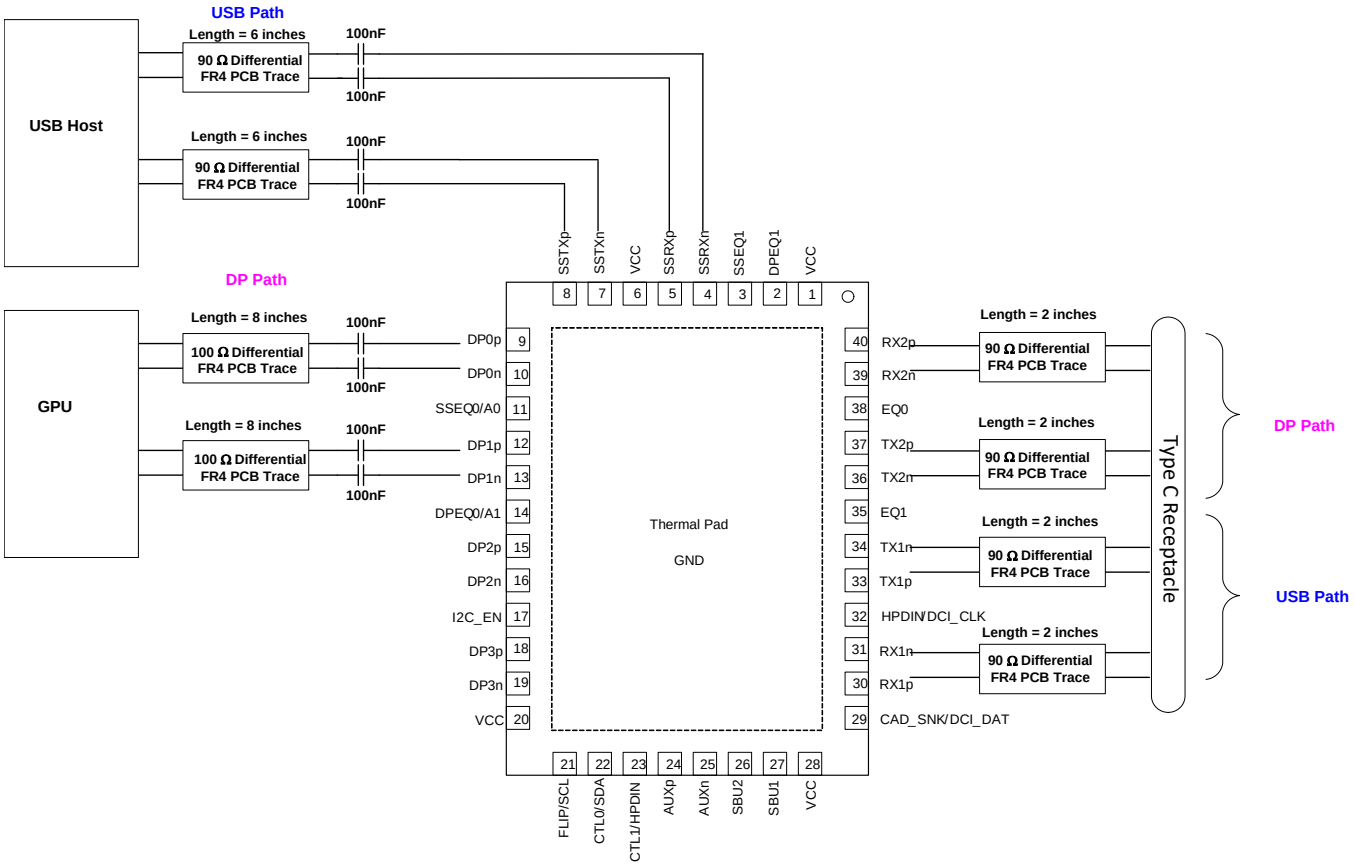

Figure 1. Host System Trace Length Example

Use the trace lengths and data rates in this example when selecting the EQ values for SSTX, DPEQ and RX1/2. Select the closest EQ gain available to match the trace loss. Example configurations:

- USB Host to TUSB1046A (SSTX) = 6 inches (5.2 dB Loss at 5 GHz)
  - SSEQ setting used = Setting #6 (6.1 dB)
- GPU to TUSB1046A (DP[1:0]) = 8 inches (5.9 dB Loss at 4.05 GHz)
  - DPEQ setting used = Setting #3 (6.5 dB)
- Type-C Receptacle to TUSB1046A (RX1/2) = 2 inches (1.7 dB at 5 GHz)
  - EQ setting used = Setting #4 (2.4 dB).

Other factors such as the layout quality, Host Controller driver and receiver quality may require the EQ settings to be adjusted higher or lower for best performance. This method should be used for selecting initial configuration settings based on system board trace lengths.

For USB3.1 Gen 2 Electrical Compliance testing, the USB-IF defines a total loss budget of 23 dB with 8.5 dB budgeted for the Host system. In some cases, the Host system can have more than the budgeted amount of loss of which the TUSB1046A compensates for the ISI. Some Host controllers cannot adequately recover the signal with the given the amount of Sj and Rj used to stress the receiver (Calibrated based on the 23 dB total loss budget). To help ensure passing of electrical compliance testing for USB, the best practice is to follow the recommended maximum trace lengths for Pre-Channel (PCH to TUSB1046A) and Post-Channel (TUSB1046A to Type-C Connector) See TUSB1046A Placement Figure 2:

Pre-Channel Maximum Trace Length = 6 inches.

Post-Channel Maximum Trace Length = 4 inches.

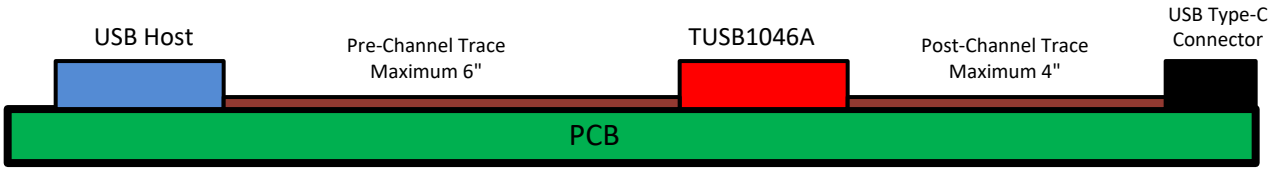

Figure 2. TUSB1046A Placement Example

4 Device Configuration

The TUSB1046A supports several configuration modes for Type-C applications, Table 3 details the different modes via configuration by pin-strapping, configuration over I2C is also available (See datasheet for I2C configuration details and register mapping). A typical host Type-C application uses USB3.1 + DP Alt Mode over Type-C, Figure 1 shows an example configuration. For example DisplayPort only implementation, see TUSB546-DCI in a DisplayPort Application, SLLA365.

Table 3. TUSB1046A Configuration

CTL1 PIN	CTL0 PIN	FLIP PIN	TUSB1046A-DCI CONFIGURATION	VESA DisplayPort ALT MODE
L	L	L	Power Down	—
L	L	H	Power Down	—
L	H	L	One Port USB 3.1 - No Flip	—
L	H	H	One Port USB 3.1 – With Flip	—
H	L	L	4 Lane DP - No Flip	C and E
H	L	H	4 Lane DP – With Flip	C and E
H	H	L	One Port USB 3.1 + 2 Lane DP- No Flip	D and F
H	H	H	One Port USB 3.1 + 2 Lane DP– With Flip	D and F

5 Layout Guidelines

The following layout guidelines should be used in routing the high-speed USB and DisplayPort signals to and from the TUSB1046A.

1. RXP/N and TXP/N pairs should be routed with controlled 90-Ω differential impedance (±15%).
2. Keep away from other high speed signals
3. Intra-pair routing should be kept to within 2 mils
4. Length matching should be near the location of mismatch
5. Each pair should be separated at least by 3 times the signal trace width
6. The use of bends in differential traces should be kept to a minimum. When bends are used, the number of left and right bends should be as equal as possible and the angle of the bend should be ≥ 135 degrees. This will minimize any length mismatch causes by the bends and minimize the impact bends have on EMI.
7. Route all differential pairs on the same of layer
8. The number of vias should be kept to a minimum. It is recommended to keep the vias count to 2 or less.
9. Keep traces on layers adjacent to ground plane.
10. Do not route differential pairs over any plane split.
11. If using a through-hole connector, route high-speed signals on opposite side of the connector such that the connector pin does not create a stub in the transmission line.

The entirety of any high-speed signal trace should maintain the same GND reference from origination to termination. If the same GND reference is not maintained, via-stitch both GND planes together to ensure continuous grounding and uniform impedance. Place these stitching vias symmetrically within 200 mils (center-to-center, closer is better) of the signal transition vias. See Figure 3 for an example of GND stitching vias:

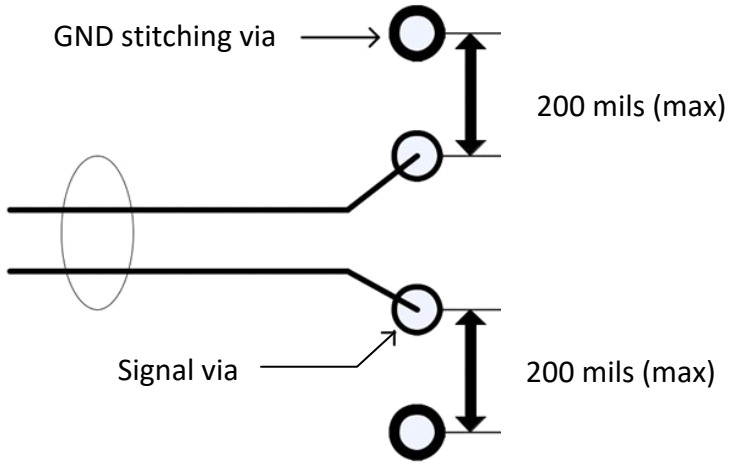

Figure 3. GND Stitching Vias Example

When placing AC-Coupling capacitors, the maximum component size used should be 0402. The AC Coupling capacitors should be placed symmetrically during layout to ensure optimum signal quality and to minimize reflections. See Figure 4 and Figure 5 for correct AC Coupling capacitor placement and symmetry examples.

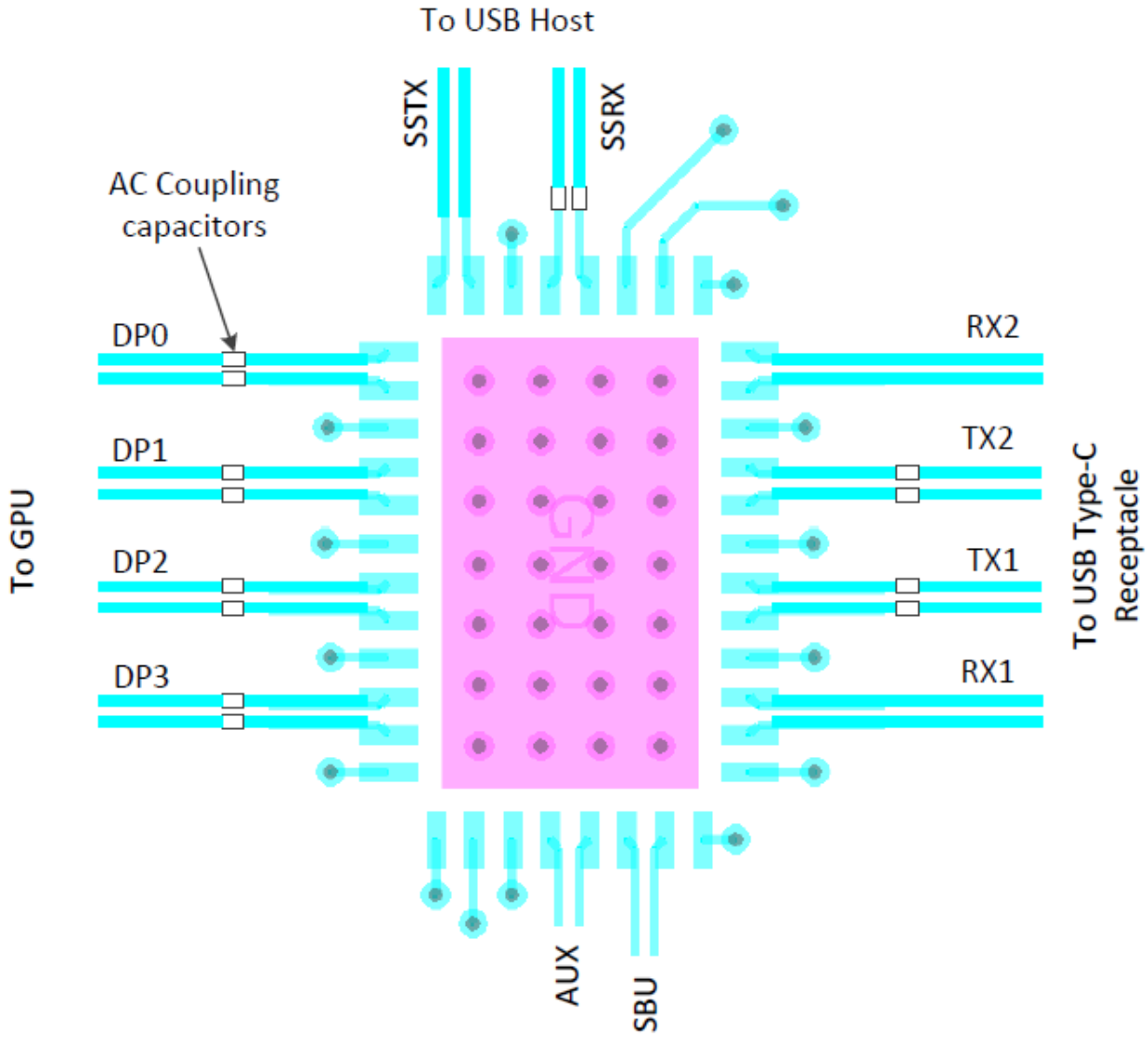

Figure 4. AC Coupling Capacitor Placement

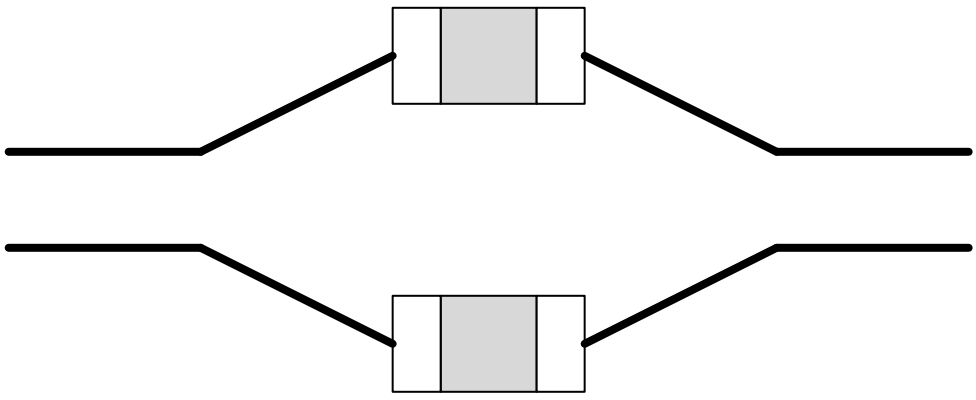

Figure 5. AC Coupling Capacitor Symmetry Example

NOTE: Adding Test points will cause impedance discontinuity which negatively impact signal performance. If test points are used, they should be placed in series and symmetrically. They must not be placed in a manner that causes a stub on the differential pair.

6 References

- Data sheet: TUSB1046~~I~~-A~~A~~-DCI Type-C DP Alt Mode Linear Redriver Crosspoint Switch, SLLSF13
- Data sheet: TUSB546A-DCI USB Type-C DP Alt Mode Linear Redriver Crosspoint Switch, SLLSF14
- HDMI 1.4b Alt Mode on USB Type-C Specification, Version 1.0a, January 17, 2017
- VESA DisplayPort Alt Mode on USB Type-C Standard, Version 1.0a, August 5, 2015

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