Product Overview

Reducing the Need for Cold Sparing in Remote Satellite Systems Designs

In remote space satellite systems, harsh environmental factors such as solar flares and coronal mass ejections (CMEs) can permanently damage satellite reliability through single-event effects (SEEs). If protection against SEEs is not considered during the initial design of the satellite's internal circuits, a single severe SEE can destroy a critical component within the satellite. This can lead to communication issues and long-term reliability problems for the satellite. Often, the delays and errors caused by destructive SEEs can render a satellite inoperable, significantly hindering advancements in space missions. To reduce the impact of a destructive single-event effect (SEE) on long-term satellite operations, system designers commonly incorporate cold spares (backup circuit components) into their designs. This approach allows satellite operators to switch to these backup components if the primary devices fail due to an SEE.

Texas Instruments (TI) has developed its first space-grade multiplexer, the TMUX582F-SEP, to reduce the number of cold spare components required in satellite designs. This part enables system designers to integrate a multiplexer into their signal processing designs while also providing a form of SEE protection through Single Event Latch-up (SEL) immunity.

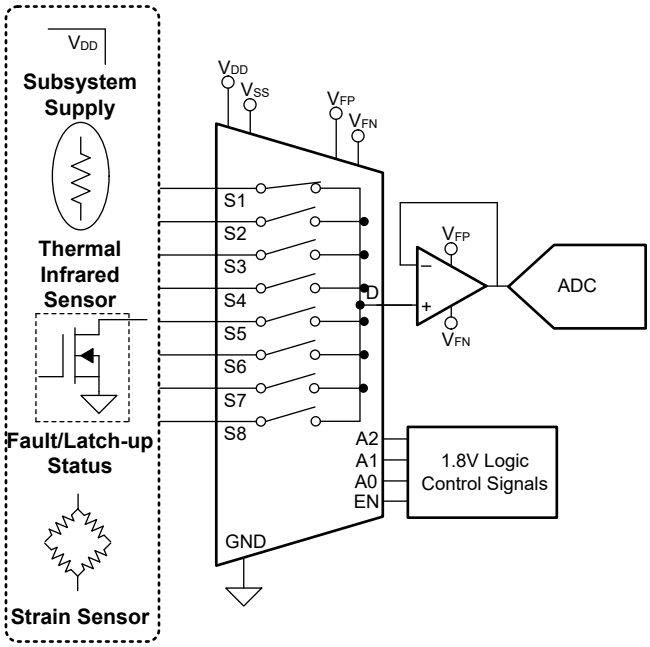

Figure 1. Typical Application- Satellite Telemetry

In Remote satellite systems, an SEL is an unintended creation of a low-impedance path between the power supply rails of a MOSFET circuit, caused by excess current injection from passing energetic ions in space. This results in a parasitic SCR that typically disrupts the proper functioning of a part or even leads to its destruction due to overcurrent.

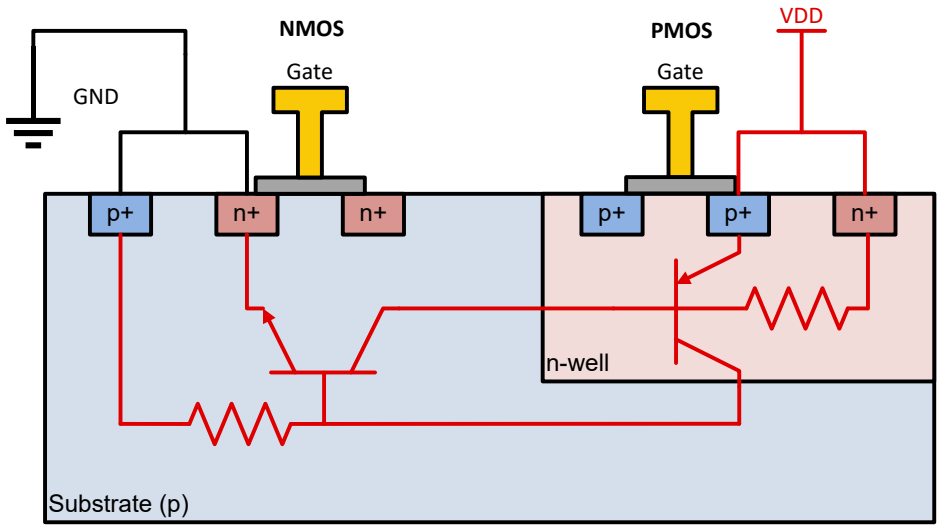

Figure 2. Parasitic SCR Structure Created by SEL

The TMUX582F-SEP is protected from SEL because it is constructed on a Silicon on Insulator (SOI- based process where an oxide layer is added between the PMOS and NMOS transistor of each CMOS switch to prevent parasitic structures from forming. The SEL immunity feature allows the TMUX582F-SEP to be used in remote space satellite systems and reduces cold-sparing requirements for system designers.

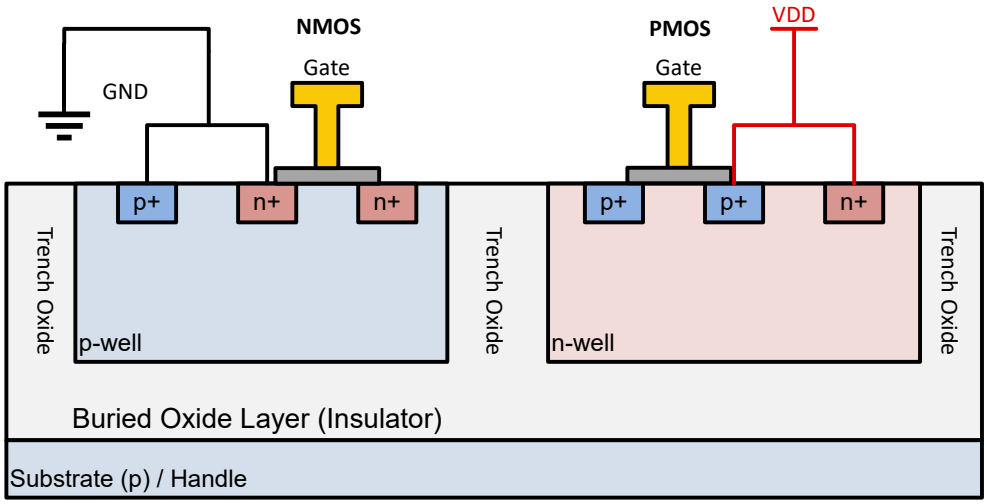

Figure 3. TMUX582F-SEP SEL Prevention: Buried Insulating Oxide Trench

References

- Texas Instruments: *TMUX582F-SEP Single-Event Effects (SEE) Radiation Report*
- Texas Instruments: *Using Latch-Up Immune Multiplexers to Help Improve System Reliability Application Report*
- Texas Instruments: *What is Latch-Up Immunity Precision Labs Video*

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