

## TUSB1310A Errata

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<b>Problem:</b>	<b><i>RX CMD Byte does not return the correct VBUS State. This only affects legacy USB2 link controllers that do not use Power Present.</i></b>
<b>Work Around:</b>	Must use the Power Present input to detect the presence of VBUS (use an SS link controller). If a legacy controller is used, the user must implement the logic required to use Power Present.
<b>Severity:</b>	Low
<b>Problem:</b>	<b><i>RX_ELECIDLE low (it should be high) when not receiving a valid LFPS.</i></b>
<b>Work Around:</b>	None.
<b>Severity:</b>	Low
<b>Problem:</b>	<b><i>Corrupted SKIPS returned to USB3 Loopback Master.</i></b>
<b>Work Around:</b>	Implement external loopback in FPGA.
<b>Severity:</b>	Low
<b>Problem:</b>	<b><i>No output on pipe interface under some conditions.</i></b>
<b>Work Around:</b>	Use external pull up on OUTPUT ENABLE, internal pull up resistor may not work over PVT (process, voltage, temperature).
<b>Severity:</b>	Low
<b>Problem:</b>	<b><i>RX.DETECT fails in P3.</i></b>
<b>Work Around:</b>	Use P2.
<b>Severity:</b>	Low
<b>Problem:</b>	<b><i>RJ out of spec when SSC is enabled.</i></b>
<b>Work Around:</b>	Use 40-MHz input clock with SSC enabled. This is not an issue if SSC is disabled, any valid input clock frequency can be used.
<b>Severity:</b>	Medium
<b>Problem:</b>	<b><i>BER greater than E-12 when low freq SJ is enabled.</i></b>
<b>Work Around:</b>	Use 40-MHz input clock. Not an issue if SSC is disabled.
<b>Severity:</b>	Medium

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