UNITRODE

Design Note

Versatile Low Power SEPIC Converter
Accepts Wide Input Voltage Range

by Jack Palczynski

Much attention has been given to the Single Ended Primary Inductor Converter (SEPIC) topology recently because output voltage may be either higher or lower than input voltage. The output is also not inverted as is the case in a flyback or Cuk topology. Voltage conversion is accomplished without transformers, instead using low cost inductors to transfer energy. The input and output voltages are DC isolated by a coupling capacitor. This design note illustrates an application for a 5V, 100mA output converter for battery powered and Automotive applications. It makes use of a UCC3803 BiCMOS current mode controller to provide a 5V output at full load of 100mA from an input of 2.5V to 13.5V after an initial start-up at 5 volts.

This SEPIC converter uses current mode control to simplify stabilization of the control loop. Peak cur-

rent in the FET is limited by the pulse by pulse current limiting of the UCC3803. Switching frequency is 500kHz, allowing low output current handling and low output ripple with small inductors and capacitors while remaining in the continuous inductor current mode (CCM). Once started, the low voltage operation of the UCC3803 is extended by bootstrapping from the output through a UC3612 Schottky diode. By including slope compensation (Q2, R3), the duty cycle may exceed 50% without experiencing subharmonic oscillations.

This topology places higher stresses on both the switch and the diode than with other PWM topologies. Peak switch and diode stresses are both $V_{IN}+V_{OUT}$ and $I_{IN} + I_{OUT}$. Peak to peak ripple current in the coupling capacitor is $I_{IN} + I_{OUT}$.
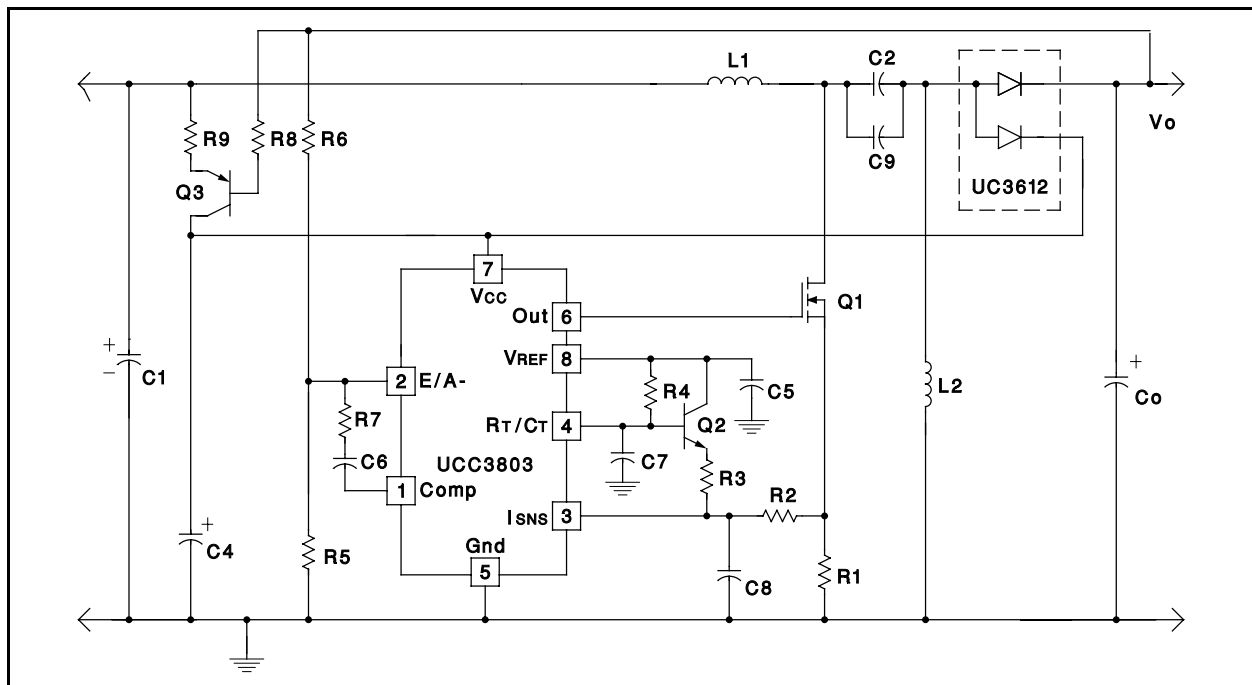

Figure 1. UCC3803 Controlled SEPIC Converter

Specifications :

V_{IN} (initial start-up) 5V
V_{IN} . . . . 2.5V to 13.5V
I_{OUT} . . . . 45mA to 100mA
Switching Frequency 500kHz
Output Regulation . . . . ±3%
Output Ripple . . . . 150mV (max)

SEPIC Converter Design Guide:

1. Choose a switching frequency, fs.

   $fs = 500kHz$

2. Calculate minimum duty cycle (D_{MIN}):

   $$D_{MIN} = \frac{V_O}{V_O + V_{IN}(max)}$$

   $$D_{MIN} = \frac{5V}{(5V + 13.5V)} = 0.27$$

3. Calculate maximum duty cycle (D_{MAX}):

   $$D_{MAX} = \frac{V_O}{V_O + V_{IN}(min)}$$

   $$D_{MAX} = \frac{5V}{(5V + 2.5V)} = 0.67$$

4. Find an appropriate inductor so that I_{DIODE} is not less than zero (note that this value should be used for both inductors):

   $$L > \frac{V_{IN}(max) \bullet D_{MIN}}{fs \bullet I_O(min)\left(\frac{V_O}{V_{IN}(max)} + 1\right)}$$

   $$L_1 = L_2 > \frac{13.5V \bullet 0.27}{500kHz \bullet 45mA\left(\frac{5}{13.5} + 1\right)} = 118\mu H$$

Note that the COILCRAFT inductor selected is specified at twice this value of inductance at light load, and decreases at high loads.

5. Calculate $I_{IN}(max)$ at maximum output current:

   $$I_{IN}(max) = \frac{I_O(max) \bullet D_{(max)}}{1 - D_{(max)}}$$

   $$I_{IN}(max) = \frac{0.1 \bullet 0.67}{1 - 0.67} = 202mA$$

6. Find RMS current ripple and choose an appropriate C_{cc}:

   $$\sqrt{I_O(max)^2 \bullet D_{(max)} + I_{IN}(max)^2 \bullet (1 - D_{(max)})}$$

   $$\sqrt{0.1^2 \bullet 0.67 + 0.2^2 \bullet (1 - 0.67)} = 141mA$$

Select a capacitor to handle this ripple current.

7. Choose an output capacitor for ripple voltage:

   $$dI_O(max) = I_{IN}(max) + \frac{V_{IN}(max) \bullet D_{(max)}}{2Lfs}$$

   $$dI_O(max) = 202mA + \frac{2.5V \bullet 0.67}{2 \bullet 220\mu H \bullet 500kHz} = 209mA$$

then, ripple voltage

   $$dV > dI_O(max)\left(\frac{1}{2\pi fs \bullet C} + ESR\right)$$

   $$150mV > 209mA\left(\frac{1}{2\pi \bullet 500kHz \bullet 33\mu F} + 0.7\right) = 148mV$$

Some iterations with different capacitors will yield an acceptable voltage ripple.

It may become necessary to run the converter in discontinuous inductor current mode (DCM) when minimum load is a very small percentage of the maximum load. D will become dependent on output load and output voltage regulation will vary more than in CCM. The CCM system double pole occurs at

   $$fdp = \frac{1}{\sqrt{2} \bullet \pi (L1 + L2)C_{cc}}$$

and the ESR zero occurs at

   $$fz = \frac{1}{2 \bullet \pi \bullet ESR \bullet C_O}.$$

A plot of efficiency is shown below for the range of input voltage. Efficiency may be increased by using lower switching frequencies at a cost of larger components. This might be desirable in equipment with small batteries that demand lower power consumption for extended life.

The SEPIC converter may be used for a wide range of output voltages over a range of input voltages.

Other outputs tested were 3V and 12V with circuits similar to that of this design note. As output current increases, conduction losses in the switch and output diode begin to degrade efficiency and ripple current in the coupling capacitor may be excessive. In high power applications, a transformer isolated con-

Efficiency vs Input Voltage

verter or cascaded stages may be more practical.

Parts List:

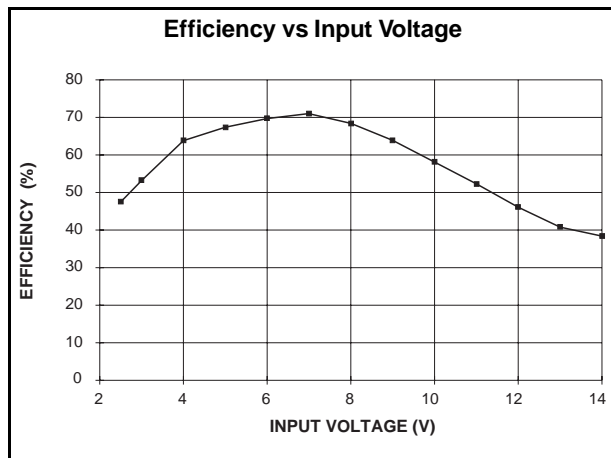|	
D1, D2	Unitrode UC3612D Dual Schottky phone # (603) 429-8610
C1-3, C9	33µF 25V Sprague 293D336X0025E2T phone # (207) 324-4140
C4,C5,C6	0.1µF Ceramic
C8	150pF Ceramic
L1, L2	220µH COILCRAFT DT3316-102-224 phone # (708) 639-1469
Q1	Siliconix Si9410DY phone # (800) 554-5565
Q2	2N2222S
Q3	2N2907AS
R1	1 ohm 1/4W
R2	1k 1/8W
R3, R6	10k 1/8W
R4	30k 1/8W
R5, R7	6.2k 1/8W
R8,R9	50 ohm 1/8W
U1	Unitrode UCC3803D BiCMOS PWM IC

REFERENCES:

[1] W. Andreycak U-133 "UCC3800/1/2/3/4/5 BiCMOS Current Mode Control ICs" Unitrode Application Note

[2] L. Dixon "High Power Factor Preregulator Using the SEPIC Converter" Unitrode Seminar SEM-900 pp. 6.1-6.12

[3] L. Dixon "Control Loop Design SEPIC Preregulator Example" Unitrode Seminar SEM-900 pp. 7.1-7-6

[4] U-97 "Modeling, Analysis and Compensation of the Current-Mode Converter" Unitrode Applications Handbook A-100 pp. 260-266

[5] U-100 "UC3842 Provides Low-Cost Current-Mode Control" Unitrode Applications Handbook A-100 pp.278-291

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