48-V_{IN}, 12-V_{OUT} Loadshare System Using The UCC39002 With Three dc-to-dc Modules

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ABSTRACT

This application note features the UCC39002 BiCMOS 8-pin advanced load share controller and specifically illustrates equal current sharing between three 48-V_{DC} to 12-V_{DC} power modules, each rated for 8.4-A maximum output current, paralleled to supply a load of up to 24 A. The example uses high-side current sensing with the bias for the controllers supplied directly from the module's output voltage. The complete list of materials, schematic, and Gerber file images are included. The intent of this application is to step through the calculations required to use this device, keeping in mind the actual values of the components are dependent upon the specific modules to be paralleled.

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1 Introduction

Many systems benefit from paralleling low-current low-voltage power modules for high-current low-voltage applications. Paralleling modules adds redundancy for enhanced reliability, hot-swap capability, and aids in distributed heat removal when compared to a single high-current low-voltage supply. Load sharing provides the equal distribution of load currents among paralleled voltage-stabilized power supplies. Without a controller, the supply with the highest output voltage contributes the majority of the output current.

Since the output impedance of these modules is extremely low (on the order of mΩ), a small difference in output voltage among the supplies would result in a relatively large difference among output currents. The module supplying the majority of the load current could potentially enter current-limit mode, increasing its thermal stress, which leads to decreased reliability. A load share controller adds a voltage feedback loop. Within this loop, the output current of each module is measured and compared to a common load share bus. Load sharing is realized when the output voltage of each module is suitably adjusted via this voltage feedback loop so that each module delivers an equal amount of output current. To do this, each module must have true remote sense capability or an output voltage adjustment terminal. One load share controller and minimal compensation components are required for each module. A typical high side application is shown in Figure 1 and is repeated for each module being paralleled. This circuit is repeated for each module to be paralleled.

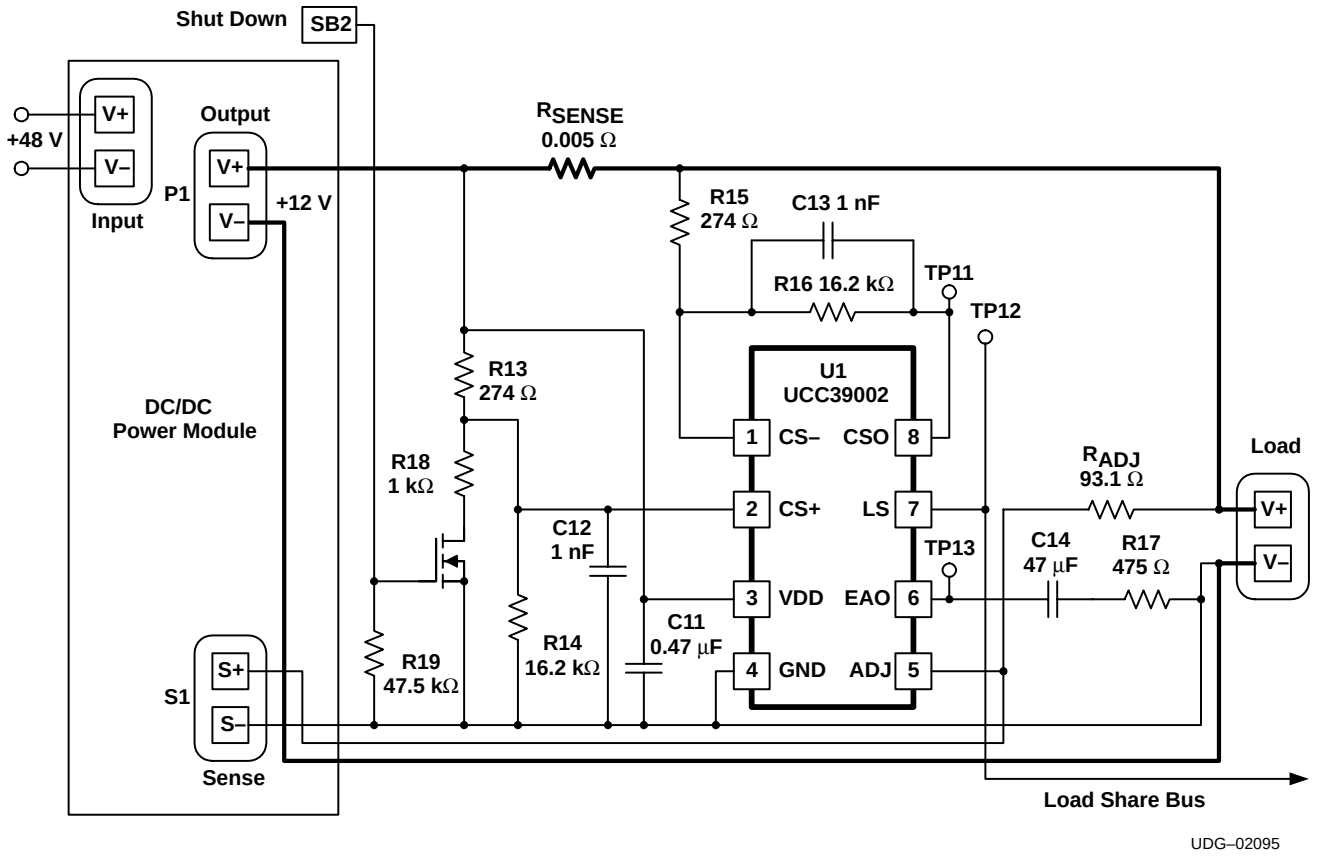

Figure 1. Typical High-Side Application for Single Power Module

2 Setting Up the UCC39002 Load Share Controller

2.1 Measure the Modules

In order to accurately current share between power modules, specific parameters must be known. Among these parameters are the nominal output voltage of the modules (V_{OUT}), the maximum output current of each module ($I_{OUT(max)}$), the maximum voltage adjustment range of each module (V_{ADJ}), and the transfer function of the power modules between their positive voltage sense and power output terminals.

For this particular example, as stated in the power module's data sheet (TI Literature Number SLUS495):

- V_{OUT} = 12 V
- $I_{OUT(max)}$ = 8.4 A
- $\Delta V_{ADJ(max)}$ = 600 mV

The UCC39002 requires a bias voltage of 4.375 V to turn on, but the bias should not exceed 18 V. Due to the 12-V output of the modules, direct bias from the output voltage of the modules is possible.

VDD = 12 V

Universal power modules have a very low bandwidth to ensure proper operation with a variety of loads. The transfer function is determined using a network analyzer and injecting a small signal across a 50-Ω resistor placed between the positive sense terminal and the positive voltage output terminal, much like measuring the control loop of a converter, as shown in Figure 2. The resultant Bode plot shows the dc gain and the unity gain crossover frequency of the module. Expect the module's crossover frequency to be within the range from 0.1 Hz to approximately 30 kHz. The desired crossover frequency for the load share loop is set at one decade before the unity gain crossover frequency of the modules. This is accomplished by selecting the compensation components for the transconductance error amplifier as described in Section 2.5, *Error Amplifier Compensation*.

The unity gain crossover frequency (f_{CO}) is measured from the power module's SENSE(+) terminal to the VOUT(+) terminal.

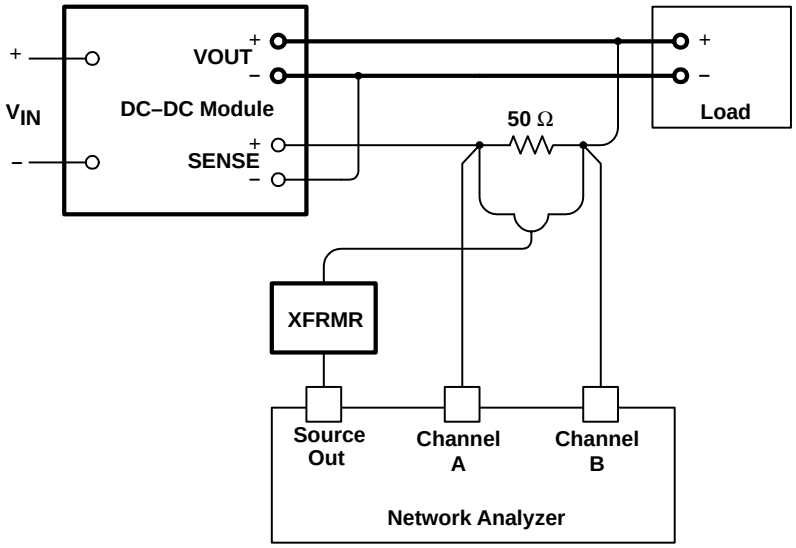

Figure 2. Measuring the Unity Gain Crossover

The resultant Bode plot of the loop gain yields a crossover frequency (f_{CO}) of 40 Hz. The unity gain crossover frequency is unique to the module and must be specifically measured for each module type.

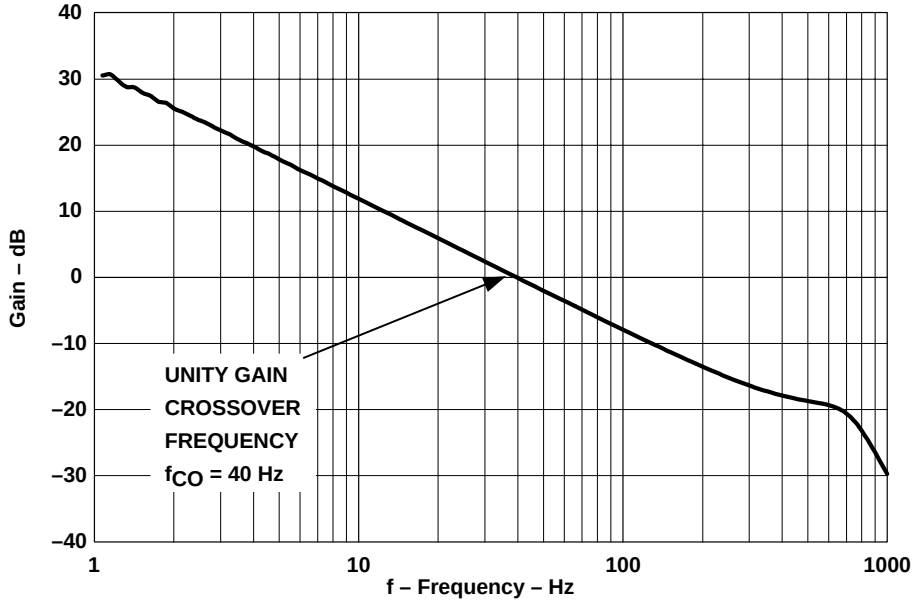

Figure 3. Power Module Bode Plot

2.2 Choosing the Sense Resistor

The primary concern in the selection of the sense resistor is to ensure that the sum of the voltage drops across the resistor and the parasitic wire impedances, at maximum module output current, is significantly less than the output voltage adjustment range of the modules, otherwise there would be no room for output voltage adjustment.

$$I_{OUTmax} \times R_{SENSE} << \Delta V_{ADJ(max)}$$

Other limitations for the sense resistor are the desired minimum power dissipation and available component ratings.

For this particular example, the power dissipation of each current sense resistor was desired to be less than 500mW:

- $R_{SENSE(max)} = P_{RSENSE} / I_{OUT(max)}^2 = 500\ mW / 8.4A^2 = 7\ m\Omega$
- $R_{SENSE} = 5\ m\Omega$ is selected
- $P_{RSENSE} = 353\ mW$
- $I_{OUT(max)} \times R_{SENSE} = 42\ mV << \Delta V_{ADJ(max)}$

2.3 Setting the CS Amplifier Gain

The gain of the current sense amplifier (CSA) is configured by adding compensation components between the inverting input to the amplifier, CS–, and the current sense amplifier output, CSO, of the load share device. The maximum voltage at the CSO pin is limited by the saturation voltage of the internal current sense amplifier and must be at least 2-V less than VDD. For this particular example, $V_{CSO(max)}$ must be less than 10 V.

- $V_{CSO(max)} < VDD - 2\ V$
- $V_{CSO(max)} < 12\ V - 2\ V$
- $V_{CSO\ (max)} < 10\ V$

The CSA gain, A_{CSA}, is equal to:

$$A_{CSA(max)} = \frac{V_{CSO(max)}}{\left(R_{SENSE} \times I_{OUT(max)}\right)}$$

Referring to Figure 1, the A_{CSA} gain is set by the R16:R15 resistor ratio.

Although the maximum gain is calculated to be 238, the A_{CSA} gain is set to 60, resulting in a voltage of 2.52 V at CSO. A high-frequency pole, configured with C13, was also added for noise filtering. This impedance is mirrored at the non-inverting input, CS+, of the differential amplifier.

The CSA output voltage, V_{CSO}, serves as the input to the internal unity gain LS bus driver. The module with the highest output voltage forward biases the internal diode located at the output of the LS bus driver and determine the voltage on the load share bus on the LS pin, V_{LS}, making this module the master. This load share bus acts as a communication port between the paralleled modules. The LS pin is bi-directional. By forward biasing the internal diode, the master sets the LS bus voltage based upon the voltage across its current sense resistor. Because the internal diode is reverse biased on the other modules, referred to as the slaves, the LS voltage is used as the non-inverting input to the internal LS bus receiver. The master transmits the voltage signal to the slave modules so they can compare their voltages across their own current sense resistors with that of the master module. The slave modules represent a load on the bias current, I_{VDD}, of the master module due to the internal 100-kΩ resistor at the LS pin. This increase in supply current for the master module is equal to:

$$\Delta I_{VDD} = n \times \left(\frac{V_{LS}}{100\ k\Omega}\right)$$

where *n* is equal to the number of paralleled modules.

2.4 Determining R_{ADJ}

The SENSE(+) terminal of the module is connected to the ADJ pin of the load share controller. By placing a resistor between the ADJ pin and the load, an artificial SENSE(+) voltage is created from the voltage drop across R_{ADJ} due to the current sunk by the internal NPN transistor. The voltage at the ADJ pin must be maintained at approximately 1 V or more above the voltage at the EAO pin. This is necessary in order to keep the transistor at the output of the internal adjust amplifier from saturating. To fulfill this requirement, R_{ADJ} can be calculated using the following equation:

$$R_{ADJ} \geq \frac{\left[\Delta V_{ADJ(max)} - \left(I_{OUT(max)} \times R_{SENSE}\right)\right] \times 500\ \Omega}{V_{OUT} - \left(\Delta V_{ADJ(max)} - \left[I_{OUT(max)} \times R_{SENSE}\right]\right) - 1\ V}$$

The maximum sink current of the ADJ pin also limits the R_{ADJ} resistor selection. $I_{ADJ(max)}$ is equal to 6 mA, as determined by the internal 500-Ω emitter resistor and 3-V clamp. The value of the adjust resistor, R_{ADJ}, is based upon the maximum adjustment range of the module, $\Delta V_{ADJ(max)}$. This adjust resistor must be greater than, or equal to, the given voltage adjustment range divided by the maximum available current:

$$R_{ADJ} \geq \frac{\Delta V_{ADJ(max)} - \left(I_{OUT(max)} \times R_{SENSE}\right)}{I_{ADJ(max)}}$$

By selecting a resistor that meets both of these minimum requirements, the ADJ pin is set at least 1-V greater than the EAO voltage and the adjust pin sink current does not exceed its 6-mA maximum.

2.5 Error Amplifier Compensation

The total loadshare loop unity gain crossover frequency, f_{CO}, should be set below the measured crossover frequency of the paralleled modules previously measured, $f_{CO(module)}$ shown in Figure 2b. Compensation of the transconductance error amplifier is done by placing the compensation resistor, R_{EAO} shown as R17 in Figure 1, and capacitor, C_{EAO} shown as C14 in Figure 1, between EAO and GND thereby adding a zero at least one decade before $f_{CO(module)}$. The values of these components is determined by the following loop gain equation.

$$C_{EAO} = \left(\frac{g_M}{\pi f_{ZERO}}\right) \times A_{CSA} \times A_V \times A_{ADJ} \times \left(A_{PWR}\left(f_{ZERO}\right)\right)$$

Where:

- g_M is the transconductance of the error amplifier, typically 14 ms,
- f_{ZERO} is equal to the desired zero frequency in Hz of the load share loop, typically at least $f_{CO\ (module)}/10$,
- A_{CSA} equals R16/R15,
- A_V is the voltage gain, equal to R_{SENSE}/R_{LOAD},
- A_{ADJ} is the gain associated with the adjust amplifier, equal to $R_{ADJ}/500\ \Omega$,
- $A_{PWR}(f_{ZERO})$ is the measured gain of the power module at the desired zero frequency, converted from dB, as displayed in Figure 3, to V/V
  - $A_{PWR}\ (f_{ZERO})$ in V/V = $10^{(\text{Gain, in dB, at } f_{ZERO} \text{ (from Figure 3)}/20)}$

Once the C_{EAO} capacitor is determined, R_{EAO} is selected to achieve the desired loop response

$$R_{EAO} = \frac{1}{2\pi\left(C_{EAO}\right)\left(f_{ZERO}\right)} \quad (1)$$

2.6 Other circuitry

Referring to Figure 1, R18, R19, and Q1 provide remote disconnect. By injecting a high signal onto SB2, Q1 is turned on, shorting CS+ to ground, disabling the load share controller for that module.

3 Test Results

Following the procedure described in this application note, three dc-to-dc modules are paralleled. The list of materials and complete schematic, along with the board layout are included. Figure 3 shows the Bode plots for the dc-to-dc module, the open loop load share circuitry, and the total combined loop gain. Figure 4 displays the individual output currents measured from each module as a function of the total load current and figure 5 shows the load share error is minimal at full load. At light load, internal offset voltages and small signal measurement error have a more pronounced effect, contributing to a larger current distribution error, as expected.

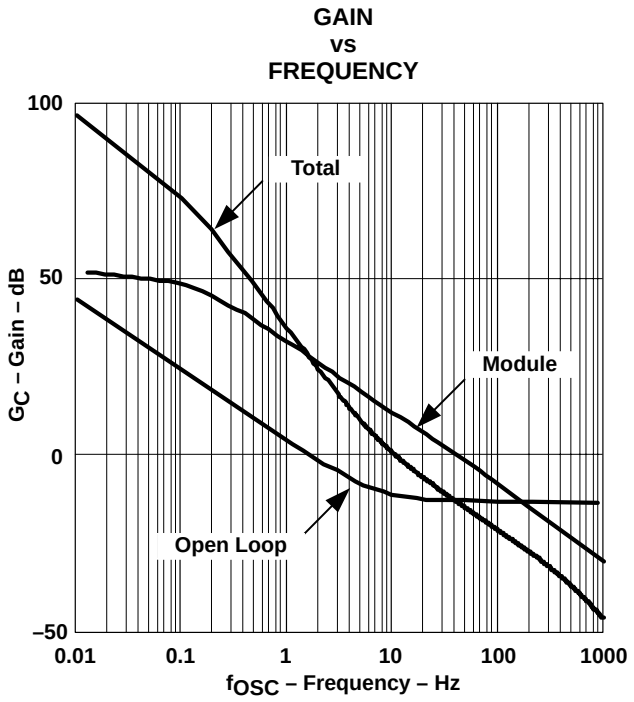

Figure 4.

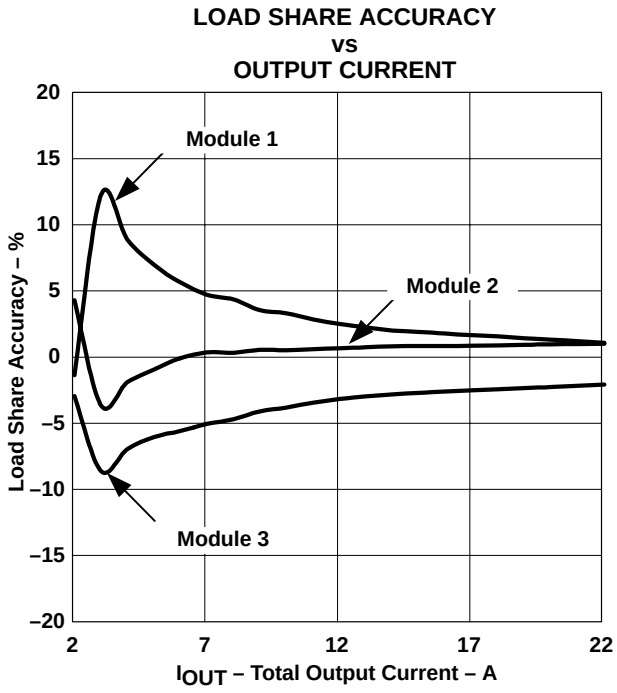

Figure 5.

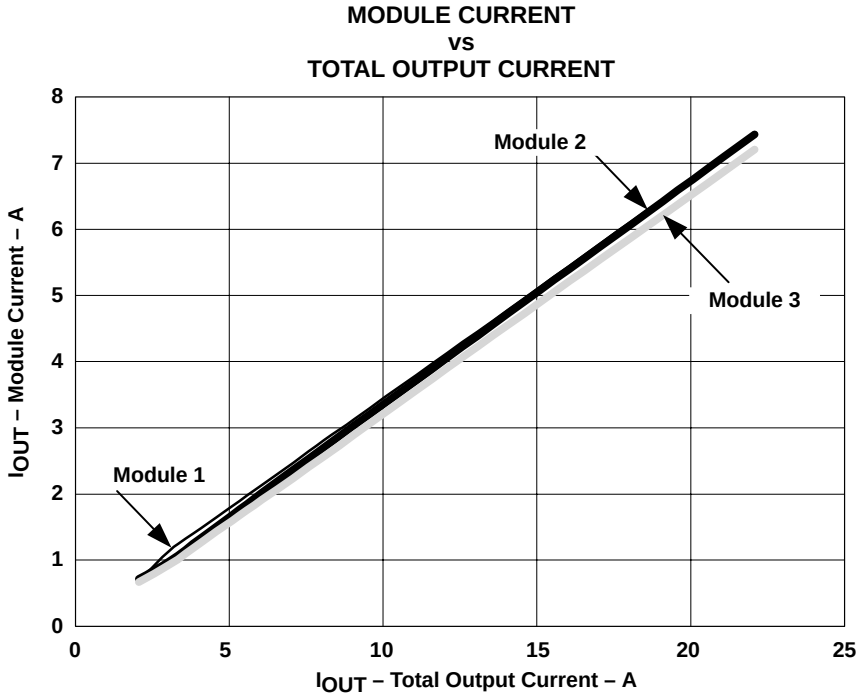

Figure 6.

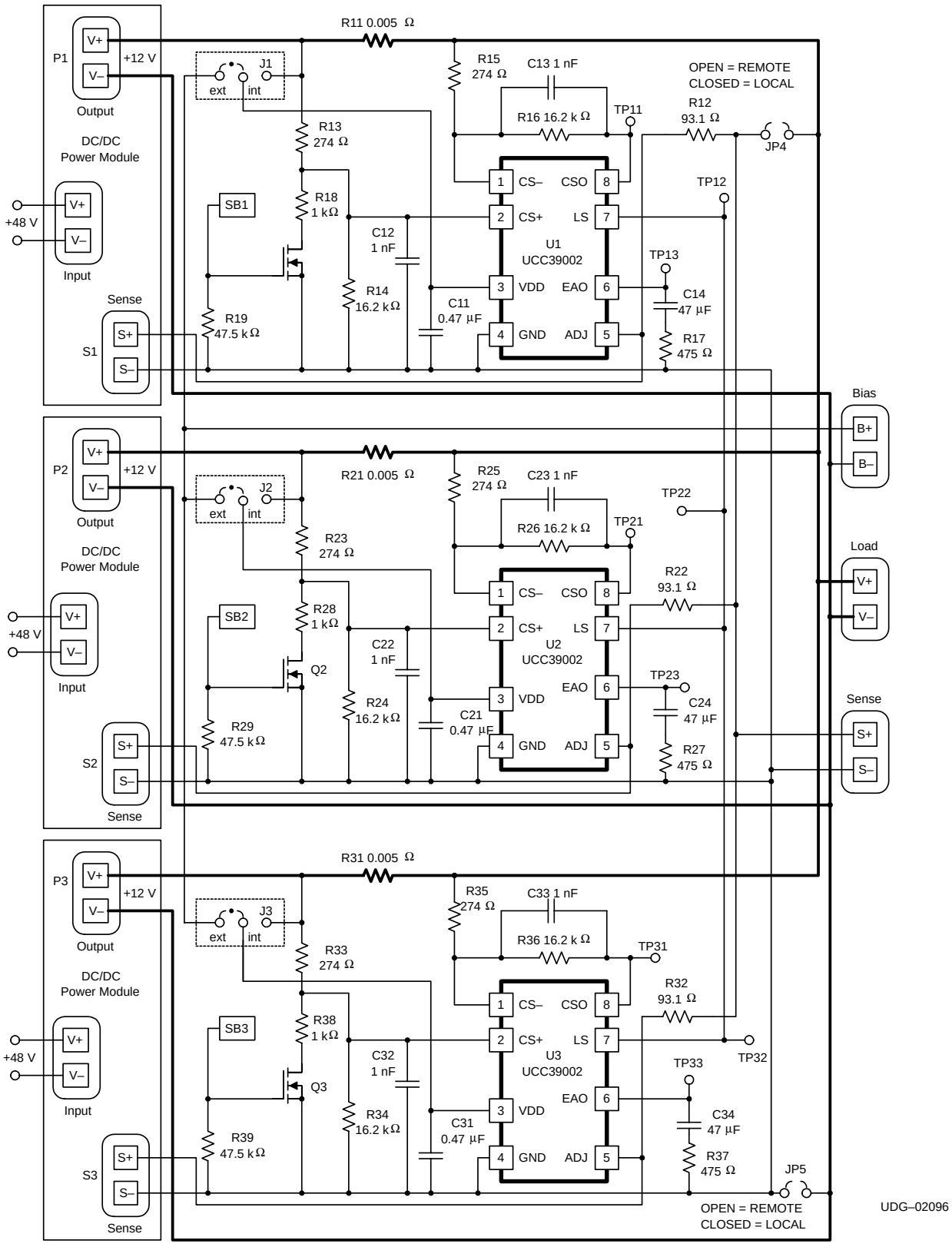

Figure 7. Three Module Load Share Application

4 Board Layout

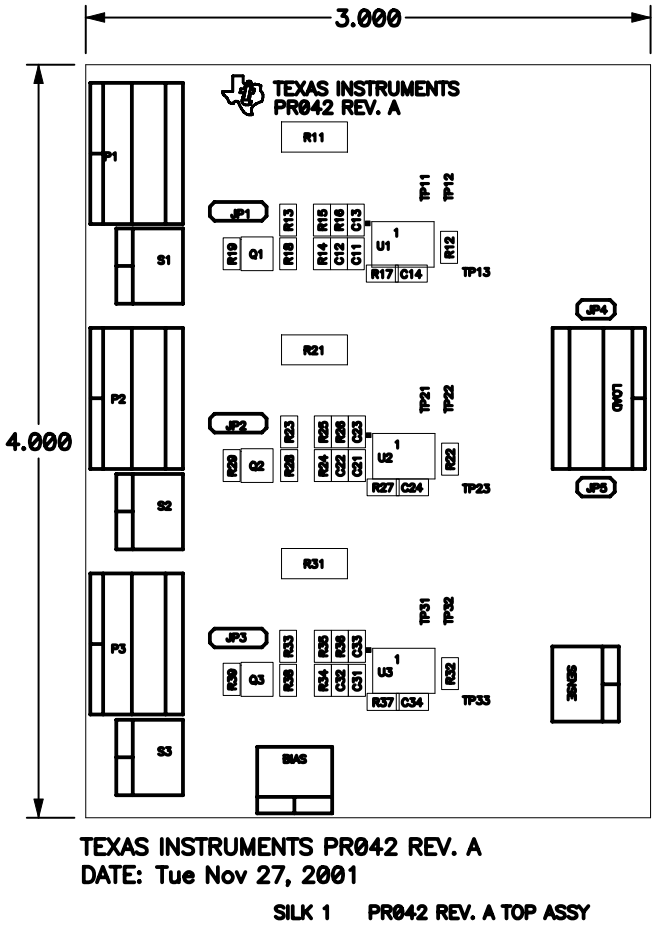

Figure 8. Top Layer Assembly

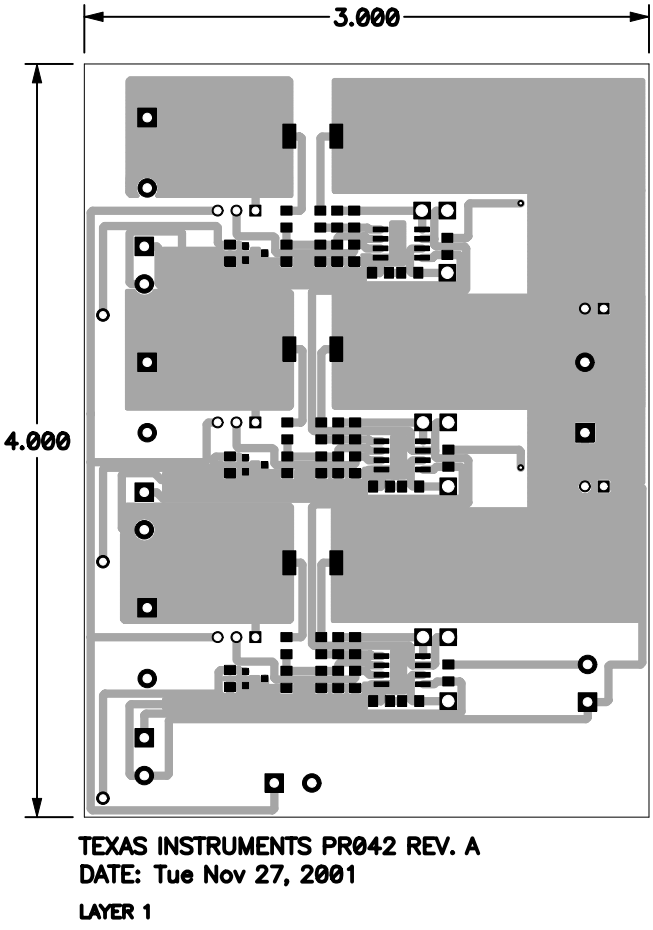

Figure 9. Top Layer

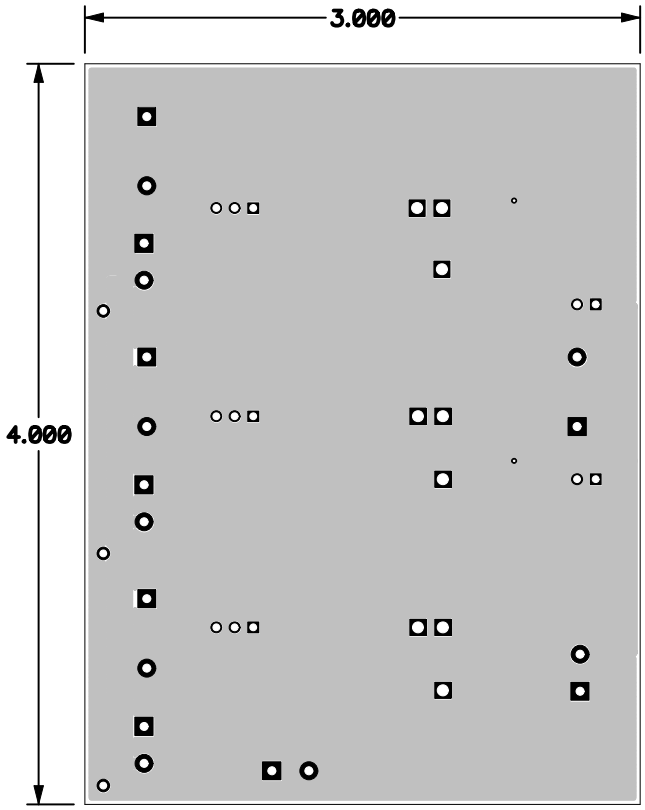

Figure 10. Bottom Layer

5 List of Materials

Table 1 lists the board components and their values, which can be modified to meet the application requirements.

. List of Materials

	QTY	REFERENCE	DESCRIPTION	MFG	PART NUMBER
Transistor	3	Q1, Q2, Q3	N-channel, 60V, 115mA, SOT–23	ON Semiconductor	2N7002LT1
Resistor	3	R11, R21, R31	Thick film, 0.005 Ω, 1W, ±1%, 2512	Vishay–Dale	WSL–2512
	3	R12, R22, R32	Thick film, 93.1 Ω, ±1%, 1/10W, 0805	Panasonic	ERJ–6ENF93R1V
	6	R13, R23, R33, R15, R25, R35	Thick film, 274 Ω, ±1%, 1/10W, 0805	Panasonic	ERJ–6ENF2740V
	6	R14, R24, R34, R16, R26, R36	Thick film, 16.2 kΩ, ±1%, 1/10W, 0805	Panasonic	ERJ–6ENF1622V
	3	R17, R27, R37	Thick film, 475 Ω, ±1% , 1/10W , 0805	Panasonic	ERJ–6ENF4750V
	3	R18, R28, R38	Thick film, 1.0 kΩ, ±5%, 1/10W , 0805	Panasonic	ERJ–6GEYJ102V
	3	R19, R29, R39	Thick film, 47.5 kΩ, ±1%, 1/10W , 0805	Panasonic	ERJ–6ENF4752V
Capacitor	3	C11, C21, C31	Ceramic, 0.47 µF, ±10%, 25V, X7R	Kemet	C0805C474K3RAC
	6	C12, C22, C32, C13, C23, C33	Ceramic, 1 nF, ±10%, 50V, X7R	Panasonic	ECJ–2VB1H102K
	3	C14, C24, C34	Tantalum, 47 µF, ±10%, 4V, Case C	Vishay–Dale	293D476X9004C2X
Terminal Block	4	P1, P2, P3	High-current (10 A) screw type terminal block (or similar)	Weidmuller	LM5.00/9.0
	5	S1, S2, S3	2 pos. 5.08mm spacing, low current (signal) screw type (or similar)	Phoenix Contact	1730612
Jumper	3	J1, J2, J3	64 pin strip, cut to 3 pins per assembly, gold plate, 0.024” tail, 0.030” pin (0.028” hole)	Mill–Max	800–10–064–10–001
	2	J4, J5	64 pin strip, cut to 2 pins per assembly, gold plate, 0.024” tail, 0.030” pin (0.028” hole)	Mill–Max	800–10–064–10–001
	5	J1, J2, J3, J4, J5 mates	5 sockets per assembly, gold plate	Mill–Max	801–93–050–10–001
Test Point	9	TP11, TP12, TP13, TP21, TP22, TP23, TP31, TP32, TP33	White 0.063 inch diameter, 1.6mm, 5012	Keystone	

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