A New Synchronization Circuit for Power Converters

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ABSTRACT

The synchronization of multiple PWM and PFC controllers is desirable for many reasons. The most common reason is that it keeps all the noise at one particular frequency and makes it easier to filter. The circuit described changes the slope of the ramp to lock the converter's switching frequency to an applied signal by a phase locked loop turning it into a voltage controlled oscillator. Furthermore, this circuit is suited for PWM controllers that have internal timing capacitors, such as the UCC28510 family and the UCC38083 family or that have more than one function dependant on the ramp such as maximum duty cycle limiting.

The circuits takes both the frequency of the converter and the frequency of the synchronization signal and mixes the two resulting in a pulse width modulated signal that is changing at the beat frequency of the two signals. This signal is used to increase or decrease the current that is charging the timing capacitor forcing the frequency of the converter to match the incoming synchronization signal.

This approach results in:

1. Synchronization of converters where the timing capacitor is unavailable and there is no synchronization pin available.
2. Uniform ramp amplitude from unit to unit therefore stable voltage gain and current compensation.
3. No distortion of the ramp which allows for maximum duty cycle limiting.

1 Introduction

The synchronization of earlier PWM controllers (eg. UC3842) has usually been implemented by applying a pulse to the timing capacitor at the CT pin that results in the reset of the timing capacitor voltage being forced to occur earlier in the cycle than would naturally occur. This results in an effective decrease in the ramp amplitude and affects the gain of the voltage controlled feedback loop. If the ramp is used to limit duty cycle then this too is thrown off. In addition the converter frequency can only be increased by this method. With many controllers having frequency tolerances as high as +/– 20%, to ensure that you can synchronize, you have to set the unit to run at a frequency such that if the natural frequency of this converter is high, it will still be lower than the synchronization frequency. The pulse applied to the CT has to be large enough so that if the converter is running at its lowest frequency it can still be *pulled in*. This means that the pulse applied must be as high as 50% of the natural ramp amplitude.

However some newer controllers also provide a dedicated synchronization pin. This too terminates the ramp waveform early and reduces the effective ramp amplitude. Again the ramp may be reduced in amplitude by as much as 50%.

Certain newer converter controllers can not be synchronized in the conventional manner due to the inability to affect the timing capacitor ramp with an externally applied pulse. One of these is the UCC28517 PFC controller. This controller has neither an external timing capacitor nor a synchronization pin. However, it does have a buffered ramp output.

A new method described here preserves the linearity of the ramp, allows the free running frequency to be set using the nominal components to the nominal desired frequency and allows the frequency to be adjusted up or down to lock to the external clock without varying the ramp amplitude. Though this circuit was developed for controllers that had internal timing capacitors and no synchronization pin, it can be used for almost any converter. This circuit uses the buffered ramp as an input, but any signal that indicates the frequency of the internal converter can be used.

2 Circuit Description

The circuit described below in Figure 1 shows how to synchronize an UCC28517 converter.

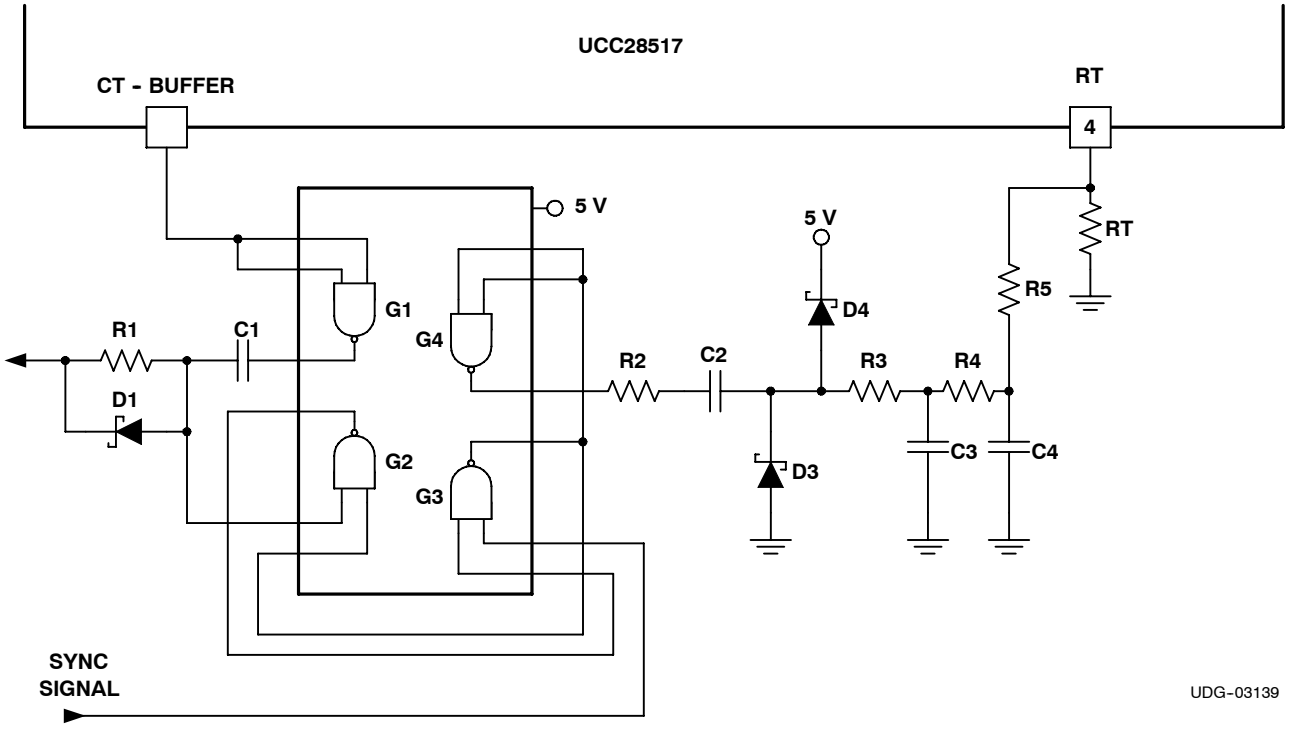

Figure 1. Synchronization Circuit for the UCC28517

A very narrow negative going pulse is generated from the buffered ramp of the UCC28517 and is one of the inputs into the two input NAND gate G2.

This is accomplished by having the ramp injected into the dual inputs of a two input NAND gate (G1) which sharpens the edges and buffers the ramp from any loading. The output of G1 is capacitively coupled by C1 to one of the inputs of the second NAND gate G2. That input is resistively tied high by R1 and will pulse low at the falling edge of the first NAND gate G1. Schottky diode D1 is added so that when the output of G1 goes high the voltage on the input to G2 is kept at the Vcc of the CD4011.

A third NAND gate G3 has one of its inputs connected to the incoming synchronization signal. This signal is normally high but pulses negative at the sync frequency. The output of the second NAND gate G2 is connected to the second input of the third NAND G3 gate and the output of the third NAND gate G3 is connected to the second input of the second NAND gate G2. NAND gates G2 and G3 form a set-reset flip-flop where negative going edges will trigger a change of state.

Both the inputs of the fourth NAND gate G4 of the CD4011 are connected to the third NAND gate G3's output which is acting as a buffer for the signal. The output of this gate is dc isolated from the remainder of the circuit by C2 and the resistor R2 which acts to limit the instantaneous power out of the device. C2 also prevents any dc bias from being applied to the converter in the event of the synchronization signal being lost. A dc bias at this point would result in a shift in frequency. A positive dc voltage would result in a low frequency and a zero or ground potential would result in a higher frequency.

The output of G4 is shown below in Figure 2 and Figure 3. Both figures contain the ramp voltage as the top trace and the bottom trace is the incoming synchronization signal. The signal in the middle is the output of G4. This waveform is a reflection of the difference in the phase between the synchronization signal and the ramp signal of the UCC28517. When the sync frequency is lower than the converter's natural frequency the average of the G4 output is high (phase shifted in one direction). When the sync frequency is higher than the converter's natural frequency the G4 output average is a low voltage (phase shifted in the other direction). This signal is passed through C2. Note that the ramp in both cases is both linear through the cycles and that both of the ramps are the same amplitude. This means that the gain does not change in the voltage control loop as a function of frequency and that the maximum duty cycle clamp in the UCC28517 will be unaffected.

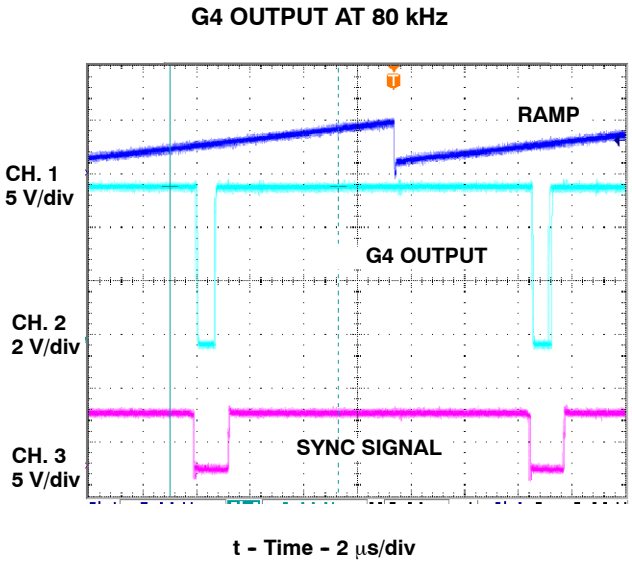

Figure 2

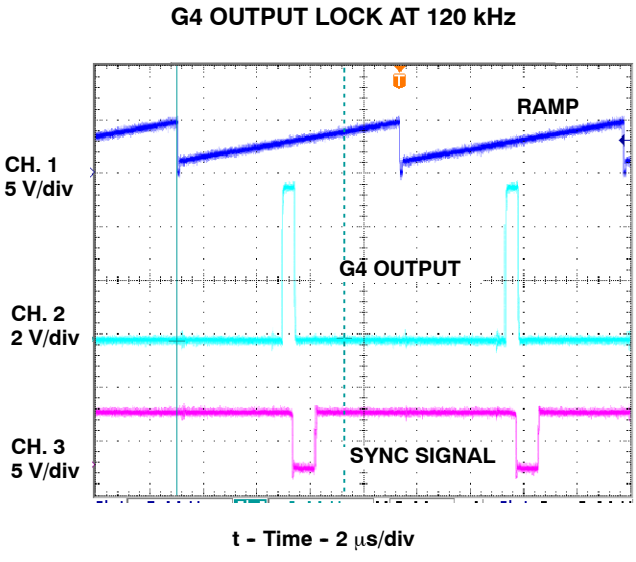

Figure 3

The ac signal from C2 is limited to be between –0.5 V and V+ plus 0.5 V by diodes D3 and D4. The resulting waveforms will generate a pulse width modulated voltage that when filtered by R3 and C3 (see Figure 4) and then further filtered by R4 and C4 (See Figure 5) results in a dc voltage that is a function of the difference in the phase of the ramp from the UCC28517 as represented by the signal at the input of G2 and the incoming sync signal. Care must be taken to keep the filtered output from resulting in a 180 degree phase shift of the signal on C4. The filtered voltage is connected to the RT pin of the UCC28517 via R5.

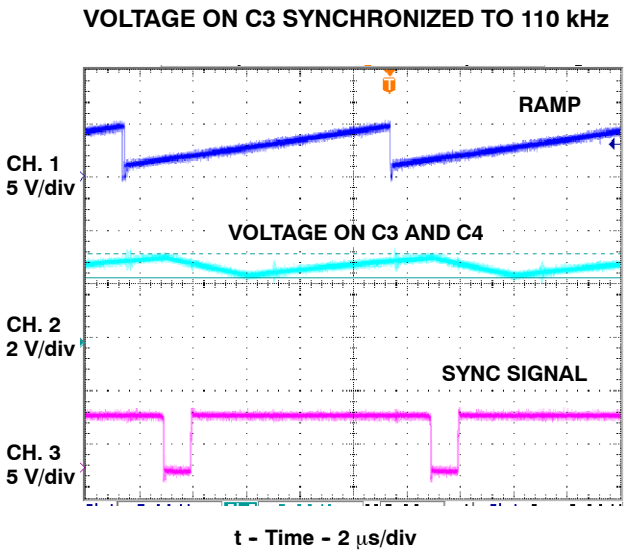

Figure 4

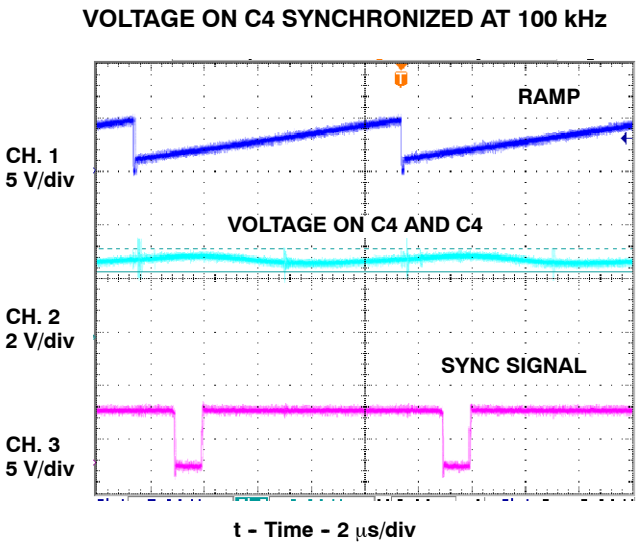

Figure 5

The voltage on the RT pin is fixed but the current coming out of the RT pin is normally the current that is going through RT. If there is no signal going through C2 then all the current out of the RT pin goes down RT. This current is mirrored on the inside of the UCC28517 and is the current that is used to set the current into the internal CT of the UCC28517.

The filtered voltage on C4 is connected to the RT pin. If the voltage on C4 is less than the voltage on the RT pin additional current is drawn from the RT pin and hence the current into the internal CT is increased and the ramp slope increases resulting in an increase in frequency.

Similarly if the voltage on C4 is greater than the voltage on the RT pin the current through R4 flows into RT and decreases the current flow from the RT pin of the UCC28517 resulting in a decrease in current flow from the RT pin. This decrease in current flow causes the current into the internal CT to decrease and the slope of the voltage ramp to decrease resulting in a decrease in frequency.

If the circuit is not locked up (in sync) the voltage that appears on the C2 R3 junction is a phase shifting waveform that would, if the averaged voltage per cycle were used, appear as a ramp voltage. Depending on which of the two signals was the higher frequency the ramp would either be ascending (sync signal slower than internal oscillator. See Figure 6) or descending (sync signal faster than internal oscillator. See Figure 7) and at the beat frequency of the two signals.

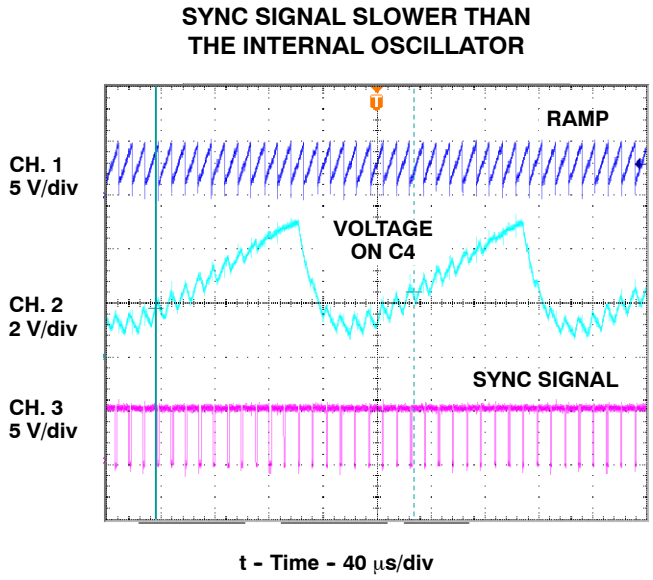

Figure 6

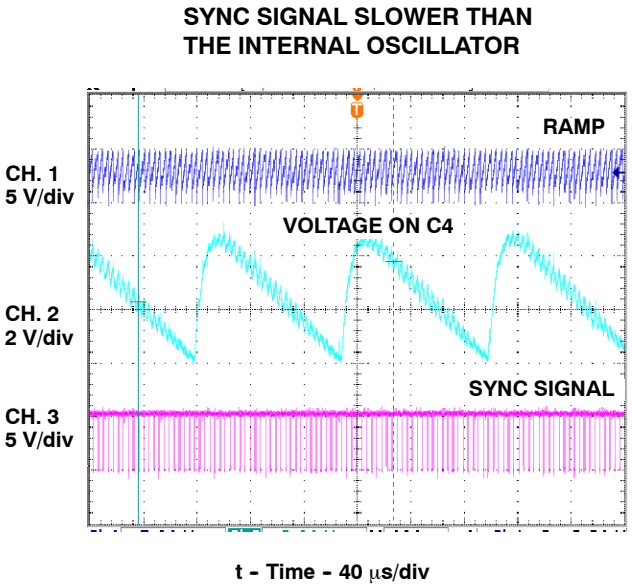

Figure 7

The filter consisting of R3–C3 was set with a 3 dB point at a factor of about 6 below the internal ramp frequency. In this case the ramp frequency was 100 kHz and the filter was set at about 25 kHz with a 6.1-kΩ resistor and a 1-nF capacitor. The second filter R5–C5 has to have a much higher impedance than the first to limit the influence on the first so a 25-kΩ resistor and 100-pF resistor with a filter 3 dB frequency of 60 kHz was used.

The idea with the filters is that the voltage that is presented must be as close as possible to a dc value but that it must be able to change enough to capture the unit when the two are out of sync.

If you assume that the power converter might be as much as 20% out (depending on the device and components) you want to be able to adjust the current out of the RT pin enough to cause the circuit to lock. To do that you have to have the voltage on C4 change enough so that the current through R5 will swing as the beat frequency is applied to the inputs of the filters. RT was set at 287 kΩ to achieve a free running frequency of 100 kHz. R5 was set at 402 kΩ to achieve the +/– 20% frequency adjustment If a wider range were desired R5 could have been decreased.

3 Measured Data

The circuit's nominal frequency was adjusted to 100 kHz and then this circuit was added. The synchronization signal was applied to the input and the frequency was varied. The circuit was found to be able to swing from 80 kHz to 120 kHz without any problems.

4 Other Circuits

There are new lines of converters that are appearing that have no ramp waveform available. The output of the converter (the switch drive) can be used instead of the ramp with proper buffering. Even those with dual outputs can be used in the same manner. An example of the configuration necessary for the UCC38083 (a controller where there is no ramp output) is shown in Figure 8.

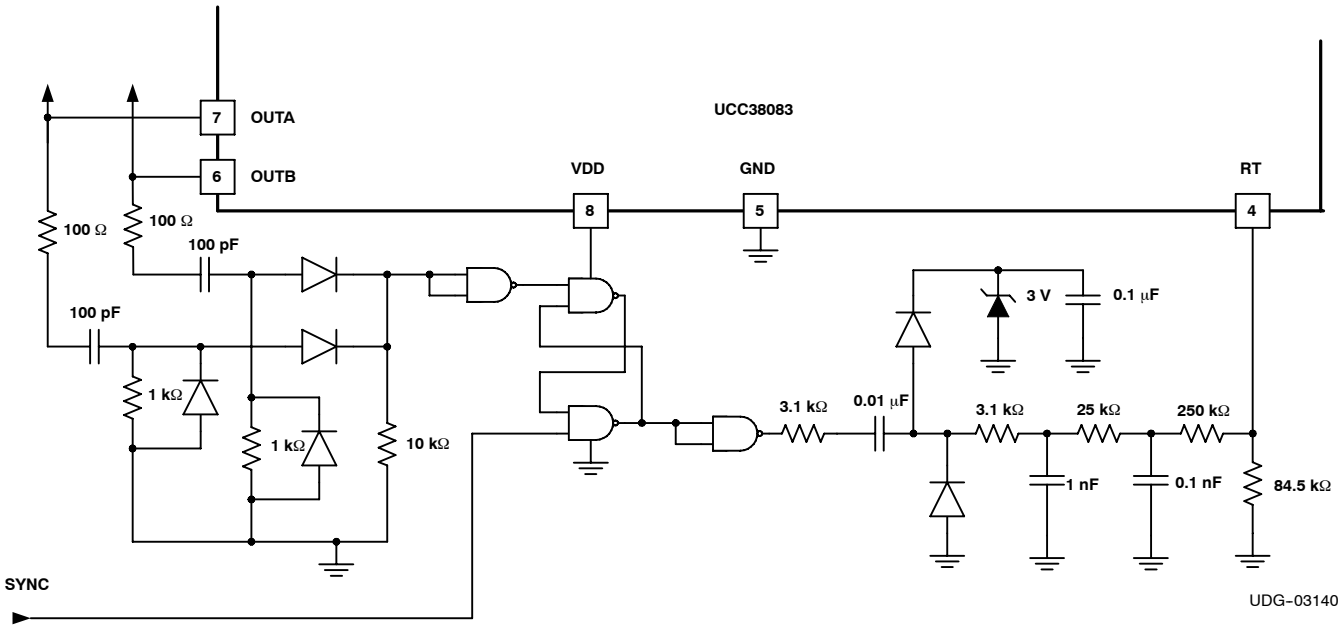

Figure 8. Synchronizing the UCC38083

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