

## ***Frequency Dithering With the UCC28950 and TLV3201***

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### **ABSTRACT**

For some power-supplies, even after careful considerations throughout the design cycle the issue of Electro-Magnetic Compatibility (EMC) still remains. One final tool available to power designers is the use of Frequency Dithering to pass EMC compliance testing. This paper demonstrates a simple circuit that could be used when such a need arises.

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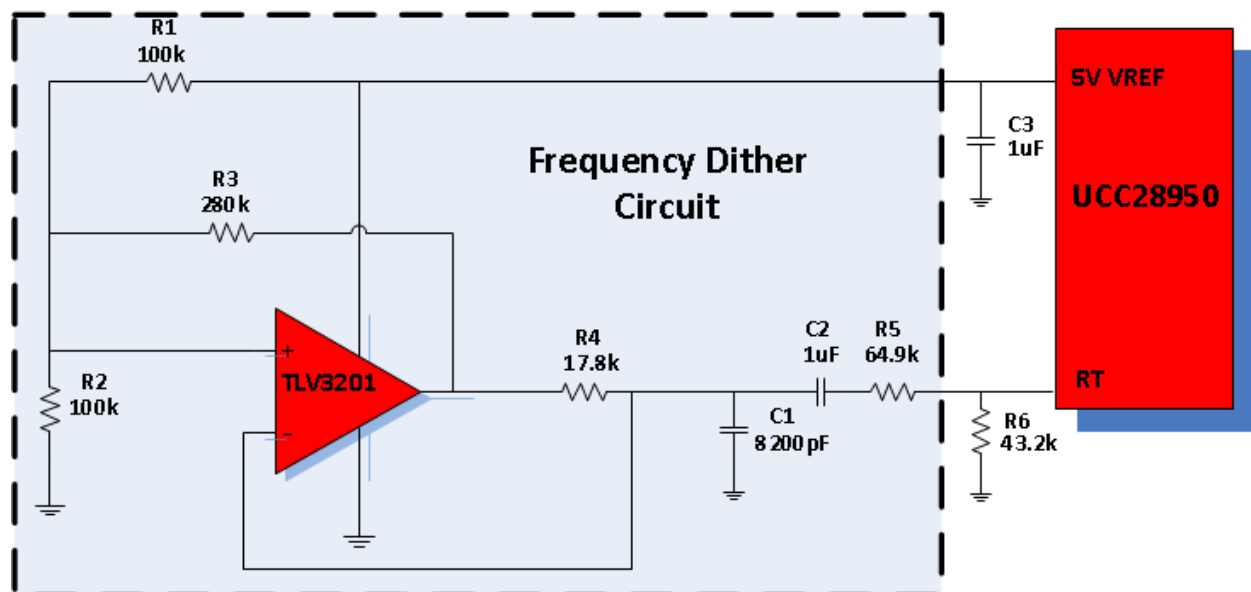
## I. Introduction:

One of the greatest challenges in designing switching power supplies is limiting its Electromagnetic Interference (EMI) with other electronics. Beyond layout techniques to minimize high di/dt current loop areas and snub high dv/dt nodes, extensive filtering, slowing switching edges, and shielding, one method for limiting such interference and/or becoming certified by regulatory agencies is to spread the frequency spectrum of the main oscillator, also called adding “frequency dither” to the oscillator. This small variation in switching frequency decreases the narrowband emissions by changing the frequency content of the converter from a relatively narrowband spectrum to more wideband. To demonstrate how to design such a dither circuit, this article will showcase a simple example using a [TLV3201](#) comparator to add dither to a [UCC28950](#) phase-shifted full-bridge controller. This article is intended as more of a practical example. For a detailed observation on the theory that lends to this article, please see the provided references.

## II. Background:

Though the electromagnetic emissions of a switch-mode power supply are indeed spread across many frequencies by using a square-wave pulse, the greatest energy is at the fundamental frequency. If we were to slightly vary the fundamental frequency, we would see that the peak energy would be shared among multiple fundamental frequencies. The total EM energy remains the same, but narrowband energy has been decreased.

A typical circuit to apply such a function can be seen in Figure 1 below:



**Figure 1.** Typical Dither Application Circuit with UCC28950 and TLV3201

In essence, we are seeking to modulate our fundamental frequency slightly. For the UCC28950, the switching frequency is set by the choice of resistor value at the Rt pin. With the controller set as a master, this resistor is tied from the Rt pin to the Vref pin which supplies a 5V source. For a slave

configuration the  $R_t$  resistor is tied to ground. The  $R_t$  pin itself has an internal 2.5V source and therefore the current into or out of the  $R_t$  pin (depending on Master/Slave configuration) determines the switching frequency of the controller. This frequency-setting method is very similar to most power-supply controllers available and thus this dithering circuit can apply to nearly all modern power controllers. Our practical objective will therefore be to apply a time-varying current signal to modulate the dc-current set by the  $R_t$  resistor to add a small periodic variation in the main controller frequency.

### III. Example using a small UCC28950 Control Card:

The UCC28950 control circuit seen in the appendix was used for this example.

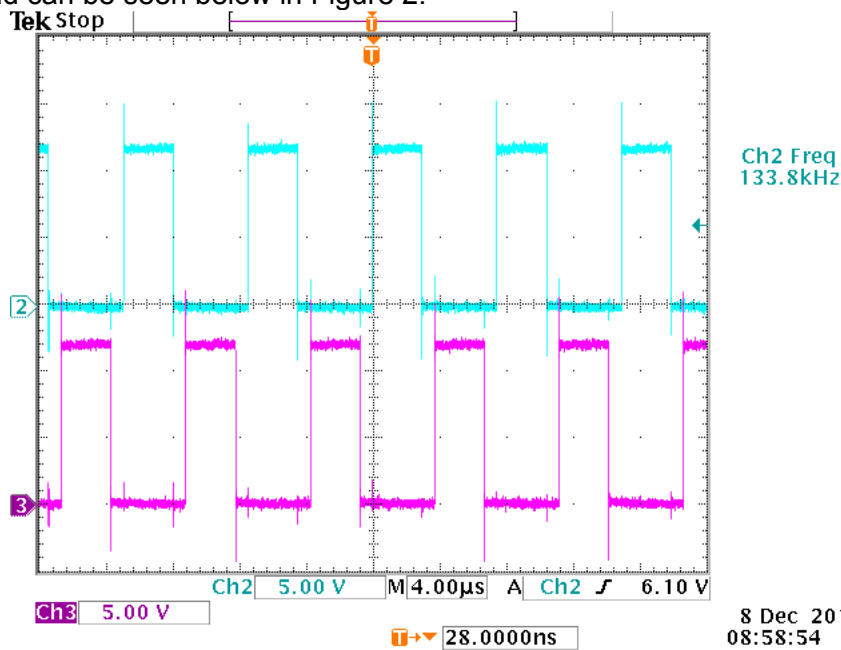
For all scope measurements, the following equipment was used:

#### Equipment:

- a. Oscilloscope: Tektronix TDS3054 at full BW of 500MHz
- b. Scope Probes: Tek5050, 500MHz, 11.1pF, 10Mohm, 10X

#### 1) Original Circuit:

For this control card, the  $R_t$  resistor was set to 43.2K. From Figure 11 in the [UCC28950 datasheet](#), this  $R_t$  resistor value equates to a switching frequency of approximately 133kHz. This is verified on the hardware and can be seen below in Figure 2:



**Figure 2.** Two Output Signals of the UCC28950 without dithering added

**Ch2** = OUTA Signal of controller  
**Ch3** = OUTB Signal of controller

## 2) Calculations:

(Note: Refer to the schematics seen in Figures 1 or 3 for component references.)

### a. Controller Frequency Variation Goal:

133kHz is the center frequency from which we want to vary the oscillator. The variation should not be excessive since the designed component values were chosen based on operating at that frequency. Therefore, we will choose to vary the frequency by +/- 10% for an effective variation of 20%.

Originally, with the 43.2k Rt resistor tied to 5V (Vref pin) and 2.5V (Rt pin itself),  $(5-2.5)/43.2k = 57.87\mu A$  is being supplied into the Rt pin and setting the switching frequency. Though the switching frequency is not a linear proportion of the current and the Rt resistor, since it does not need to be exact we will choose to vary the current by +/- 10% to achieve our proper dithering goal of 20%. Therefore, we will vary the current going into the Rt pin by +/- 6uA.

### b. Modulation Signal Amplitude Goal:

To keep the frequency centered at 133kHz, we need to vary the current into the Rt pin above and below 57.87uA by +6uA and -6uA. To do that, we need to vary the voltage above and below 2.5V and then add a series resistor to set the current. We will choose to vary the voltage from 2.1V to 2.9V for a modulating signal amplitude of 0.8V.

### c. Modulation Signal Frequency Goal:

To vary the current at Rt, the comparator circuit will be designed to supply a time- varying signal AC-coupled to the Rt pin. It is generally advised that the modulation frequency be at least an order less than the fundamental switching frequency of 133kHz. For most EMC test equipment, a bandpass filter is used on the front end to limit noise and improve resolution at the desired frequencies. The lower cutoff frequency of some of this equipment is 9kHz. As such, for the dither to have any effect on the measurements, the dither frequency itself must be higher than this frequency. We don't want the frequency to be too high though because that could interfere with the performance of the power supply itself. Therefore, for our example we will choose a modulating frequency of 11kHz. This results in a period (T) of  $1/11kHz = 90\mu s$ .

The output of the comparator changes from GND to full rail of 5V (tied to 5V Vref of the UCC28950). This output will be tied through a resistor to a capacitor to create a charging/discharging sequence that will become our modulating signal. By choosing a reasonable series resistor of 17.8k(R4) and knowing that the voltage difference across the resistor will on average be  $(5V-2.5V) = 2.5V$ , we will have both a charging and discharging current of 140uA to a capacitor.

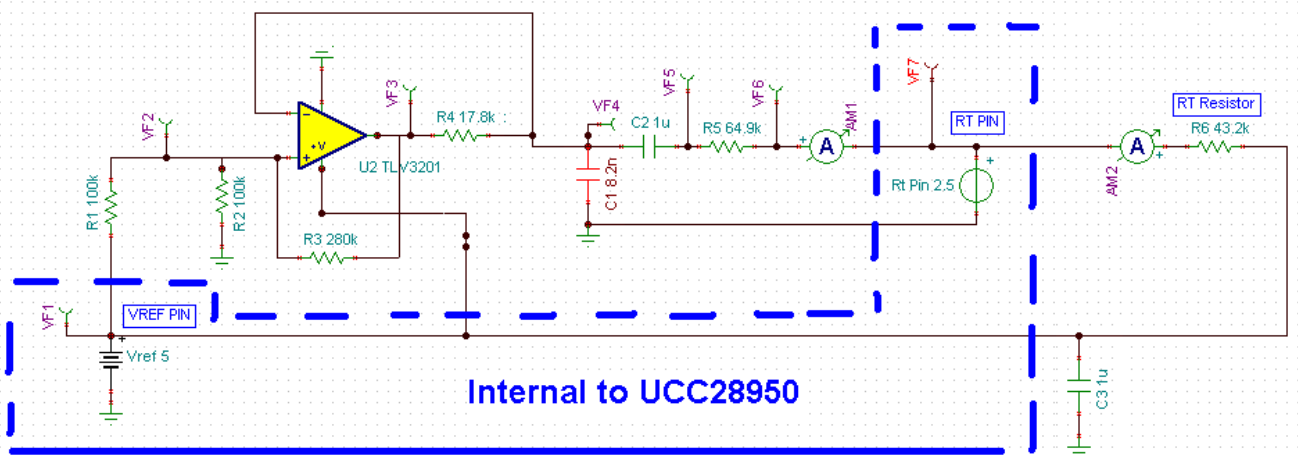
From **b.** above, the modulating signal will charge and discharge from 2.1V to 2.9V and back again. Knowing  $I = C dv/dt$ , having I and dv and knowing that the charge(or discharge)  $dt = \frac{1}{2} * T = 45\mu s$ , we achieve a capacitor value of ~ 8000pF. Therefore we select a standard 8200pF cap to be the charge/discharge cap(C1) to set the modulating frequency.

### d. Series Resistor for Modulating Current Goal:

With 2.9V chosen as the upper voltage of the (modulation+2.5V DC), the series resistor needs to be  $(2.9V-2.5V)/6\mu A = 66K\Omega$ . We will use the standard resistor value of 64.9 KΩ(R5). At 2.9V, it can be seen by the positive current that this current will sum with the original 57.87μA and be greater, resulting in a slightly higher frequency. Likewise, it can be seen that at 2.1V (modulation+2.5V DC)  $(2.1V-2.5V)/64.9 K\Omega = -6.16\mu A$ . The negative here signifies that current will be pulled away from the Rt pin and thus the current going into the Rt pin will be less. This will result in a lower current entering the Rt pin and thus a slightly lower switching frequency.

### 3) Dither Circuit Simulation:

The following circuit was assembled in the [TINA-TI SPICE](#) circuit simulator to prove the dither circuit before hardware assembly:



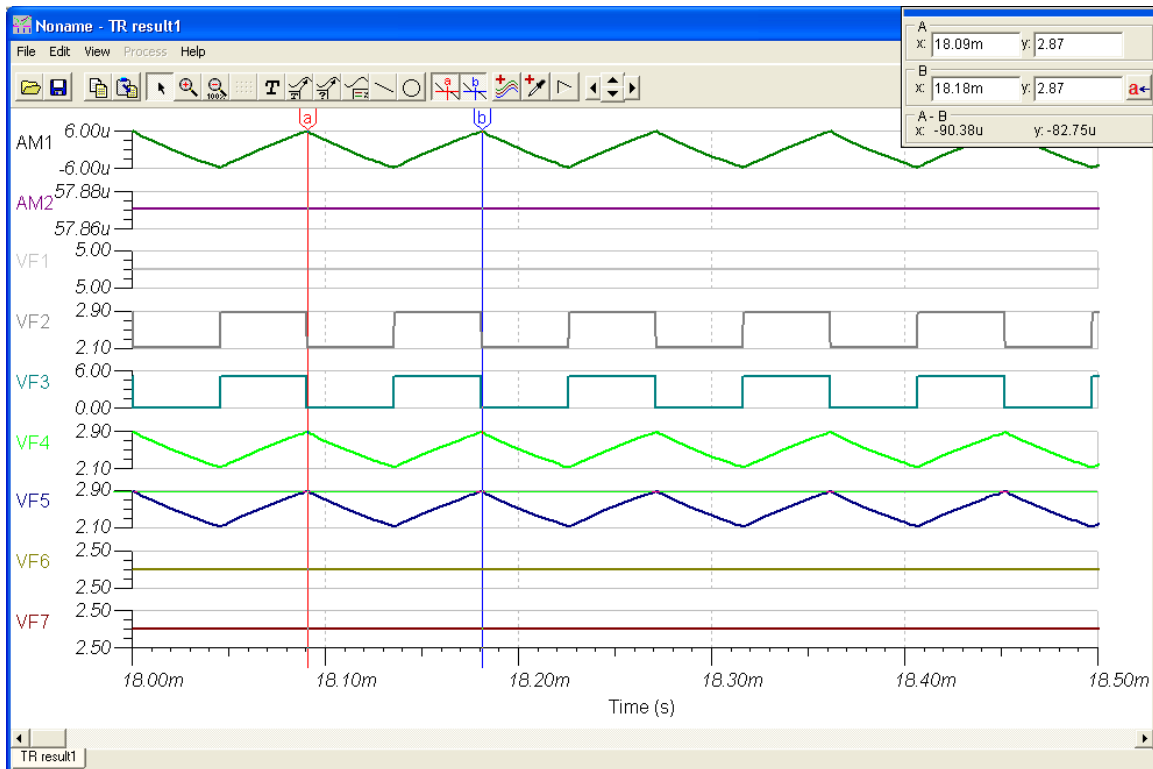
**Figure 3.** TLV3201 Comparator Frequency-Dither Circuit in SPICE simulator

R3 was chosen as 280K so that when the output of the comparator (VF3) switches high to 5V, R3 // R1 and the non-inverting pin (VF2) goes to the 2.9V reference threshold. Likewise, when the output of the comparator switches low to 0V, R3 // R2 and the non-inverting pin goes to the 2.1V reference threshold. This action of switching occurs as the inverting pin charges and discharges from 2.1V to 2.9V because of the capacitor C1. The capacitor C2 is added to AC-couple the signal from the comparator to the 2.5V source at the Rt pin.

From a high-level, the circuit functions like this:

- A. Upon initial power-up, the output of the comparator goes high to 5V, setting the non-inverting(+) pin to 2.9V. This begins charging of C1, increasing voltage at the inverting(-) pin.
- B. When the (-) pin charges above the 2.9V threshold set at the (+) input, the output VF3 goes to 0V. This begins discharging of C1 and decreasing voltage at the (-) pin. The (+) pin threshold instantly changes to 2.1V as well.
- C. After the (-) pin discharges down below the 2.1V threshold seen on the (+) pin, VF3 goes high again and the process repeats.

To better assist in understanding the operation of the circuit, see the waveforms in Figure 4 below:



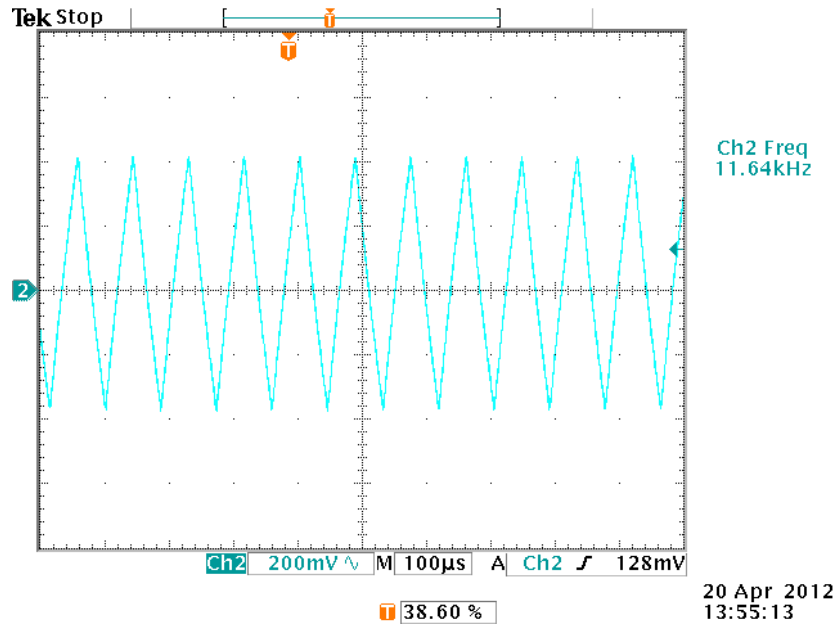
**Figure 4.** Performance of Comparator Circuit in Simulation

The current read at the ammeter AM2 shows the DC current we expected of 57.87uA from the  $R_t$  resistor alone. The current read at AM1 at the top of Figure 4 is the modulating current of +/- 6uA, which was our circuit goal. Therefore, from the simulation the circuit is verified.

#### 4) Dither Circuit Hardware:

The UCC28950 control card Vref pin was tied to the TLV3201 VCC pin and VF1 node seen on the comparator simulation schematic through 1uF+0.1uF bypass decoupling ceramic capacitors along with a 22uF electrolytic bulk cap to prevent impedance instability from the wire inductance.

Before connecting VF6 of the comparator board to the  $R_t$  pin of the UCC28950, the following waveform was observed at VF5:

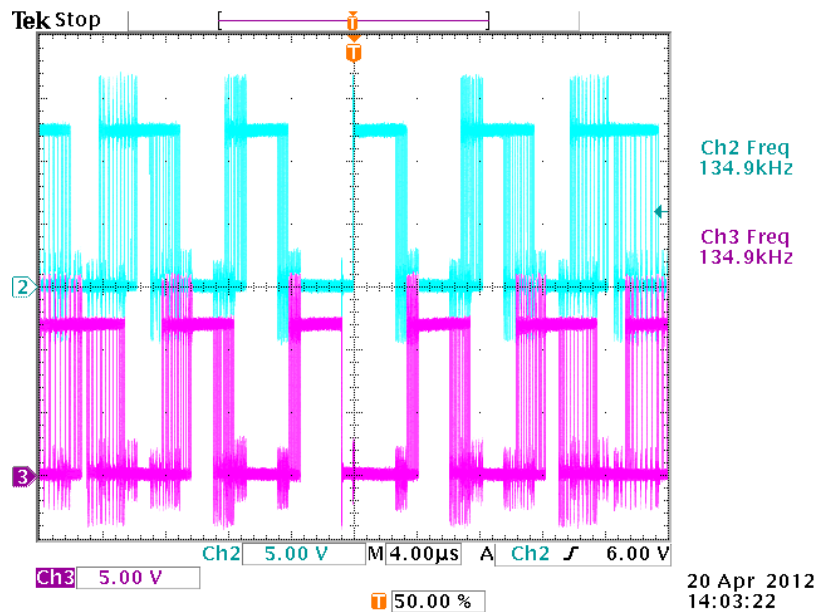


**Figure 5.** Hardware-tested output of Comparator Board

**Ch2** = VF5 of Comparator board

From Figure 5, we can see the 800mV, 11.64kHz modulation signal, which is very close to our design goals for the modulating signal in terms of voltage and frequency.

After connecting VF6 of the comparator board to the Rt pin of the UCC28950, the OUTA and OUTB signals of the UCC28950 can be observed below in Figure 6:

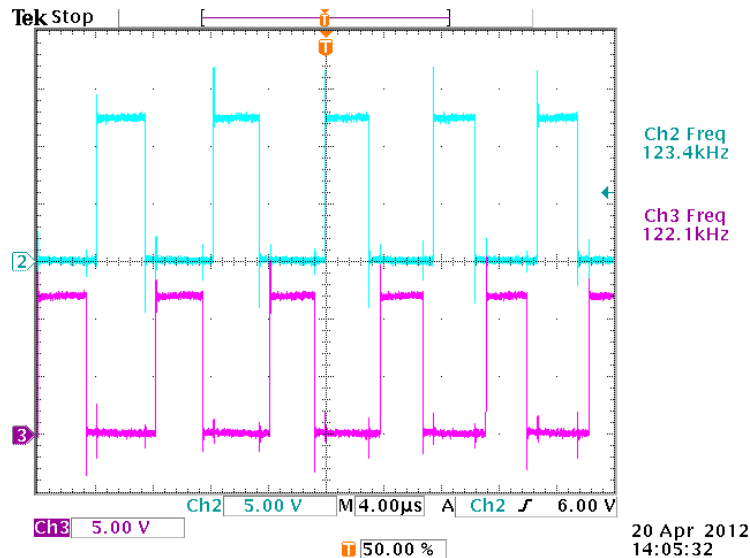


**Figure 6.** Two Output Signals of the UCC28950 with dithering added

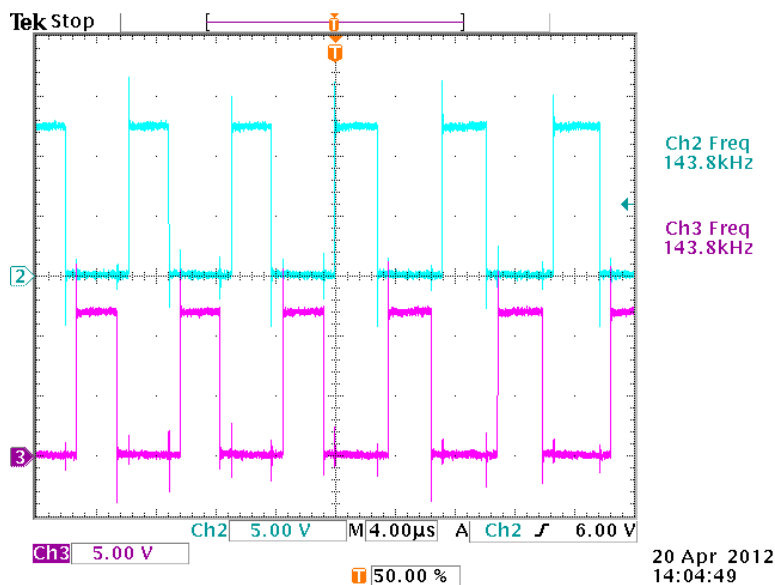
**Ch2** = OUTA Signal of controller

**Ch3** = OUTB Signal of controller

Here in Figure 6 the slight frequency variation of the outputs, and thus the main internal oscillator, can be observed. If we were to view different single captures of these signals, the frequency would be different each time. This can be observed in Figures 7 and 8. The frequency is varying both above and below the 133kHz center frequency.



**Figure 7.** Two Output Signals of the UCC28950 with dithering added (single capture = ~ 122kHz)  
**Ch2** = OUTA Signal of controller  
**Ch3** = OUTB Signal of controller



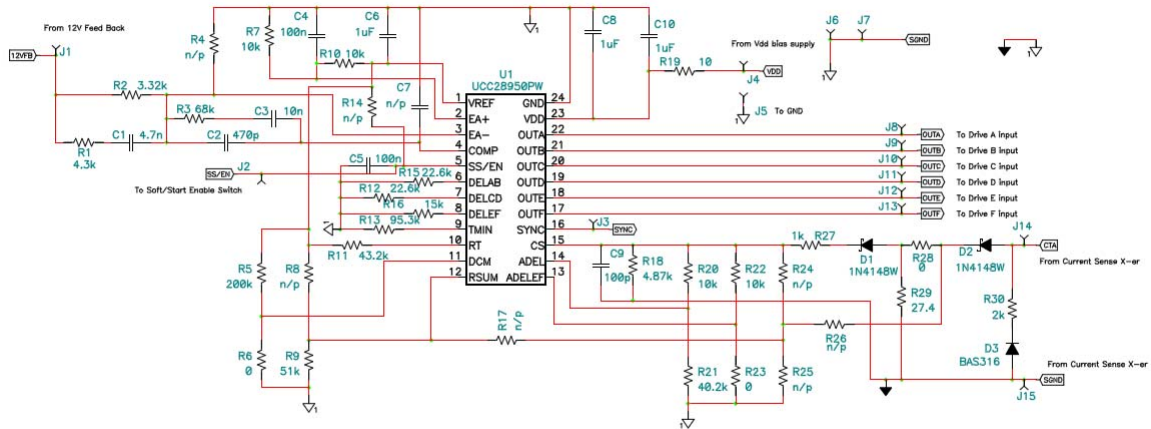
**Figure 8.** Two Output Signals of the UCC28950 with dithering added (single capture = 144kHz)  
**Ch2** = OUTA Signal of controller  
**Ch3** = OUTB Signal of controller



**IV. Conclusions:**

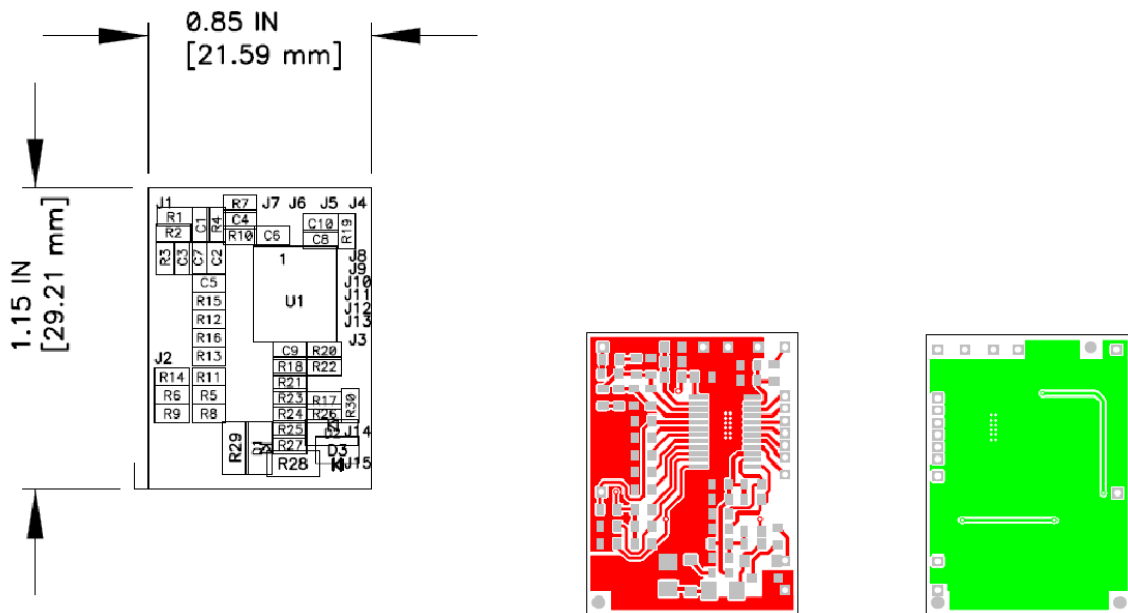
This Application Note has explained how to design a circuit using the TLV3201 comparator to dither the switching frequency of a UCC28950 phase-shifted full-bridge controller. It has been seen that with just a few simple components, the current can be varied into the frequency setting  $R_t$  pin of the controller to spread the frequency spectrum of the converter, which in turn will spread the EMI emissions to lower the narrowband energy amplitude for EMC/I compliance.

**V. Appendix: UCC28950 Control Card Schematic and Layout:**



Note 1. n/p means non populated  
 Note 2: First engineering samples have pin out in accordance to U1 and ON/OFF DCM mode. The final part will have pin DCM and RSUM swapped and gradually reduced OUTE and OUTF signals as function of load current. Some functionality differences between the first samples and the final version are described in the "Errors Sheet, June 28, 2009" document that will accompany the samples.

**App 1: UCC28950 Small Control Card Schematic**



**App 2: UCC28950 Small Control Card Layout and Assembly**

## References

1. *“Dither a power converter’s operating frequency to reduce peak emissions”, Bob Bell and Grant Smith, EDN Magazine, October 13, 2005*
2. *“Understanding Noise-Spreading Techniques and their Effects in Switch-Mode Power Applications”, John Rice, Dirk Gehrke, and Mike Segal, Unitrode Power-Supply Design Seminar SEM1800, 2008/2009, Available online at <http://www.smeps.us/Unitrode.html>*
3. *“PFC Pre-Regulator Frequency Dithering Circuit”, Mike O’Loughlin, Texas Instruments’ Literature No. SLUA424A, May 2007*
4. *“Understanding and Optimizing Electromagnetic Compatibility in Switchmode Power Supplies”, Bob Mammano and Bruce Carsten, Texas Instruments’ Literature No. SLUP202*

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