# Power over Ethernet Consortium
## Clause # 33 PSE Conformance Test Suite v 2.9 Report

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Report Rev. 1.1 – SLUA718

Enclosed are the results from the Clause # 33 PSE Conformance testing performed on:

| | |
|---|---|
| Device Under Test (DUT): | Texas Instruments TPS23861 |
| IOL ID: | 18870 |
| Port Tested: | 1 |
| Hardware Version: | TPS23861EVM-613 |
| Configuration Information: | The LED jumper for port 1 was removed for the duration of testing, as it was suspected to present a parallel load and interfere with the DUT's ability to accurately measure the current draw at the MDI. |

The test suite referenced in this report is available at the UNH-IOL website:

ftp://ftp.iol.unh.edu/pub/ethernet/test_suites/CL33_PSE/PSE_test_suite_V2.9.pdf

| The Following Tests Exhibited Non-Conformant Behavior |
|---|
| No issues were discovered during Clause 33 PSE Conformance Testing. |

| The Following Tests Were Either Not Performed Or Have Additional Comments | |
|---|---|
| **33.1.9 – Physical Layer Classification (part f)**<br>**33.2.2 – Load Regulation (part a)**<br>**33.4.1 – Midspan PSE Return Loss**<br>**33.4.2 – Midspan PSE Insertion Loss**<br>**33.4.3 – Midspan PSE NEXT Loss** | These tests are currently under development. |
| **33.1.13 – Alternative B Backoff Cycle** | This test only applies to devices that power on Alternative-B. |
| **33.2.6 – PSE Current Unbalance (part a)** | This test does not apply to Type-2 PSE's. |
| **33.3.6 – Range of $T_{MPDO}$ Timer (part b)**<br>**33.3.9 – AC MPS Signal Parameters**<br>**33.3.10 – AC MPS Signature** | These tests do not apply to devices that do not support AC disconnect. |
| **33.3.7 - PD MPS Dropout Current Limits ($I_{MIN}$ measurement)** | The LED jumper for port 1 was removed for the duration of testing, as it was suspected to present a parallel load and interfere with the DUT's ability to accurately measure the current draw at the MDI. |
| **33.4.4 – PSE Impedance Balance**<br>**33.4.5 – PSE Common Mode Output Voltage** | These tests do not apply to devices without a PHY. |

For specific details regarding issues please see the corresponding test result.

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## Result Key

The following table contains possible results and their meanings:

| Result | Interpretation |
|---|---|
| **PASS** | The Device Under Test (DUT) was observed to exhibit conformant behavior. |
| **PASS with Comments** | The DUT was observed to exhibit conformant behavior however an additional explanation of the situation is included, such as due to time limitations only a portion of the testing was performed. |
| **FAIL** | The DUT was observed to exhibit non-conformant behavior. |
| **Warning** | The DUT was observed to exhibit behavior that is not recommended. |
| **Informative** | Results are for informative purposes only and are not judged on a pass of fail basis. |
| **Refer to Comments** | From the observations, a valid pass or fail could not be determined. An additional explanation of the situation is included. |
| **Not Applicable** | The DUT does not support the technology required to perform these tests. |
| **Not Available** | Due to testing station or time limitations, the tests could not be performed. |
| **Borderline** | The observed values of the specified parameters are valid at one extreme, and invalid at the other. |
| **Not Tested** | Not tested due to the time constraints of the test period. |

## Revision History

| Revision | Explanation |
|---|---|
| 1.0 | Initial Version |
| 1.1 | The report was re-issued to include a TI reference number per request of TI. This was placed at the end of the Report Revision number. |

## Test Setup

| Testing Equipment | |
|---|---|
| Real-time DSO | TEKTRONIX, TDS 3014 |
| Current Probe and Amplifier | TEKTRONIX, TPS305 and TPSA300 |
| Digital Multimeter | HEWLETT-PACKARD, 34401A |
| Digital Power Supply | AGILENT TECHNOLOGIES, E3641A |
| Chroma DC Electronic Load | Chroma,6312A,0,01.40,0 |
| UNH-IOL Developed Test Board | PoE Shark Board Rev4.0 |

### Basic Testing Configuration

The basic testing configuration is defined in the UNH Interoperability Laboratory PSE Parametric Test Suite v2.9

## GROUP 1: DETECTION CHARACTERISTICS

| Test # and Label | Part(s) | Result(s) |
|---|---|---|
| **33.1.1 – Valid PSE Pinout** | **a** | **PASS** |
| **Expected Results and Procedural Comments** | | |
| Purpose: To verify that the PSE has a compliant pinout and that it is in a valid location with respect to the link segment.<br><br>a. A PSE may operate on either Alternative A or Alternative B. An Alternative A device may have either polarization. An Alternative B device must supply positive Vport on pins 4 and 5, and negative Vport on pins 7 and 8. | | |
| **Comments on Test Results** | | |
| a. The PSE is in a valid location and its power supply has a valid pinout: ALT-A MDI-X | | |

| Test # and Label | Part(s) | Result(s) |
|---|---|---|
| **33.1.2 - Open Circuit Voltage** | **a** | **PASS** |
| **Expected Results and Procedural Comments** | | |
| Purpose: To verify that the open circuit voltage at the PI of the PSE during detection mode is below the conformance limits.<br><br>a. The open circuit voltage ($V_{oc}$) should not exceed 30 Volts. | | |
| **Comments on Test Results** | | |
| a. $V_{oc}$ = 20.13 V | | |

| Test # and Label | Part(s) | Result(s) |
|---|---|---|
| **33.1.3 - Detection Circuit** | **a** | **PASS** |
| **Expected Results and Procedural Comments** | | |
| Purpose: To verify the Thevenin equivalent detection circuit of the PSE detection source.<br><br>a. If the DUT does not accept current into the Vdetect+ port, the DUT follows Figure 33–12. Otherwise, the DUT should accept current into the Vdetect+ port and the DUT should show a loaded PI voltage of less than half of the open circuit PI voltage, according to Figure 33–11. | | |
| **Comments on Test Results** | | |
| a. The DUT was observed to reject current into the Vdetect+ port. This would appear to be compliant with the Alternative PSE detection source shown in IEEE Standard 802.3-2012 Figure 33-12. Output Impedance was not calculated. | | |

| Test # and Label | Part(s) | Result(s) |
|---|---|---|
| **33.1.4 - Backdriven Current** | **a** | **PASS** |

**Expected Results and Procedural Comments**

Purpose: To verify that the detection circuit of the PSE can withstand maximum backdriven current over the range of $V_{Port}$.

a. A backdriven current of 5mA should not affect the DUT.

**Comments on Test Results**

a. The DUT was observed to properly ignore the backdriven current.

| Test # and Label | Part(s) | Result(s) |
|---|---|---|
| **33.1.5 – Detector Circuit Output Current** | **a** | **PASS** |

**Expected Results and Procedural Comments**

Purpose: To verify that the short circuit output current of the PSE during PD detection is within the conformance limits.

a. The output short circuit current should not exceed 5 mA.

**Comments on Test Results**

a. $I_{SC}$ = 0.54 mA.

| Test # and Label | Part(s) | Result(s) |
|---|---|---|
| **33.1.6 – Detector Circuit Output Voltage** | **a** | **PASS** |
| | **b** | **PASS** |
| | **c** | **PASS** |

**Expected Results and Procedural Comments**

Purpose: To verify the voltage output of the PSE's detection circuit conforms to the specified limits.

a. The loaded circuit voltage should be between 2.8 and 10V.
b. The voltage difference between detection probe voltages should be at least 1V.
c. The slew rate of the probe voltages should be no greater than 0.1V/µs.

**Comments on Test Results**

a. Probe Voltage1 = 4.56V
   Probe Voltage2 = 7.04V
   Prove Voltage3 = 4.60V
   Probe Voltage4 = 7.08V
b. Maximum observed detection probe voltage difference = 2.47 V
c. Maximum observed slew rate of the probe voltages = 0.015V/µS

Please refer to the figures appended to the report.

| Test # and Label | Part(s) | Result(s) |
|---|---|---|
| **33.1.7 – PD Detection Timing** | **a** | **PASS** |
| | **b** | **PASS** |

**Expected Results and Procedural Comments**

Purpose: To verify that the PSE probes its PI with valid detection pulses and completes an entire detection sequence within the proper time period.

a. The total pulse width of the detection pulse should not be greater than 500ms.
b. The detection probe voltages should have a duration of at least 2 ms.

**Comments on Test Results**

a. $T_{DET}$ = 159.68 ms
b. Probe Voltage1 pulse width = 73.6 ms
Probe Voltage2 pulse width = 73.6 ms
Probe Voltage3 pulse width = 74.4 ms
Probe Voltage4 pulse width = 80.8 ms
$T_{BP}$ > 2 ms

Please refer to the figures appended to the report.

| Test # and Label | Part(s) | Result(s) |
|---|---|---|
| **33.1.8 – PD Signature Detection Limits** | **a** | **PASS** |
| | **b** | **PASS** |
| | **c** | **PASS** |
| | **d** | **PASS** |

**Expected Results and Procedural Comments**

Purpose: To verify that the DUT will properly detect a PD's Signature impedance.

a. The minimum accepted input resistance should be between 15 kΩ and 19 kΩ.
b. The maximum accepted input resistance should be between 26.5kΩ and 33 kΩ.
c. The DUT should detect a proper signature if the input capacitance is less than 150nF.
d. The DUT should accept capacitances below 10µF and reject capacitances above 10µF.

**Comments on Test Results**

a. 16.3 kΩ ≤ $R_{accept(min)}$ ≤ 16.4 kΩ
b. 28.4 k Ω ≤ $R_{accept(max)}$ ≤ 28.5 kΩ
c. The DUT was observed to accept capacitances less than 150nF.
d. The DUT was observed to reject improper capacitances above 10µF.

| Test # and Label | Part(s) | Result(s) |
|---|---|---|
| **33.1.9 – Physical Layer Classification** | **a** | **PASS** |
| | **b** | **PASS** |
| | **c** | **PASS** |
| | **d** | **PASS** |
| | **e** | **PASS** |
| | **f** | **Not Available** |

**Expected Results and Procedural Comments**

Purpose: To verify that a DUT supporting Classification properly performs PD class detection.

a. For 1-Event classification the DUT should produce a single classification pulse at $V_{CLASS}$ (15.5-20.5V).
b. For 2-event classification the DUT should produce the following sequence $V_{CLASS}$, $V_{Mark}$, $V_{CLASS}$, $V_{Mark}$ where $V_{CLASS}$ is 15.5-20.5 volts, and $V_{Mark}$ is 7-10V.
c. The DUT should accurately classify the PD.
d. If the current drawn is equal to or greater than 51mA, a Tyle 1 PSE shall either return to the IDLE state or classify the PD as Class 0: a Type 2 PSE shall return to the IDLE state.
e. $I_{CLASS\_LIM}$ should be less than 100 mA.
f. For 2-Event classification $I_{MARK\_LIM}$ should be between 5 and 100mA for all mark events.

**Comments on Test Results**

The DUT was observed to implement both 1-event and 2-event Classification.

a. $V_{CLASS}$= 18.85 V
b. $V_{CLASS1}$= 18.79 V
   $V_{Mark1}$= 8.37 V
   $V_{CLASS2}$= 18.80V
   $V_{Mark2}$ = 8.38 V
c. The DUT was observed to accurately classify the PD.
d. The DUT was observed to return to the IDLE state.
e. $I_{CLASS\_LIM}$ = 73.41 mA.
f. This test is currently not implemented.

Please refer to the figures appended to the report.

| Test # and Label | Part(s) | Result(s) |
|---|---|---|
| **33.1.10 – Classification Timing** | **a** | **PASS** |
| | **b** | **PASS** |
| | **c** | **PASS** |
| | **d** | **PASS** |
| | **e** | **PASS** |
| | **f** | **PASS** |

**Expected Results and Procedural Comments**

Purpose: To verify that a PSE capable of classifying a PD completes classification within the proper time period after successfully completing the detection of a PD.

a. For the 1-Event class pulse, $T_{PDC}$ must be between 6ms and 75ms (inclusive).
b. For the 2-Event class pulse, $T_{PDC}$ must be between 6ms and 75ms (inclusive).
c. $T_{CLE1}$ must be between 6ms and 30ms
d. $T_{ME1}$ must be between 6ms and 12ms
e. $T_{CLE2}$ must be between 6ms and 30ms
f. $T_{ME2}$ must be greater than 6ms

**Comments on Test Results**

a. 1-Event: $T_{PDC}$ = 10.71 ms
b. 2-Event: $T_{PDC}$ = 39 ms
c. $T_{CLE1}$= 11.41 ms
d. $T_{ME1}$= 6.8 ms
e. $T_{CLE2}$= 10.52 ms
f. $T_{ME2}$= 8.2 ms

Please refer to the figures appended to the report.

| Test # and Label | Part(s) | Result(s) |
|---|---|---|
| **33.1.11 – Allowed Classification Permutations** | **a** | **PASS** |

**Expected Results and Procedural Comments**

Purpose: To verify whether the DUT fits a valid classification permutation.

a. The DUT should function as a type 1 or type 2 PSE as defined in Table 33-8

**Comments on Test Results**

a. The DUT was observed to function as a Type-2 PSE with 2-event physical layer classification and without data link layer classification. Its functionality matches the behavior described by Table 33-8

Please refer to the figures appended to the report.

| Test # and Label | Part(s) | Result(s) |
|---|---|---|
| **33.1.12 – New Detection Cycle** | **a** | **PASS** |

**Expected Results and Procedural Comments**

Purpose: To verify that if the PSE is unable to supply power within $T_{pon}$ then, it initiates and successfully completes a new detection cycle before powering on.

a. The DUT should complete a full detection cycle before applying power onto the link segment.

**Comments on Test Results**

a. The DUT was observed to successfully complete a new detection cycle before applying power onto the link segment.

| Test # and Label | Part(s) | Result(s) |
|---|---|---|
| **33.1.13 – Alternative B Backoff Cycle** | **a** | **Not Applicable** |
| | **b** | **Not Applicable** |

**Expected Results and Procedural Comments**

Purpose: To verify that if a PSE implementing Alternative B fails to detect a valid detection signature at its PI, it will wait for the appropriate period of time before beginning a new detection cycle and applies a voltage on to the PI that falls within the defined limits.

a. The DUT should not apply a voltage greater than 2.8 $V_{dc}$ to the PI.
b. The value for $T_{dbo}$ should be at least 2 sec.

**Comments on Test Results**

The DUT was observed to only power on Alternative-A. These tests only apply to devices which power on Alternative-B.

## GROUP 2: POWER FEED CHARACTERISTICS

| Test # and Label | Part(s) | Result(s) |
|---|---|---|
| **33.2.1 – Power Feed Ripple and Noise** | **a** | **PASS** |
| | **b** | **PASS** |
| | **c** | **PASS** |
| | **d** | **PASS** |

**Expected Results and Procedural Comments**

Purpose: To verify that the power feeding ripple and noise are within the conformance limits.

The peak-to-peak values of ripple and noise transmitted on the line by the DUT, in both the common mode and pair-to-pair, should not exceed:

a. 500 $mV_{pp}$ between 0-500 Hz
b. 200 $mV_{pp}$ between 500 Hz -150 kHz
c. 150 $mV_{pp}$ between 150-500 kHz
d. 100 $mV_{pp}$ between 500 kHz-1 MHz

**Comments on Test Results**

a. 53.88 $mV_{pp}$ between 0-500Hz
b. 57.38 $mV_{pp}$ between 500Hz-150kHz
c. 92.75 $mV_{pp}$ between 150-500kHz
d. 33.42 $mV_{pp}$ between 500kHz-1MHz

| Test # and Label | Part(s) | Result(s) |
|---|---|---|
| **33.2.2 – Load Regulation** | **a** | **Not Available** |
| | **b** | **PASS** |

**Expected Results and Procedural Comments**

Purpose: To verify that the PSE performs load regulation while supplying power to the PI.

a. Voltage transients should not exceed 3.5 V/µs.
b. For Type-1 PSEs, the DUT output voltage should be between 44 and 57 V for all values of $I_{Port}$.
For Type-2 PSEs, the DUT output voltage should be between 50 and 57 V for all values of $I_{Port}$.

**Comments on Test Results**

a. This test is currently under development.
b. $V_{Port}$ (max)= 52.04 V
$V_{Port}$ (min)= 51.06 V

| Test # and Label | Part(s) | Result(s) |
|---|---|---|
| **33.2.3 – Voltage Transients** | **a** | **PASS** |

**Expected Results and Procedural Comments**

Purpose: To verify that a Type-2 PSE maintains proper output voltages for transient conditions.

a. Vport should not go below 46.2 Volts for any transient between 30µs and 250µs, and Vport should not go below 50V for any transient lasting more than 250µs.

**Comments on Test Results**

a. Transients between 30µs and 250µs were observed to produce a minimum Vport of 50.9 Volts. Transients above 250µs were observed to produce a minimum Vport of 50.9 Volts.

| Test # and Label | Part(s) | Result(s) |
|---|---|---|
| **33.2.4 – Power Turn On Timing** | **a** | **PASS** |

**Expected Results and Procedural Comments**

Purpose: To verify that the DUT supplies power onto the link segment within the acceptable turn on time after it has successfully detected a PD.

a. The DUT should start supplying power within $T_{pon}$ (400ms) after detection.

**Comments on Test Results**

a. The observed value of $T_{pon}$ was measured to be 39.2 ms.

| Test # and Label | Part(s) | Result(s) |
|---|---|---|
| **33.2.5 – Apply Power** | **a** | **PASS** |
| | **b** | **PASS** |

**Expected Results and Procedural Comments**

Purpose: To verify that the PSE applies power on the same pairs as those used for detection after completing a valid detection.

a. The PSE should perform a valid detection sequence before powering the PD.
b. The PSE should supply power on the same pairs as that it performed detection for the PD.

**Comments on Test Results**

a. The DUT performed a valid detection sequence before supplying power onto the link segment.
b. The DUT applied power on the same pairs as those it detected on.

| Test # and Label | Part(s) | Result(s) |
|---|---|---|
| **33.2.6 – PSE Current Unbalance** | **a** | **Not Applicable** |
| | **b** | **PASS** |

**Expected Results and Procedural Comments**

Purpose: To verify that the current unbalance between the two conductors of the power pairs of the PSE over the current load range is within the permissible range.

a. For a Type 1 PSE, current unbalance between the two conductors per power pair should not exceed 3% of $I_{CABLE}$.
b. For a Type 2 PSE, current unbalance between the two conductors per power pair should not exceed 3% of $I_{PEAK}$.

**Comments on Test Results**

a. This test is not applicable to Type 2 PSEs.
b. The DUT was observed to have a current unbalance less than 1.65% of $I_{PEAK}$.

## GROUP 3: ERROR DETECTION AND POWER REMOVAL

| Test # and Label | Part(s) | Result(s) |
|---|---|---|
| **33.3.1 – Overload Current Detection Range** | **a** | **PASS** |
| **Expected Results and Procedural Comments** | | |
| Purpose: To verify that $I_{CUT}$ is within the specified limits.<br>a. $I_{CUT}$ should be between $P_{CLASS}/V_{PORT}$ and $I_{LIM}$. | | |
| **Comments on Test Results** | | |
| a. $I_{CUT}$ = 632.884 mA | | |

| Test # and Label | Part(s) | Result(s) |
|---|---|---|
| **33.3.2 – Overload Time Limits** | **a** | **PASS** |
| **Expected Results and Procedural Comments** | | |
| Purpose: To verify that $T_{CUT}$ is within the specified limits.<br>a. The overload time limit ($T_{CUT}$) should be between 50ms and 75ms (inclusive). | | |
| **Comments on Test Results** | | |
| a. $T_{CUT}$ = 60.89 ms | | |

| Test # and Label | Part(s) | Result(s) |
|---|---|---|
| **33.3.3 – Output Current at Short Circuit Condition** | **a** | **PASS** |
| | **b** | **PASS** |

**Expected Results and Procedural Comments**

Purpose: To verify that the PSE will start removing power from the PI within $T_{LIM}$ when it detects a short circuit condition.

a. The DUT should limit $I_{PORT}$ when current draw exceeds the PSE upperbound template
b. The DUT should not remove power when below the PSE lowerbound template

**Comments on Test Results**

a. The DUT was observed to limit $I_{PORT}$ when the current draw exceeded the upperbound template.
b. The DUT was observed to continue powering the PI while current draw was below the PSE lowerbound template.

Listed below are a number of inflection points used to determine how the PSE's current draw profile fits into the PSE upperbound template.

| Attempted Current Draw | Idraw = 40A[*1] | Idraw = 1.75A[*1] | Idraw = 0.69A |
|---|---|---|---|
| Maximum Observed Current | I1 = 2.57 A | I2 = 1.38 A | I3 = 675 mA |
| Cut Time | T1 = 17 us | T2 = 8.2 ms | T3 = 61 ms |

Listed below are a number of inflection points used to determine how the PSE's current draw profile fits into the PSE lowerbound template.

| Attempted Current Draw | Idraw = 640mA | Idraw = 600mA | Idraw = 580mA |
|---|---|---|---|
| Status after 1 Second | Removed Power within the limits of Tlim | Remained Powering | Remained Powering |

Note 1: This value represents the attempted current draw. The actual current draw appeared to be limited, and was observed to be less than this amount.

Please see the appended figure for the attempted Idraw of 0.69A.

| Test # and Label | Part(s) | Result(s) |
|---|---|---|
| **33.3.4 – Output Current in Startup Mode** | **a** | **PASS** |
| | **b** | **PASS** |
| | **c** | **PASS** |
| | **d** | **PASS** |

**Expected Results and Procedural Comments**

Purpose To verify that when the PSE detects a short circuit condition it starts removing power from the PI within $T_{LIM}$ and must be done removing power within the conformant time limit.

a. For voltages from 0V to 10V, $I_{INRUSH}$ must be between 5mA and 450mA.
b. For voltages from 10V to 30V, $I_{INRUSH}$ must be between 60mA and 450mA.
c. For voltages above 30V, $I_{INRUSH}$ must be between 400mA and 450mA.
d. The short circuit time limit ($T_{INRUSH}$) should be between 50ms and 75ms.

All ranges are inclusive.

**Comments on Test Results**

a. Observed $I_{INRUSH}$ (0 to 10V) = 72.95 mA
b. Observed $I_{INRUSH}$ (10V to 30V) = 361.30 mA
c. Observed $I_{INRUSH}$ (30V and above) = 412.45 mA
d. Observed $T_{INRUSH}$ = 60.16 ms

| Test # and Label | Part(s) | Result(s) |
|---|---|---|
| **33.3.5 – Error Delay Timing** | **a** | **PASS** |
| | **b** | **PASS** |

**Expected Results and Procedural Comments**

Purpose: To verify that the PSE waits for at least the minimum conformant time before attempting subsequent detection after it removes power due to detection of error condition.

a. The DUT should wait for at least 750ms after detecting a short circuit condition and removing power before resuming detection
b. The DUT should wait for at least 750ms after detecting an overload condition and removing power before resuming detection

**Comments on Test Results**

a. The DUT was observed to wait 1.10 s after a short circuit event before resuming signature detection.
b. The DUT was observed to wait 1.03 s after an overload event before resuming signature detection.

| Test # and Label | Part(s) | Result(s) |
|---|---|---|
| **33.3.6 – Range of $T_{MPDO}$ Timer** | **a** | **PASS** |
| | **b** | **Not Applicable** |

**Expected Results and Procedural Comments**

Purpose: To verify that PSE correctly monitors the PD Maintain Power Signature

a. *DC disconnect:* 300ms $\leq T_{MPDO} \leq$ 400ms
b. *AC disconnect:* 300ms $\leq T_{MPDO} \leq$ 400ms

**Comments on Test Results**

a. Observed DC disconnect: 352.00 ms $\leq T_{MPDO} \leq$ 356.00 ms
b. This test does not apply to devices that do not support AC disconnect

| Test # and Label | Part(s) | Result(s) |
|---|---|---|
| **33.3.7 - PD MPS Dropout Current Limits ($I_{MIN}$ measurement)** | **a** | **PASS with comments** |
| | **b** | **PASS with comments** |

**Expected Results and Procedural Comments**

Purpose: To verify that PSE correctly monitors the PD Maintain Power Signature for DC disconnect.

a. The DUT may remove power if the current drawn is between 5 mA and 10 mA ($I_{MIN2\ (max)}$) for 400 ms.
b. The DUT must remove power if the current drawn is less than 5 mA ($I_{MIN1\ (max)}$) for 400 ms.

**Comments on Test Results**

a. Observed 7.30 mA $\leq I_{MIN2\ (max)} \leq$ 7.40 mA
b. The DUT was observed to remove power when current draw is less than 5mA.

Note: The LED jumper for port 1 was removed for the duration of testing, as it was suspected to present a parallel load and interfere with the DUT's ability to accurately measure the current draw at the MDI.

| Test # and Label | Part(s) | Result(s) |
|---|---|---|
| **33.3.8 – PD MPS Time for Validity** | **a** | **PASS** |

**Expected Results and Procedural Comments**

Purpose: To verify that the PSE waits for at least the minimum MPS validity time when it monitors the DC MPS component.

a. The DUT should not remove power from a PD that provides a valid DC MPS signature for at least $T_{MPS}$ every $T_{MPS}+T_{MPDO}$.

**Comments on Test Results**

a. The DUT was observed to remain powering when a valid DC MPS signature was presented for at least $T_{MPS}$ every $T_{MPS}+T_{MPDO}$.

| Test # and Label | Part(s) | Result(s) |
|---|---|---|
| **33.3.9 – AC MPS Signal Parameters** | **a** | **Not Applicable** |
| | **b** | **Not Applicable** |
| | **c** | **Not Applicable** |
| | **d** | **Not Applicable** |

**Expected Results and Procedural Comments**

Purpose: To verify that the PI probing AC signals fall within the conformance limits.

a. The PI probing AC voltage (V_open) should be between 1.9V to 10% of Vport ($V_{pp}$).
b. The AC probing signal frequency, Fp, should not be greater than 500 Hz.
c. The AC probing signal slew rate should not be greater than 0.1V/µs.
d. The measured $V_{Port}$ (Vp) should not exceed 60V.

**Comments on Test Results**

This test does not apply to devices that do not support AC MPS.

| Test # and Label | Part(s) | Result(s) |
|---|---|---|
| **33.3.10 – AC MPS Signature** | **a** | **Not Applicable** |
| | **b** | **Not Applicable** |

**Expected Results and Procedural Comments**

Purpose: To verify that the PSE that implements AC MPS component correctly monitors the PD Maintain Power Signature.

a. The DUT should supply power to the PD for signature impedance less than 27KΩ.
b. The measured impedance should be between 27KΩ and 1980KΩ (inclusive).

**Comments on Test Results**

This test does not apply to devices that do not support AC MPS.

| Test # and Label | Part(s) | Result(s) |
|---|---|---|
| **33.3.11 – Turn Off Time Limits** | **a** | **PASS** |

**Expected Results and Procedural Comments**

Purpose: To verify that the PSE disconnects power within $T_{Off}$ through a test resistor.

a. The DUT should remove power in ≤ 500ms when the PI is connected to a test resistor of 320kΩ.

**Comments on Test Results**

a. The measured value of $T_{Off}$ was observed to be 93.48 ms.

## GROUP 4: PSE TRANSMITTER AND RECEIVER CHARACTERISTICS

| Test # and Label | Part(s) | Result(s) |
|---|---|---|
| **33.4.1 – Midspan PSE Return Loss** | **a** | **Not Available** |
| **Expected Results and Procedural Comments** | | |
| Purpose: To verify that the return loss of a Midspan PSE is greater than the minimum conformant value.<br>a. The DUT's return loss should be greater than 23dB from 1 to 20MHz and greater than 14dB from 20MHz to 100MHz. | | |
| **Comments on Test Results** | | |
| This is currently under development. | | |

| Test # and Label | Part(s) | Result(s) |
|---|---|---|
| **33.4.2 – Midspan PSE Insertion Loss** | **a** | **Not Available** |
| **Expected Results and Procedural Comments** | | |
| Purpose: To verify that the insertion loss of a Midspan PSE is no greater than the maximum conformant value.<br>a. The DUT's insertion loss should be no greater than the limit described by equation 33-6 and the maximum conformant value of 0.1dB. | | |
| **Comments on Test Results** | | |
| This is currently under development. | | |

| Test # and Label | Part(s) | Result(s) |
|---|---|---|
| **33.4.3 – Midspan PSE NEXT Loss** | **a** | **Not Available** |

**Expected Results and Procedural Comments**

Purpose: To verify that the NEXT between the transmit and receive pairs of the DUT is within conformance limits.

a. The DUT's NEXT loss should be no greater than the limit described by equation 33-5 and the minimum conformant value of 65 dB.

**Comments on Test Results**

This is currently under development.

| Test # and Label | Part(s) | Result(s) |
|---|---|---|
| **33.4.4 – PSE Impedance Balance** | **a** | **Not Applicable** |

**Expected Results and Procedural Comments**

Purpose: To verify that the common-mode to differential-mode impedance balance of the transmit and receive pairs of the PI is greater than the specified limits.

a. The common-mode to differential-mode impedance balance for a 100Mb/s transmitter and receiver should exceed $34-19.2\log_{10}(f/50)$ dB (where f is the frequency in MHz) over the frequency range of 1.0 MHz to 100 MHz

**Comments on Test Results**

This test does not apply to devices without a PHY.

| Test # and Label | Part(s) | Result(s) |
|---|---|---|
| **33.4.5 – PSE Common Mode Output Voltage** | **a** | **Not Applicable** |

**Expected Results and Procedural Comments**

Purpose: To verify that the common mode AC output voltage at the PI is below the conformant limits.

a. The magnitude of the common-mode AC output voltage, *E*cm_out, should not exceed 50 mV peak when operating at 10 Mb/s, and 50 mV peak-to-peak when operating at 100 Mb/s or greater.

**Comments on Test Results**

This test does not apply to devices without a PHY.

## Annex A: Figures

Attached are the figures illustrating the measurements made during testing. These were captured either with the real time DSO or the Vector Network Analyzer and post processed using custom Matlab scripts.

**Figure 1: Open Circuit Voltage ($V_{OC}$)**

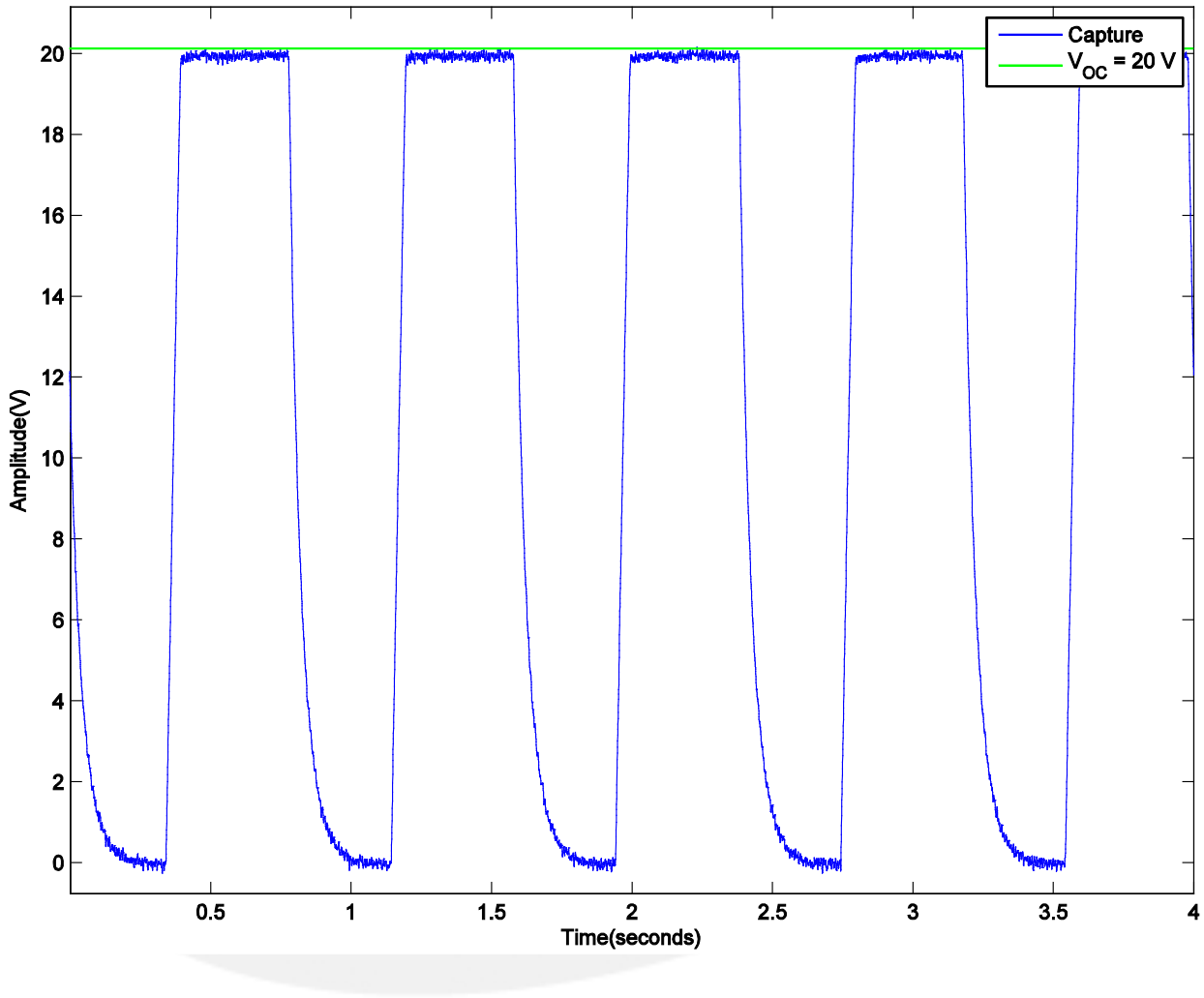


**Figure 2: Detection Pulse Identification**

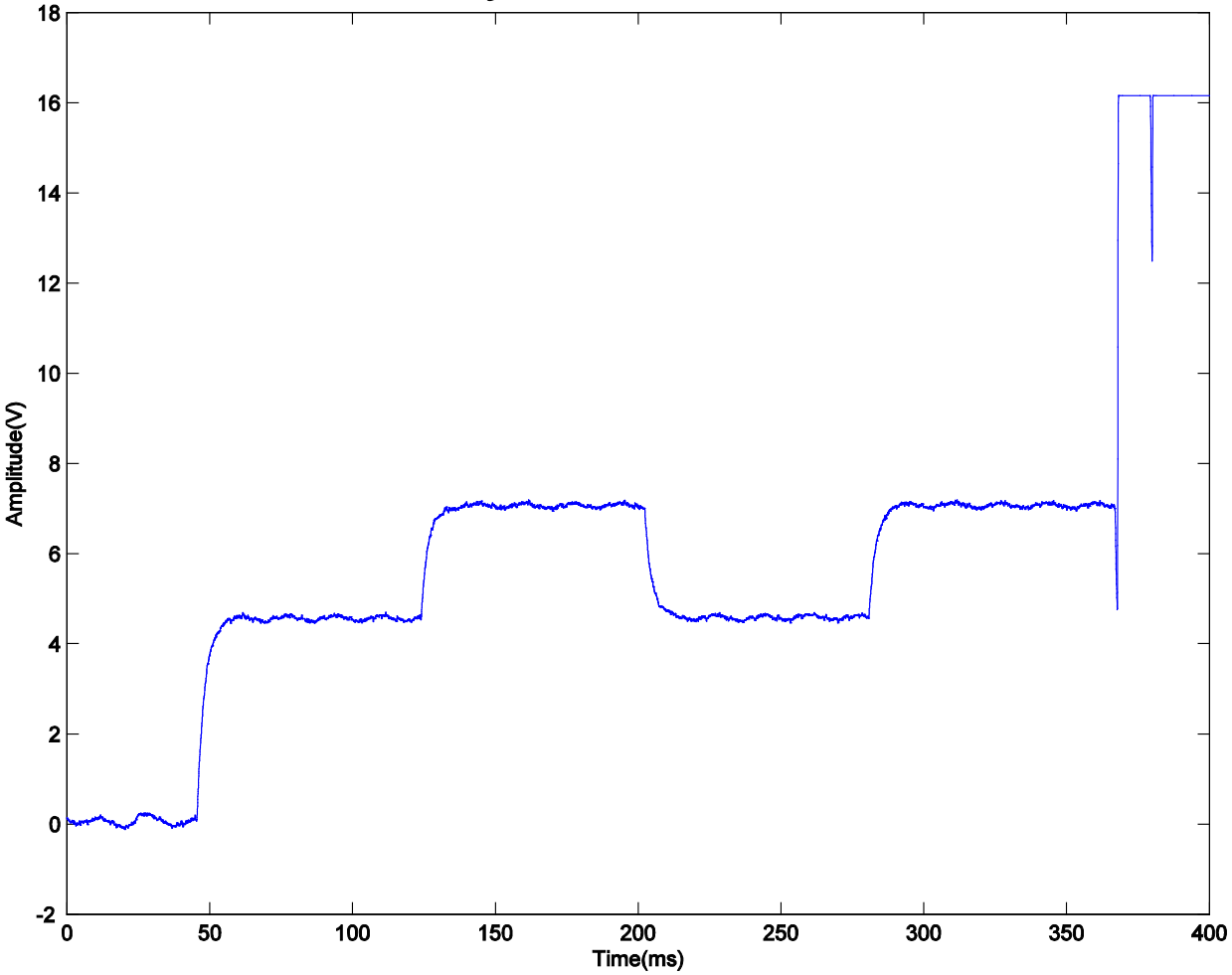


**Figure 3: Short Circuit Output Current ($I_{SC}$)**

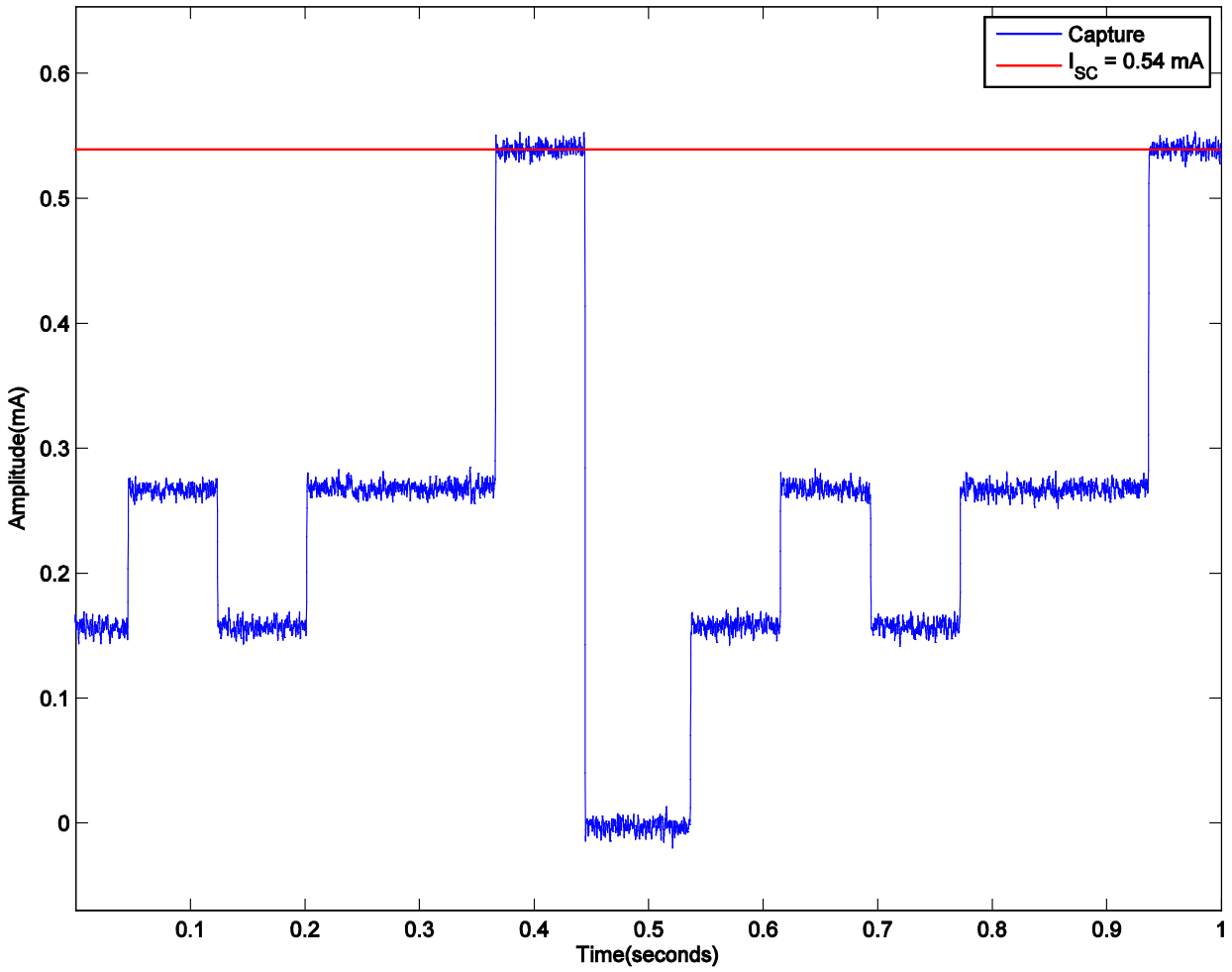


Figure 4: 1-Event Classification Pulse

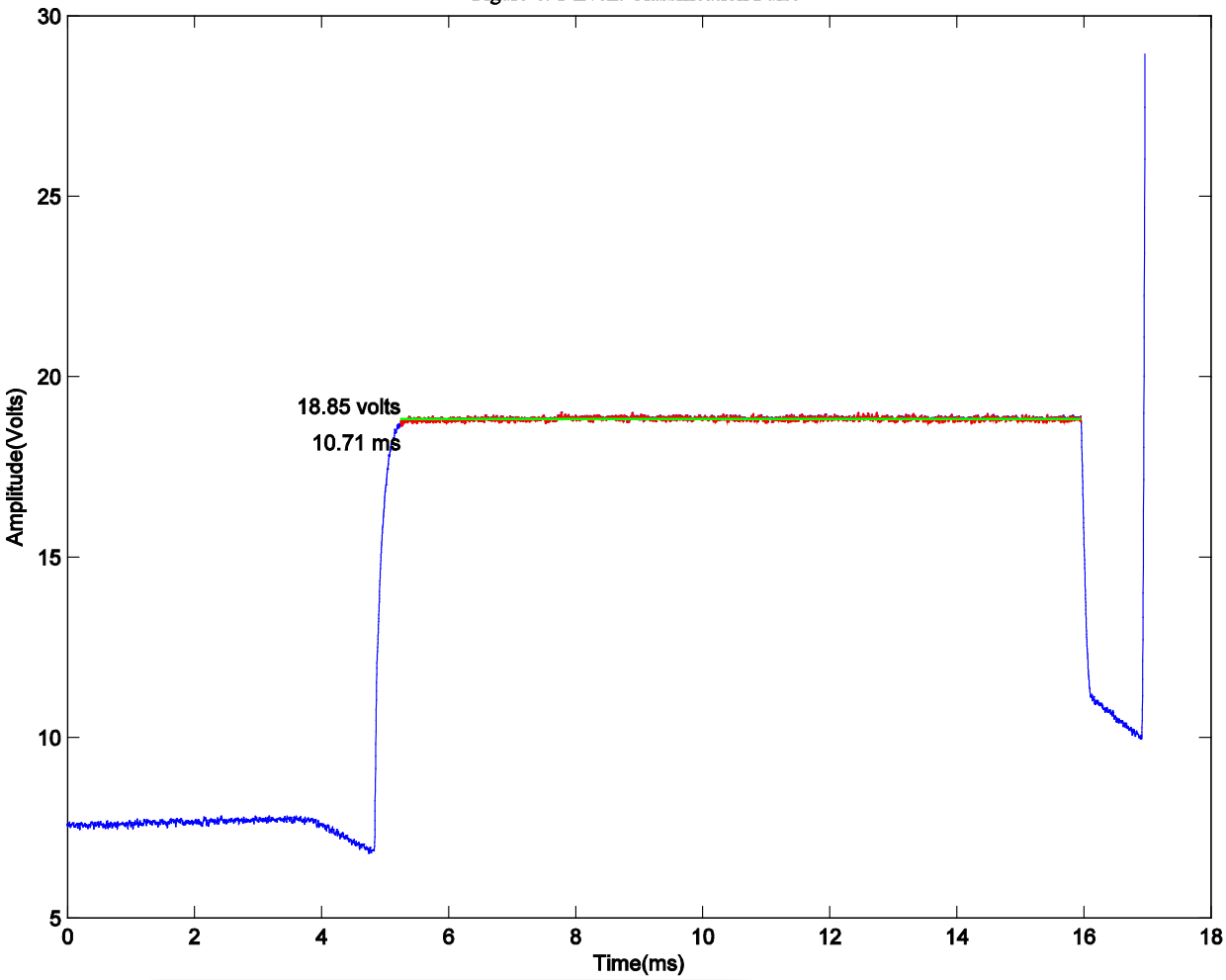


**Figure 5: 2-Event Classification**

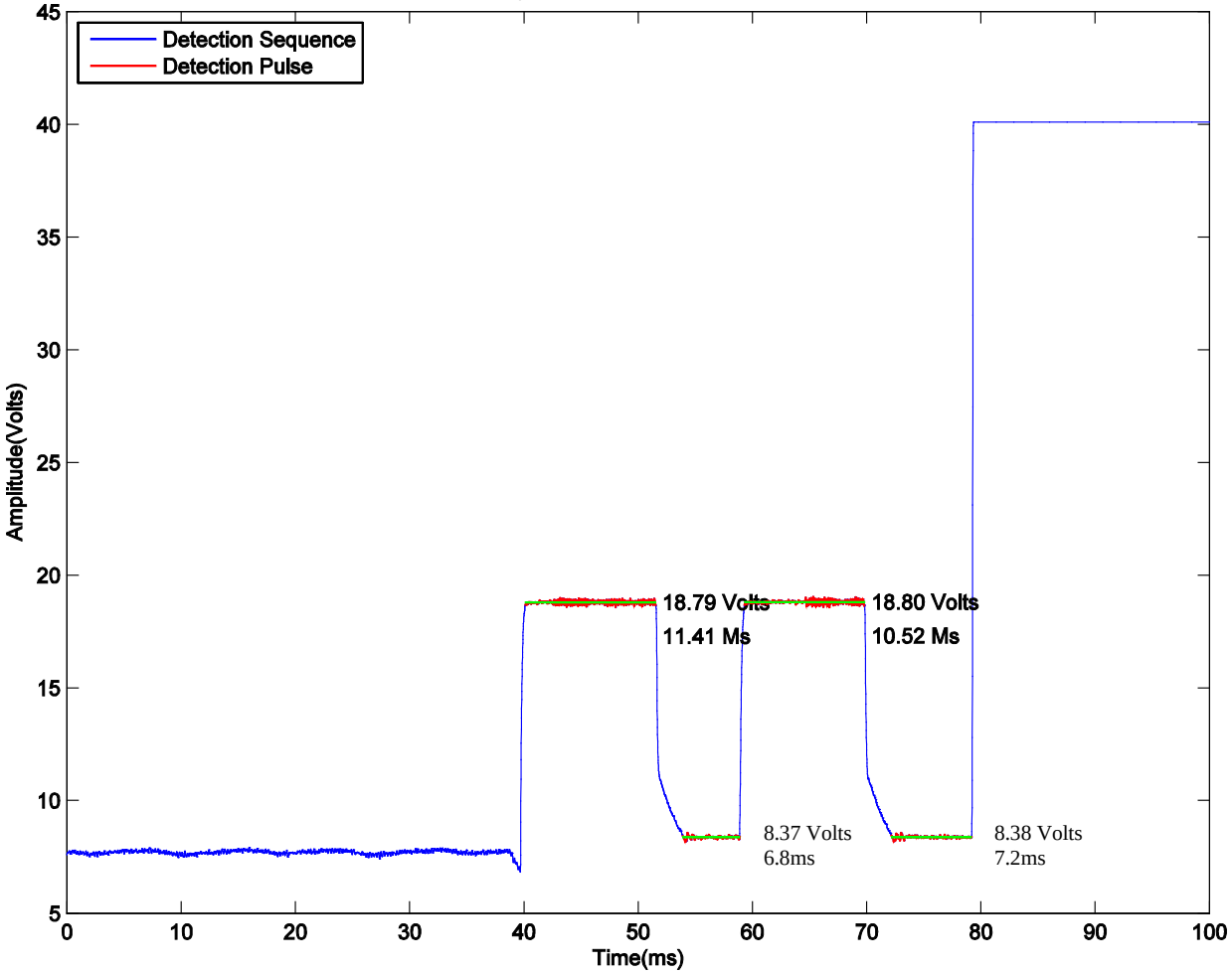


Figure 6: Class Event Current Limit ($I_{CLASS-LIM}$)

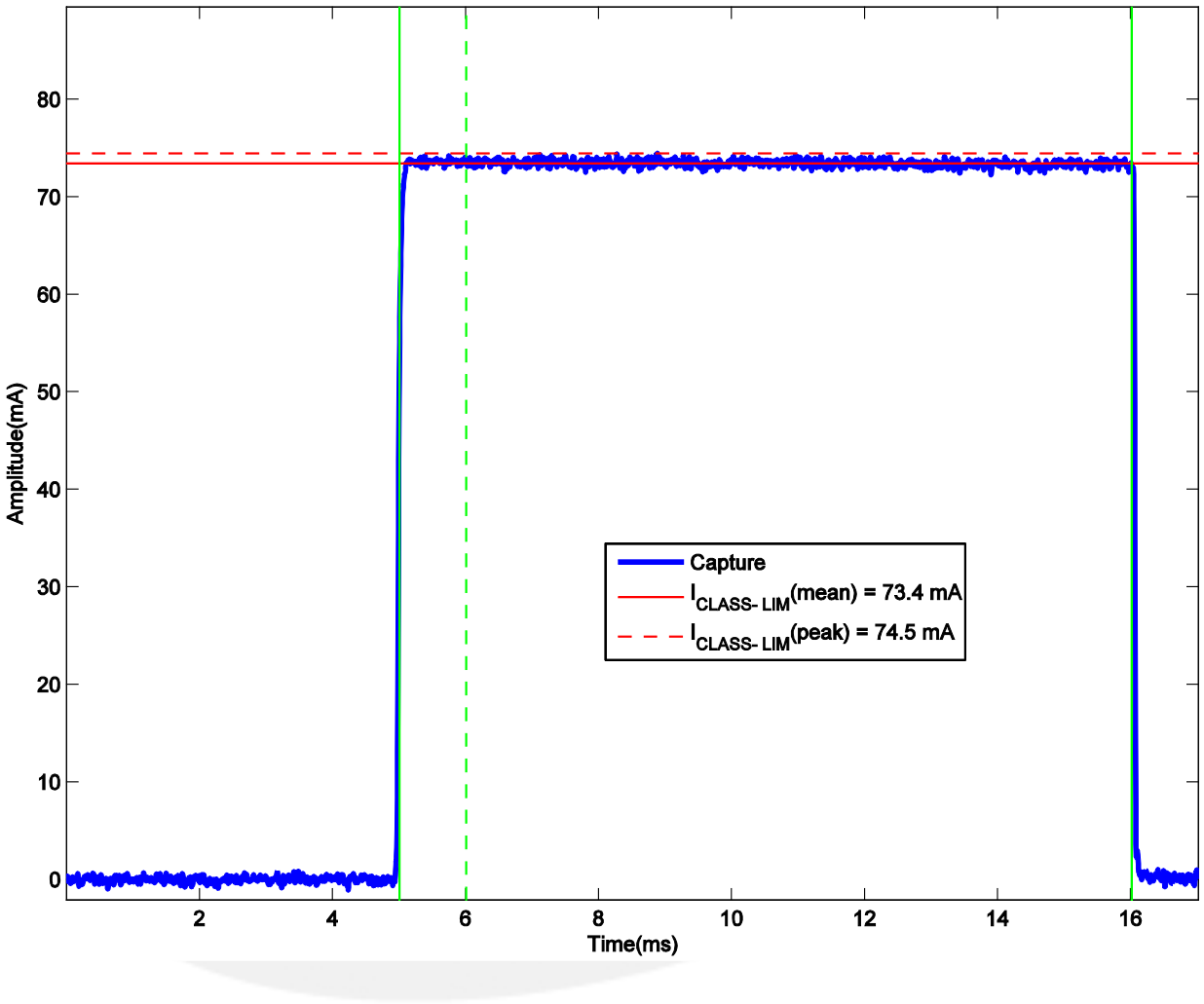


**Figure 7: $T_{PON}$**

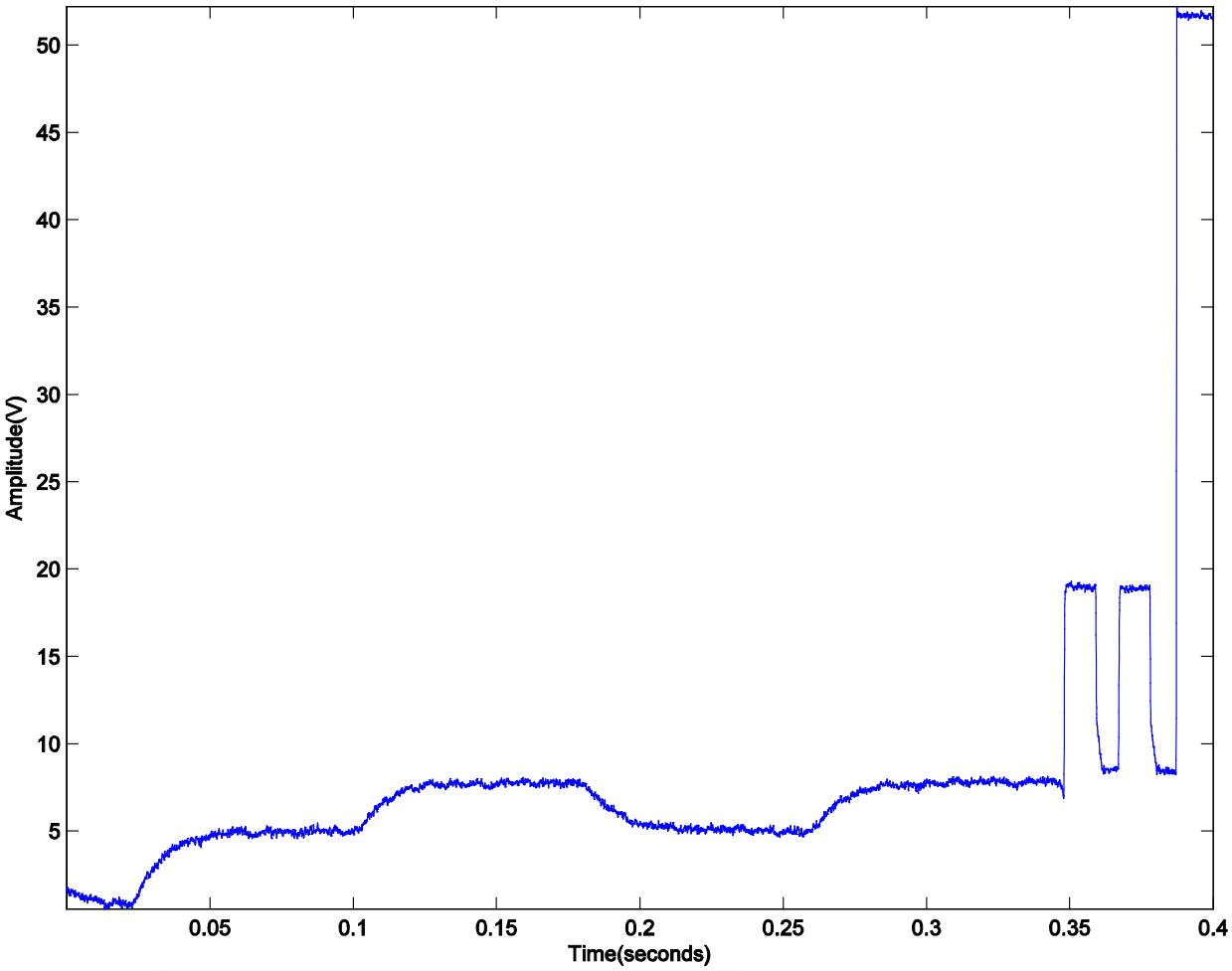


**Figure 8:Overload Error Delay Timing ($T_{ED}$(overload))**

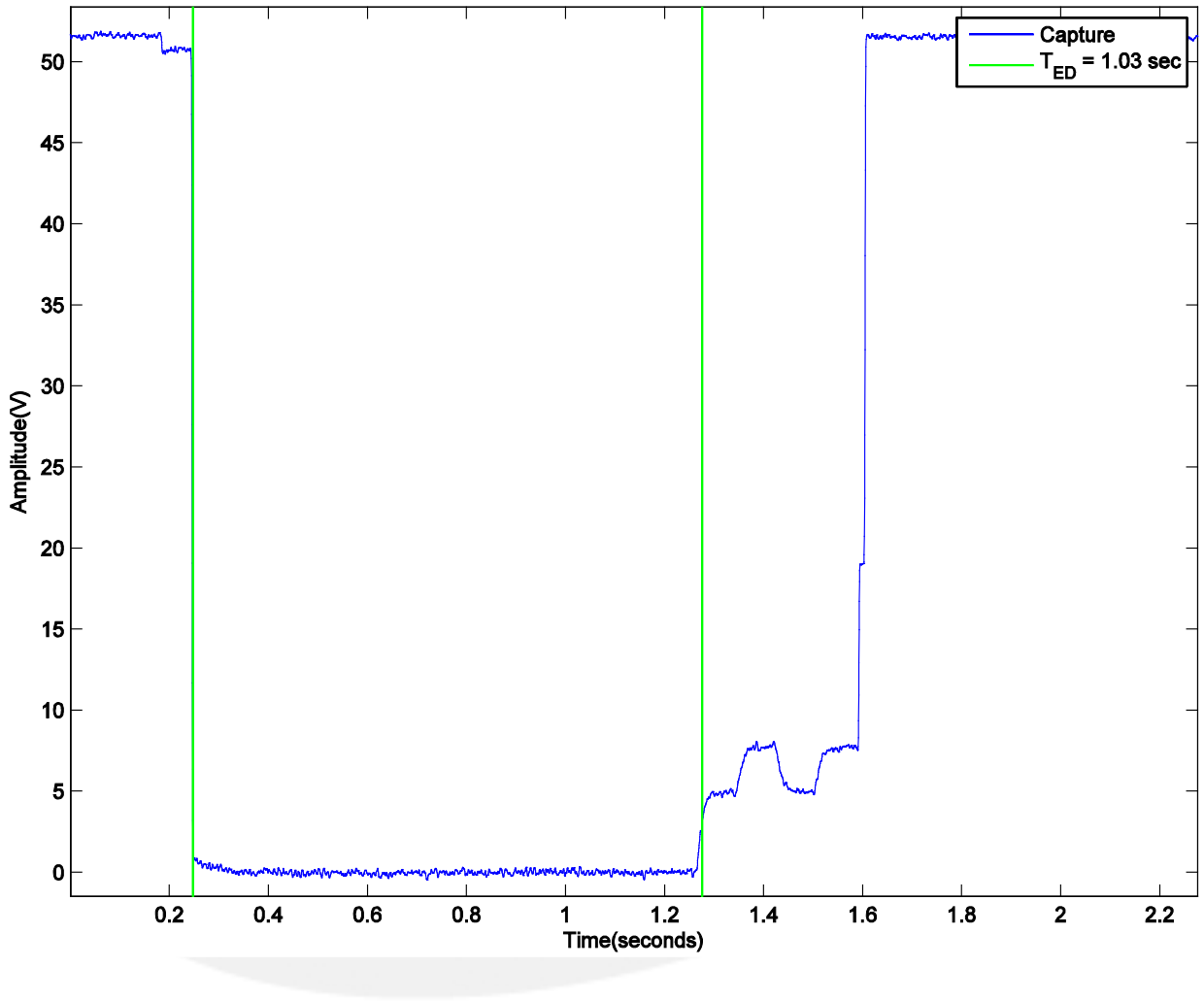


**Figure 9: Short Circuit Error Delay Timing ($T_{ED}$(short))**

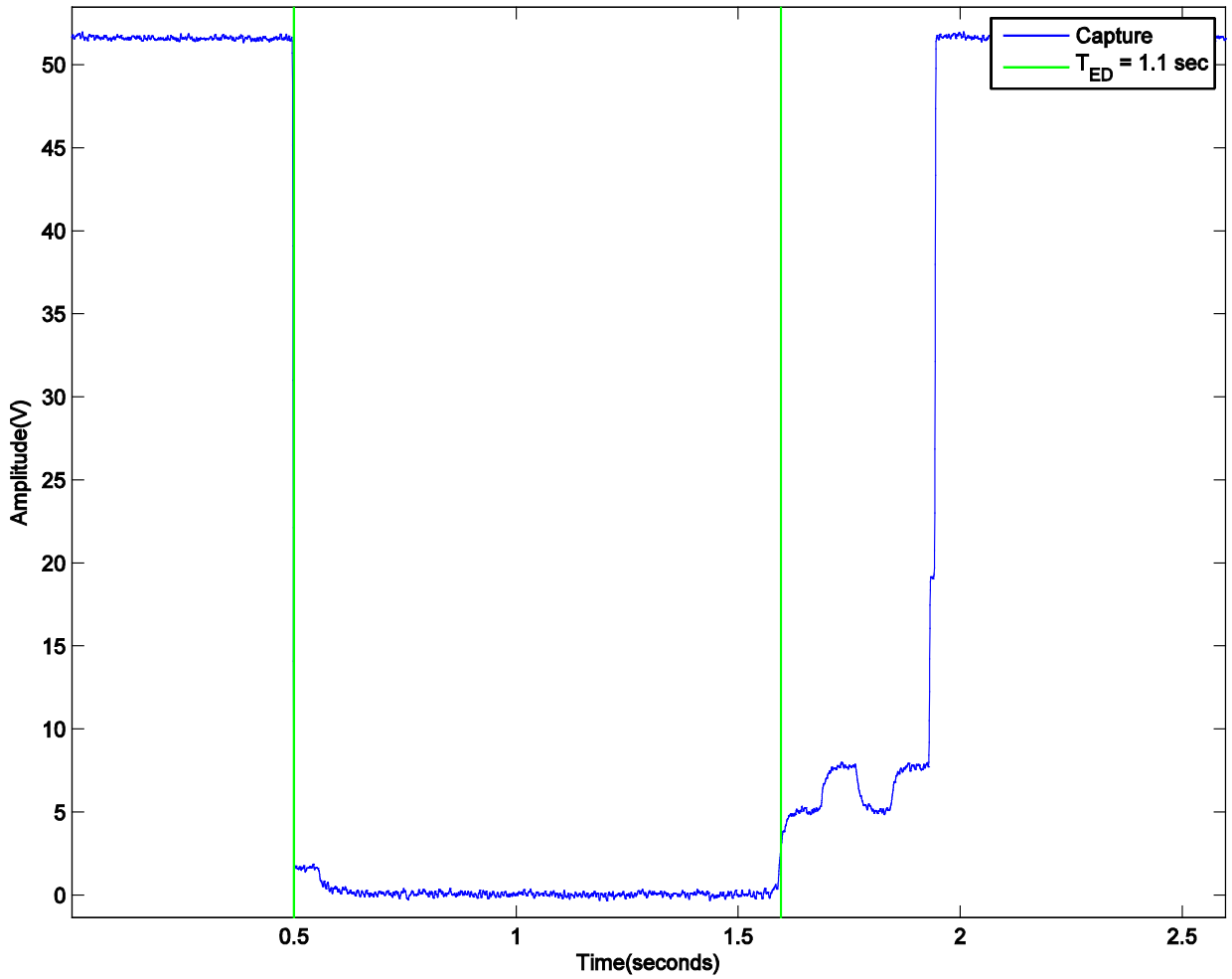


**Figure 10: Overload Current ($I_{CUT}$)**

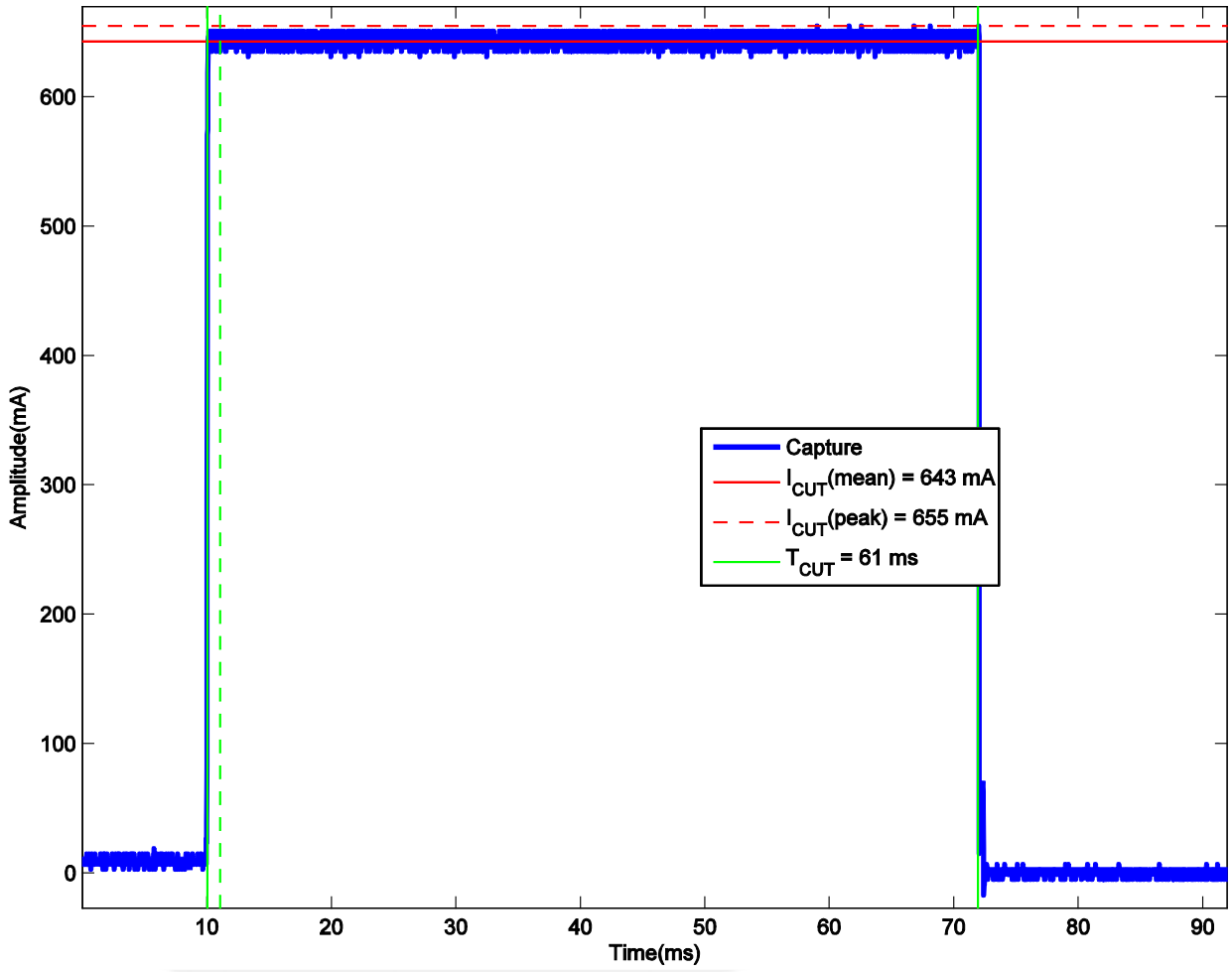


Figure 11: Output Current at Short Circuit ($I_{LIM}$)

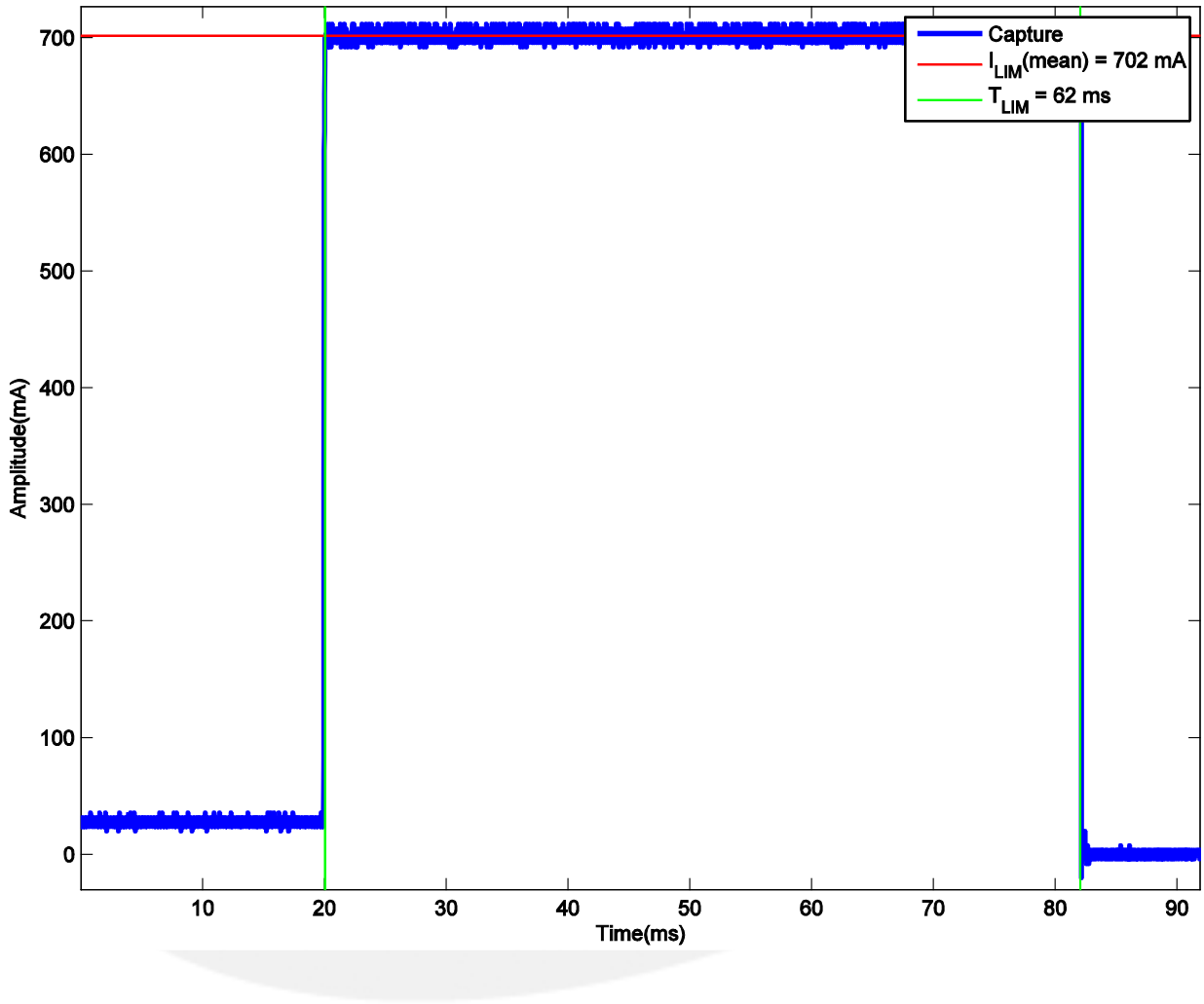


Figure 12:Output Current in Startup Mode - $I_{INRUSH}$(0-10V)

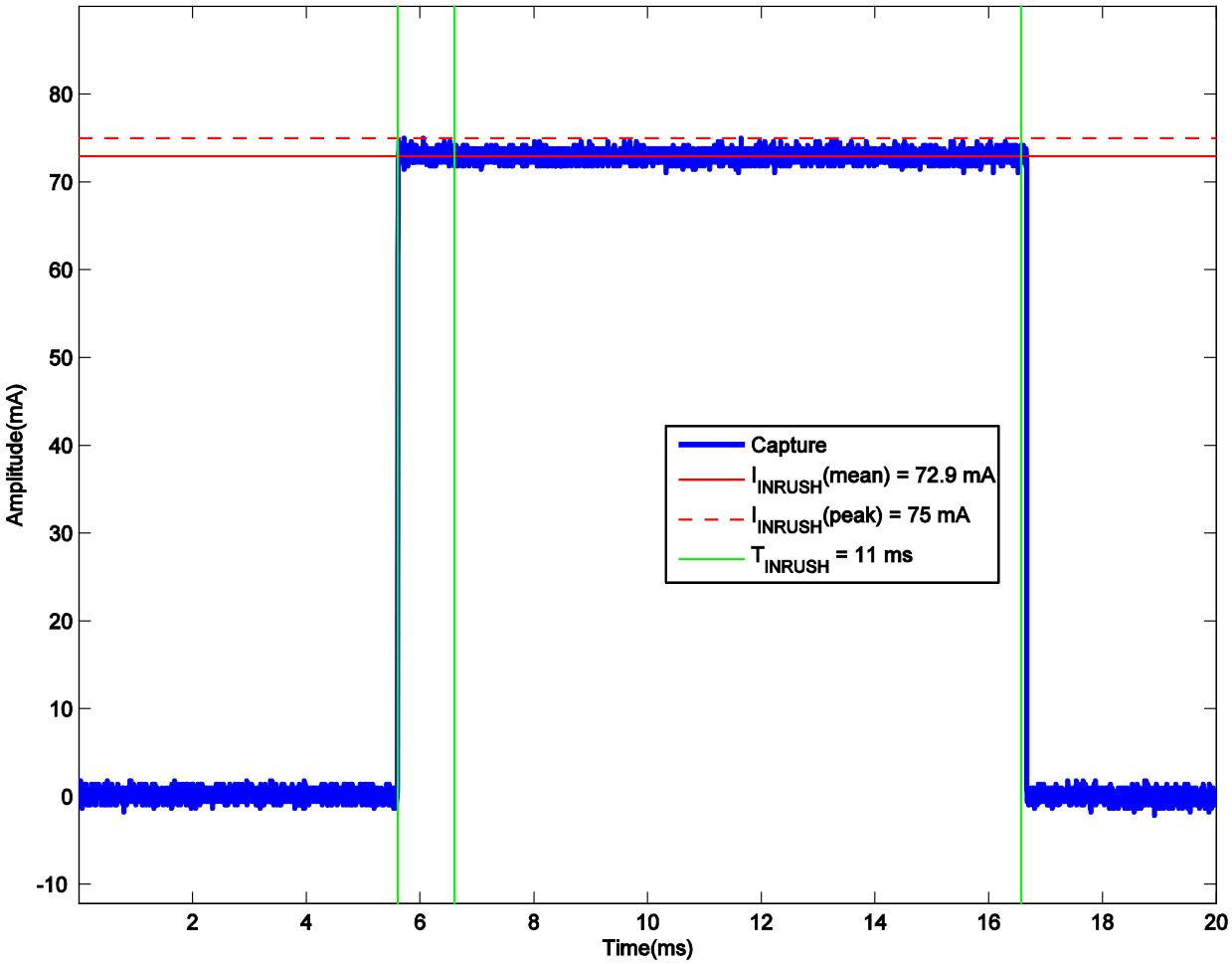


Figure 13:Output Current in Startup Mode - $I_{INRUSH}$(10V-30V)

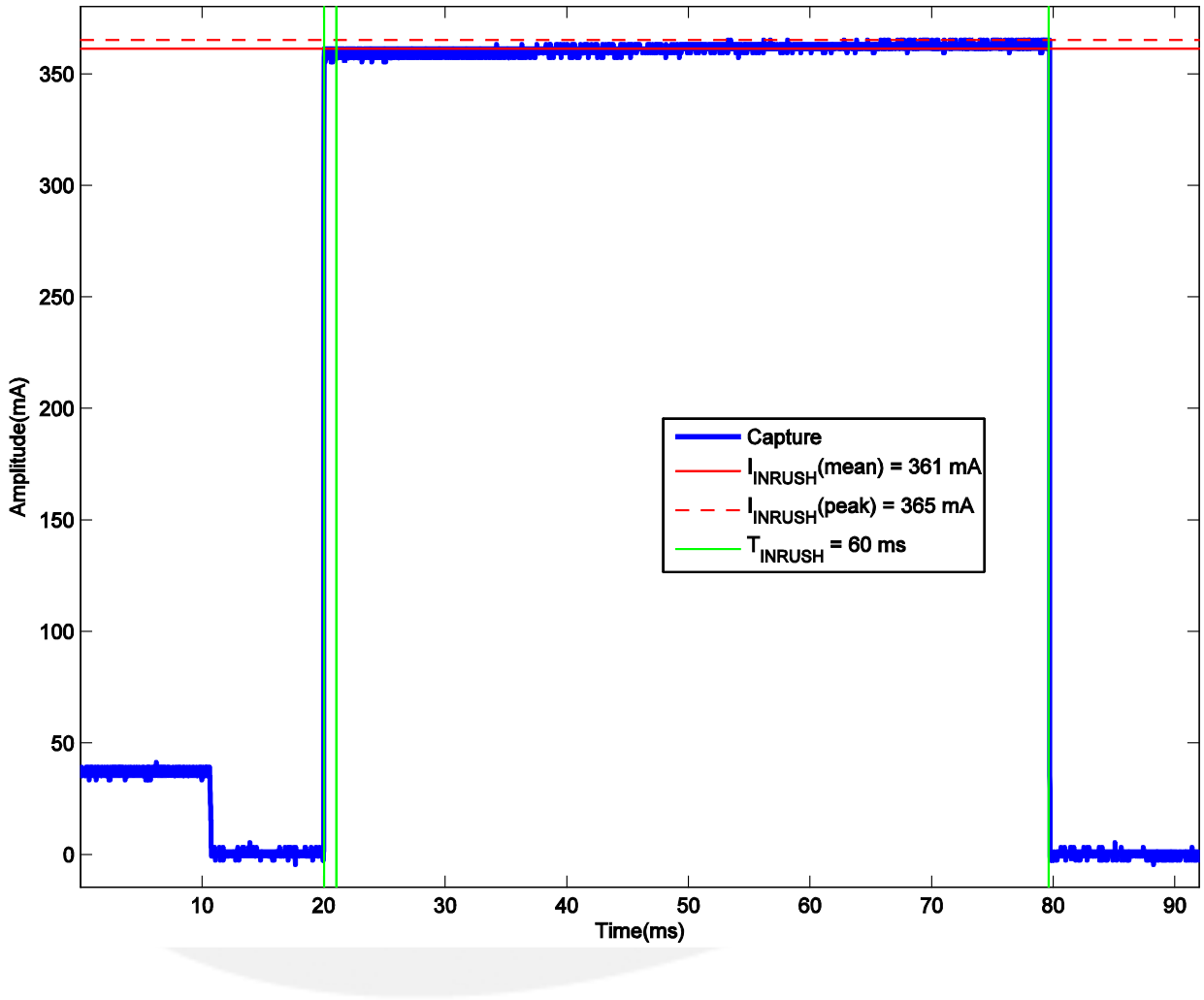
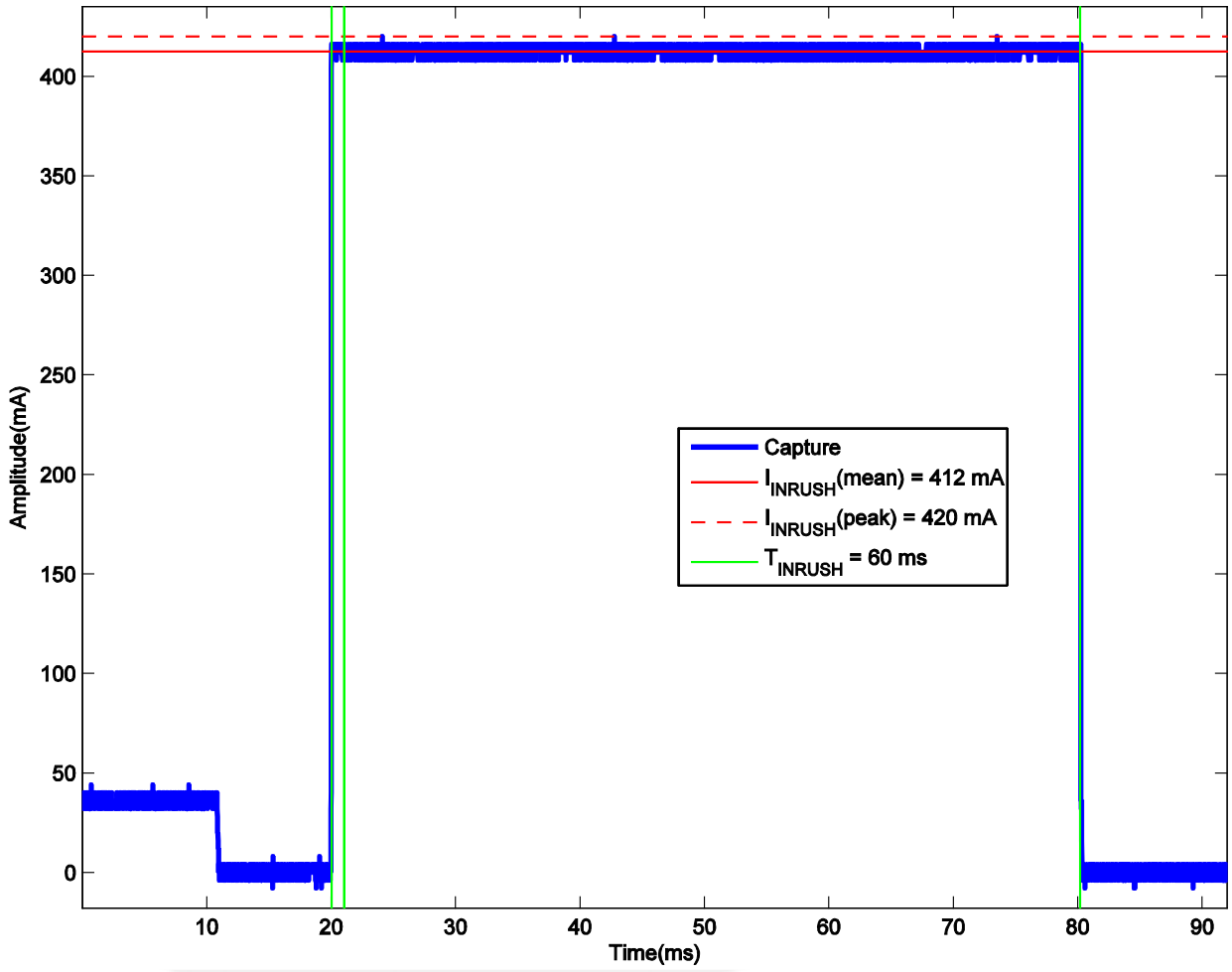


Figure 14:Output Current in Startup Mode - $I_{INRUSH}$(30V and above)



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