Application Report
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High Side P-channel Charge FET with the bq779x5 Battery Protector

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ABSTRACT

The bq77905 and bq77915 provide low side protection switching with N-channel MOSFETs, but sometimes a high side charge path is desired. This document provides examples of P-channel high side FET drive for charge current control. Circuit and test examples to address common concerns with high side P-channel FET implementations are described to help the designer with implementing a successful high side P-channel charge FET design.

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1 Introduction

The bq77905 and bq77915 protectors support low side N-channel FETs. The FETs are typically in series so that charge and discharge current pass through both FETs. Some systems will have significantly different charge and discharge current requirements. Separate charge and discharge paths allow a smaller charge FET at a lower cost, or a single charge FET while multiple discharge FETs are used. While separate paths for charge and discharge can be provided by low side switching such as in *bq77905 Separate Current Paths*, sometimes the system design will require the low current charge path on the high side.

The bq77915 includes a hibernate feature not included in the bq77905 which may add a terminal to the battery but is easily referenced to the battery positive. A basic diagram of the bq77915 with typical protection FET configuration is shown in Figure 1.

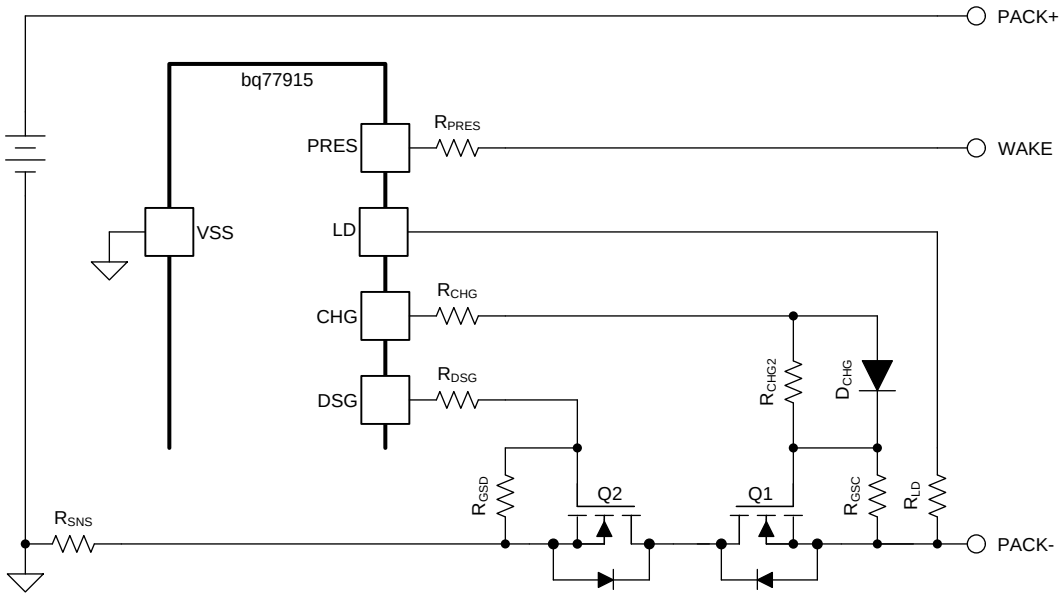

Figure 1. Typical bq77915 FET Configuration

2 Basic Circuit

The CHG pin of the bq77905 and bq77915 can drop below VSS, but is not driven below VSS in normal operation. The CHG pin can be used to control a N-channel signal FET to control a high-side P-channel power FET as shown in Figure 2. R_{CHG} may be retained to slow the switching of Q3. R_{CGS} keeps Q3 off when the bq77915 is in hibernate mode and is typically large to reduce quiescent current. R_{GSC} turns off the charge FET Q1 and will typically be 1 MΩ, but may be selected based on the Q1 gate characteristics. R_{GPD} and R_{GSC} provide a voltage divider for the pack voltage to provide a gate voltage. R_{GPD} may typically match R_{GSC} to provide a 10-V gate voltage for Q1 with the battery at 20 V. The resulting bias current at 20 V is 10 µA. Some designers will include a zener across R_{GSC} to clamp any transients below the Q1 V_{GS} absolute maximum.

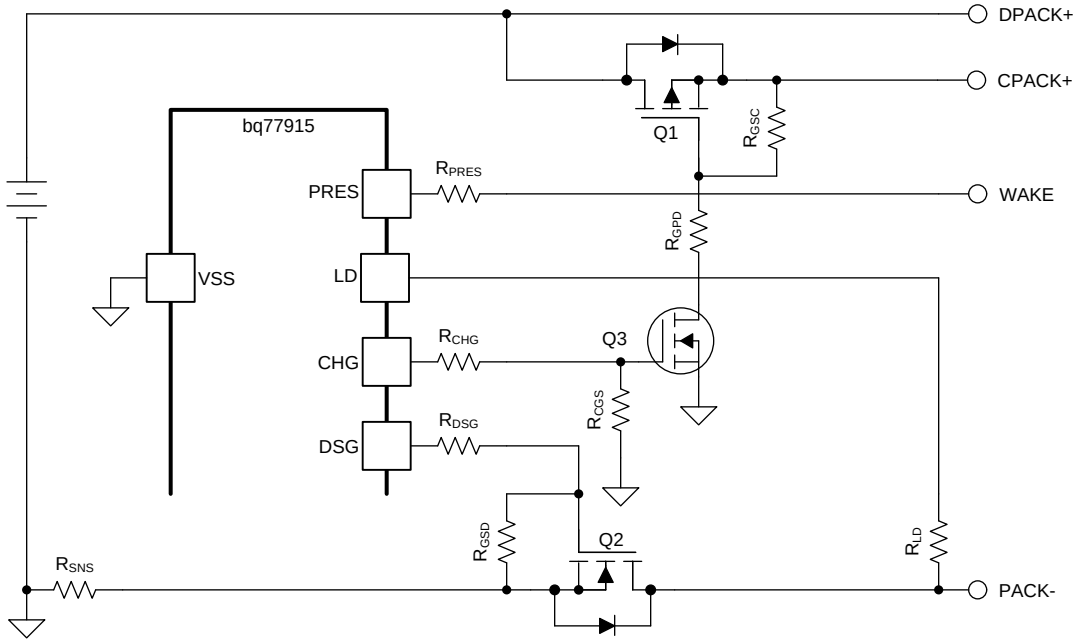

Figure 2. Basic High-side Charge FET

Figure 10 in the bq77915 data sheet shows a simple circuit to wake the part using PACK+. In Figure 3 DPACK+ provides a path to wake the battery in a system with a load. Figure 3 also shows the body diode of Q1 provides a path to wake the bq77915 when used with a charger which accesses the CPACK+ terminal.

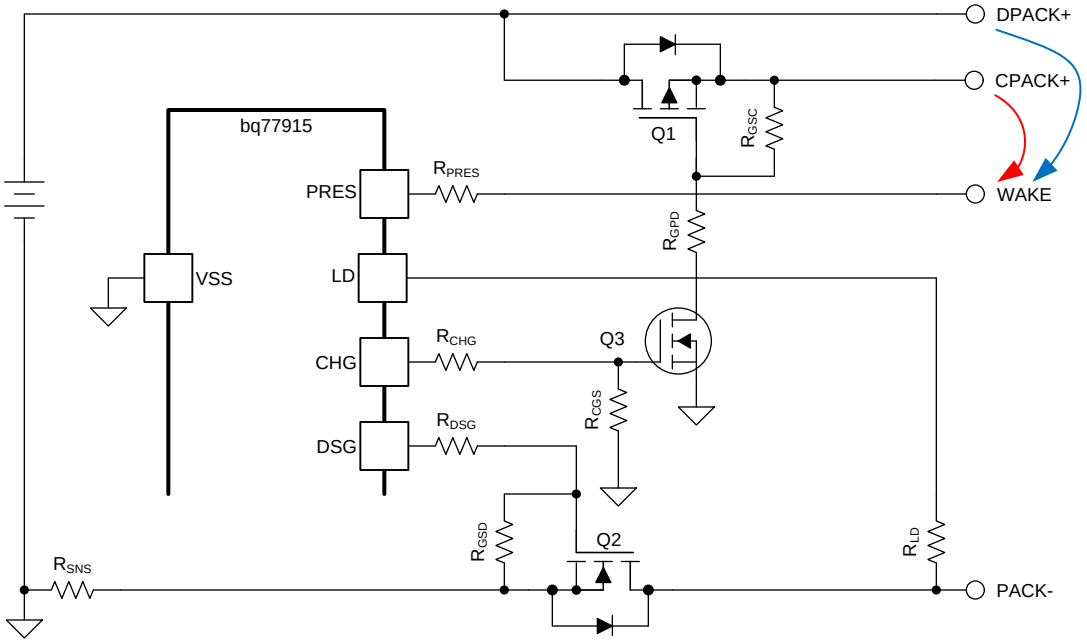

Figure 3. Wakeup Paths With P-channel

When charging, the bias current for Q1 gate comes from the charger. Figure 4 shows the Q1 body diode provides a path for the bias current for the Q1 gate to continue when the charger is removed. The Q1 body diode also allows discharge into any leakage path on the CPACK+ terminal such as might occur with an un-powered charger shown in Figure 5. The bq779x5 would protect at needed, but with a low current the battery may be discharged to a UV condition before protection. In many systems these currents will not be a concern, but needs will vary with the system design.

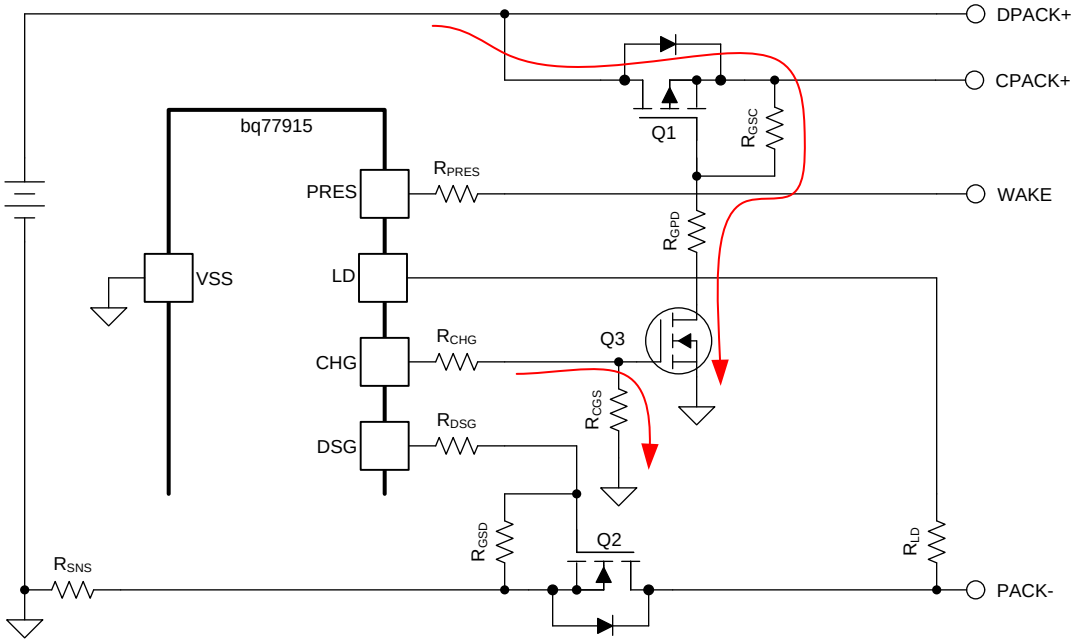

Figure 4. Quiescent Current Paths

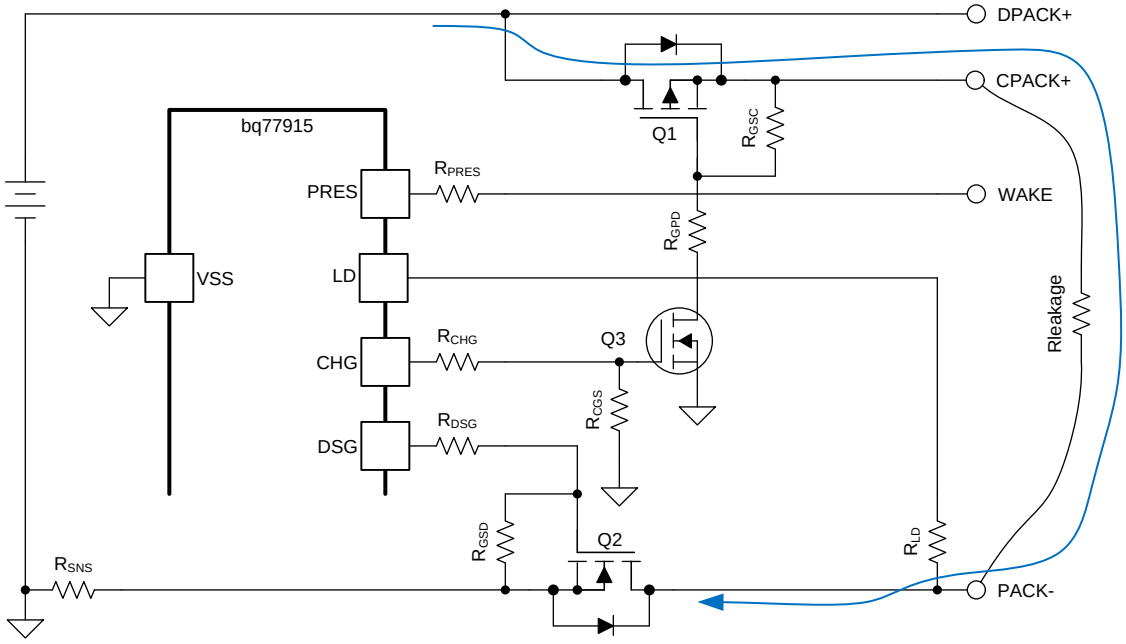

Figure 5. Leakage Into Disabled Charger

While a diode provides a loss in the charge path, some designers will prefer to include a diode to block discharge current from the charge path. When placed between the cells and the charge FET as shown in Figure 6 it will also block bias current for the Q1 gate circuit. A Schottky diode provides less loss from forward voltage but more reverse leakage. The diode also blocks current for wakeup, so a charger connecting at PACK- and CPACK+ will need to provide the wake voltage from its own source as shown in Figure 7.

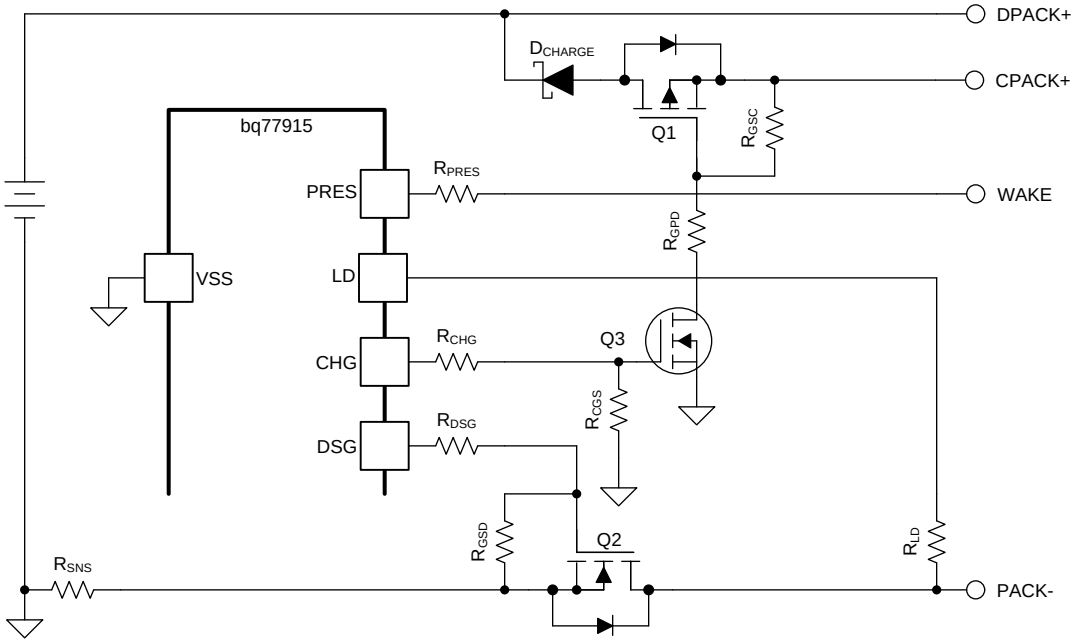

Figure 6. High-side Charge With Diode

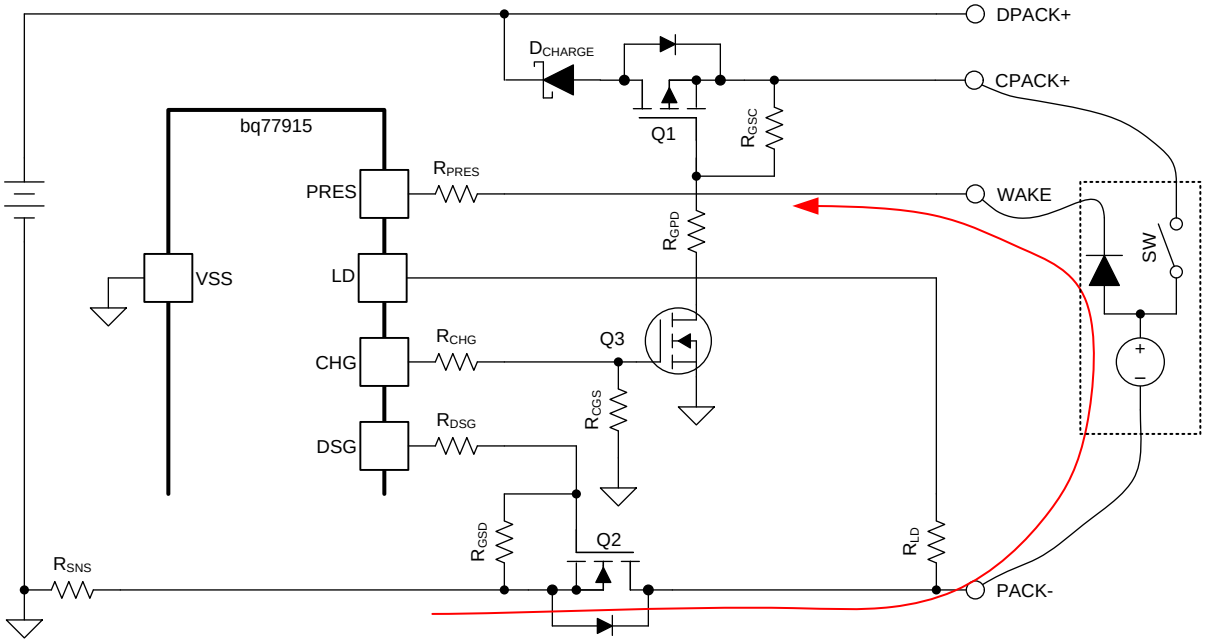

Figure 7. Wakeup From Charger Voltage

A Figure 6 circuit was built using the resistor values shown in Table 1. Figure 8 shows an example turn off. Notice the delay and slow transition of the current. The switching speed will depend on the resistors and FET used, and while it is slow may be suitable for the system. With turn on shown in Figure 9 the delay is shorter. The current has a transient as the charger supply comes into regulation.

Table 1. Resistive Test Circuit Values

Reference Designator	Value
R_{CHG}	4.7k Ω
R_{CGS}	10M Ω
R_{CPD}	1M Ω
R_{GSC}	1M Ω

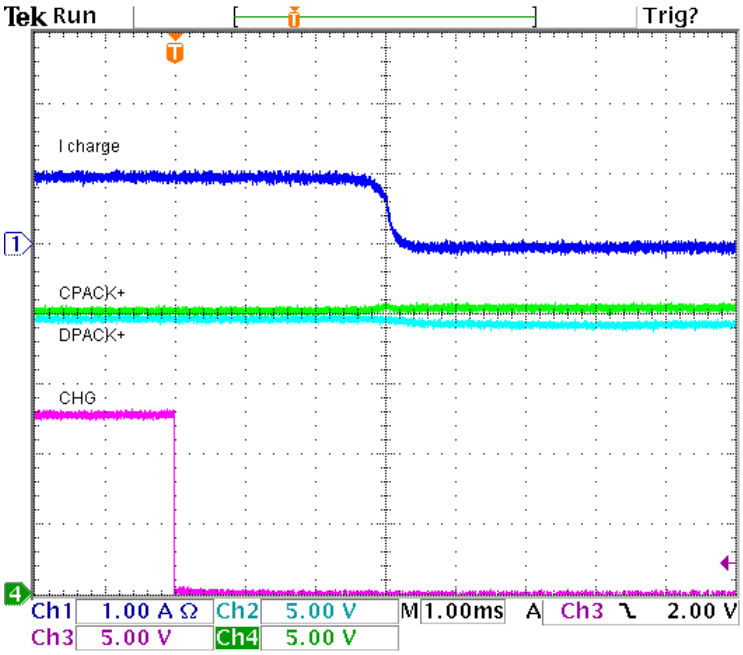

Figure 8. P-channel Resistive Circuit Turn Off

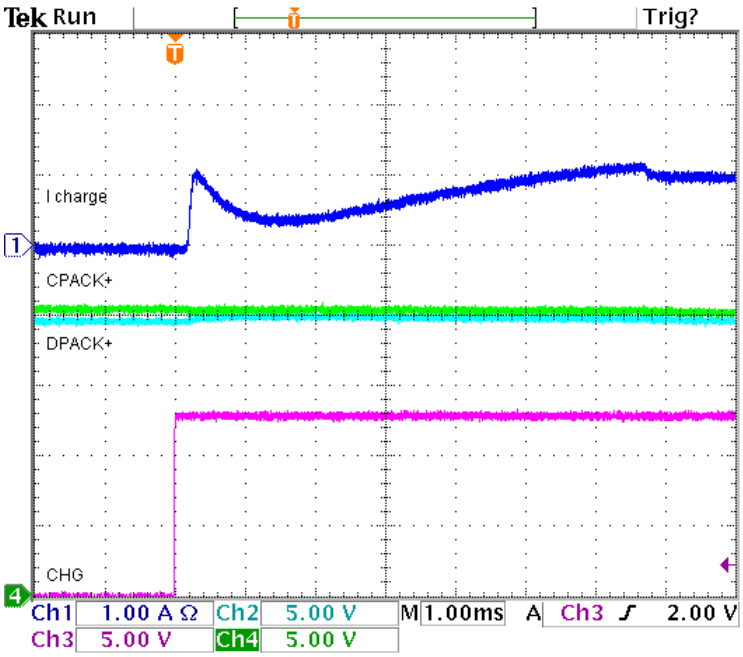

Figure 9. P-channel Resistive Circuit Turn On

Without the charger attached, leakage through the Schottky diode is apparent. Figure 10 shows the bq77915 transition into hibernate mode. Before hibernation both the bias circuit for Q1 and the scope probe pull down CPACK+ to a low voltage. When the CHG pin turns off only the 10 MΩ scope probe pulls down CPACK+. After hibernation CPACK+ transitions to about 8 V indicating a leakage of about 800 nA in this condition.

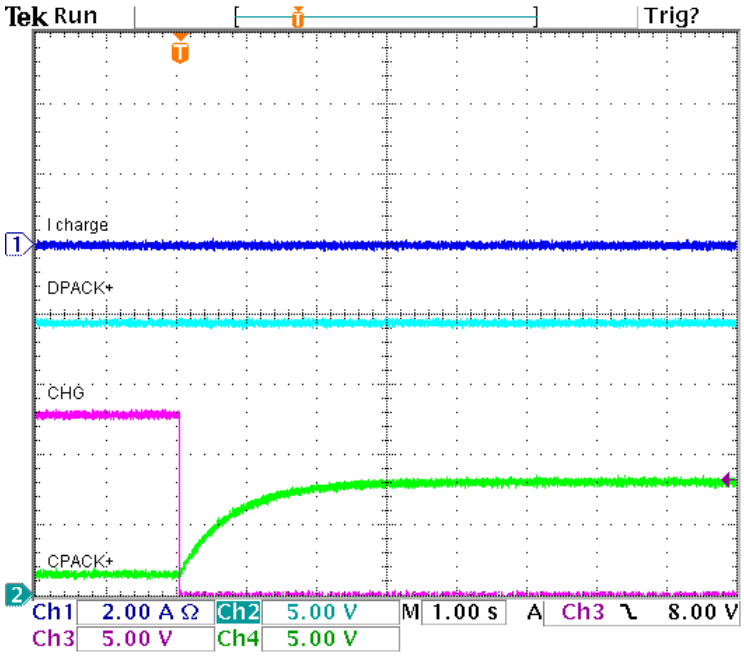

Figure 10. Diode Leakage Example in Hibernate Mode

3 Switching Options

In some systems the delay and switching speed of the Q1 charge FET from the resistive turn off of R_{GSC} will be too slow and a faster circuit will be needed. One option is a NPN transistor to turn off the P-channel FET. An example circuit is shown in Figure 11. When the CHG pin is on Q3 is on and R_{BC} and R_{GPD} divide the pack voltage pulling down the Q4 base and turning it off. D_B pulls down the gate of Q1 turning it on. When the CHG pin is turned off, Q3 turns off and R_{BC} turns the Q4 transistor on reducing the Q1 power FET V_{GS}. As the voltage gets low the NPN turns off leaving R_{GSC} to keep Q1 off. When the collector current must be limited add a resistor to the collector path. The NPN is current controlled but operates to a lower voltage than many signal FETs. If a signal FET is used in this application be sure the signal FET has a lower V_{GSth} than the P-channel FET it is controlling.

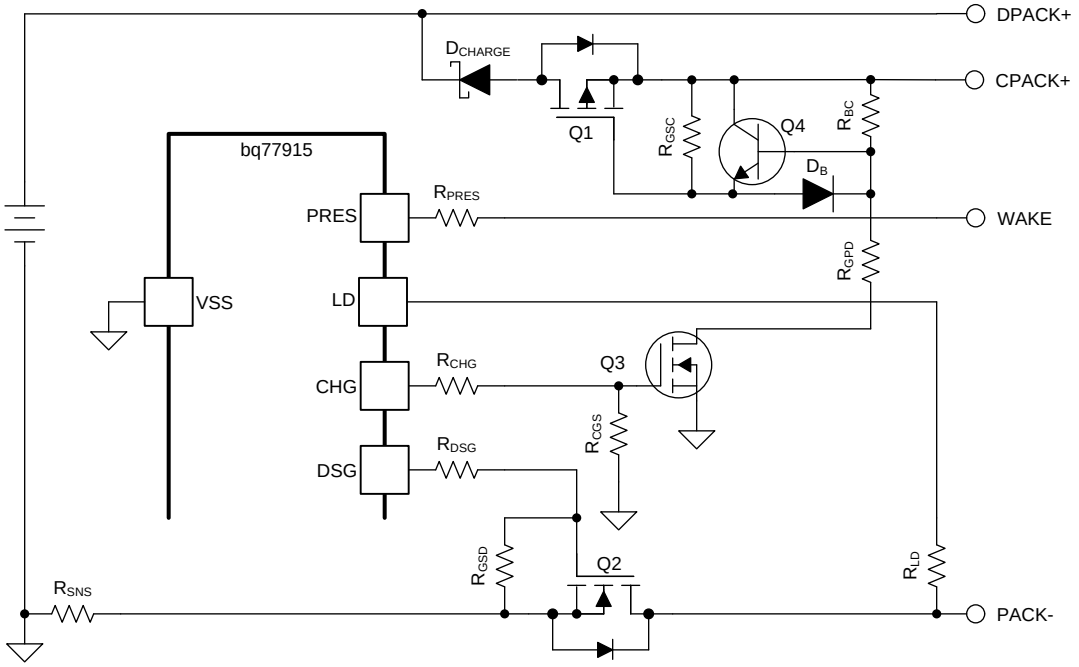

Figure 11. NPN Gate Drive Circuit

A test circuit was constructed using the values in Table 2. The current gain effect with Q4 on is shown in Figure 12. The resulting turn off of the charge shown in Figure 13 is much faster than the resistor turn off in Figure 8. Turn on shown in Figure 14 is similar to Figure 9.

Table 2. NPN Test Circuit Values

Reference Designator or Description	Value
R_{CHG}	4.7k Ω
R_{CGS}	10M Ω
R_{CPD}	1M Ω
R_{BC}	1M Ω
R_{GSC}	10M Ω
(collector resistor)	150 Ω

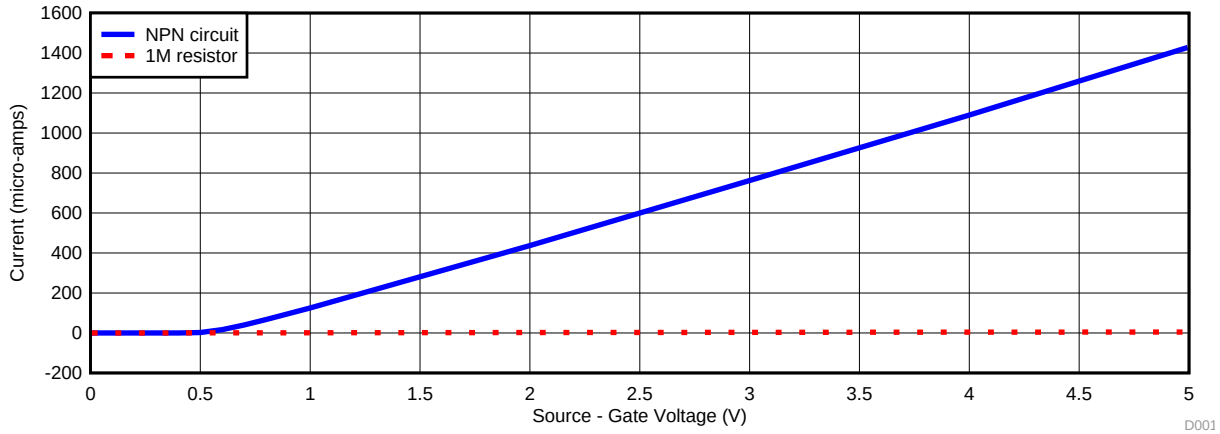

Figure 12. NPN Pull Down Current Comparison

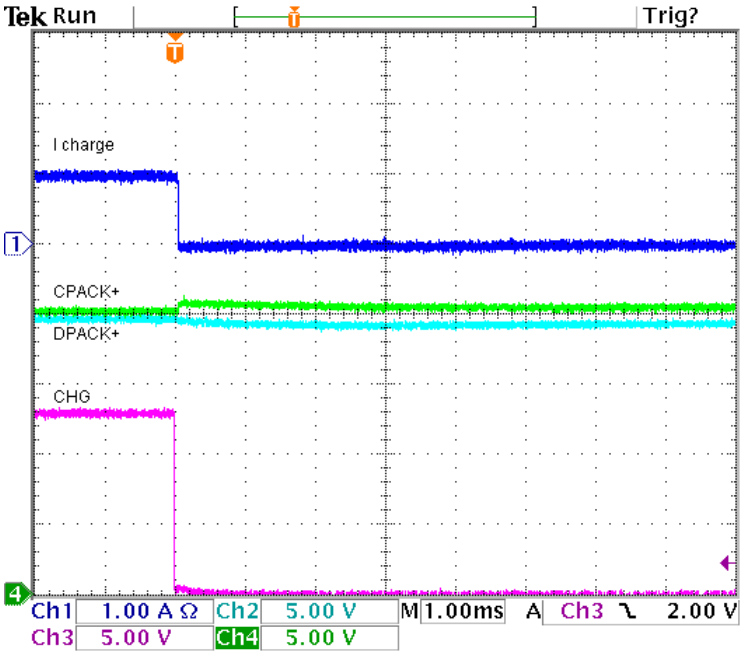

Figure 13. NPN Circuit Turn Off

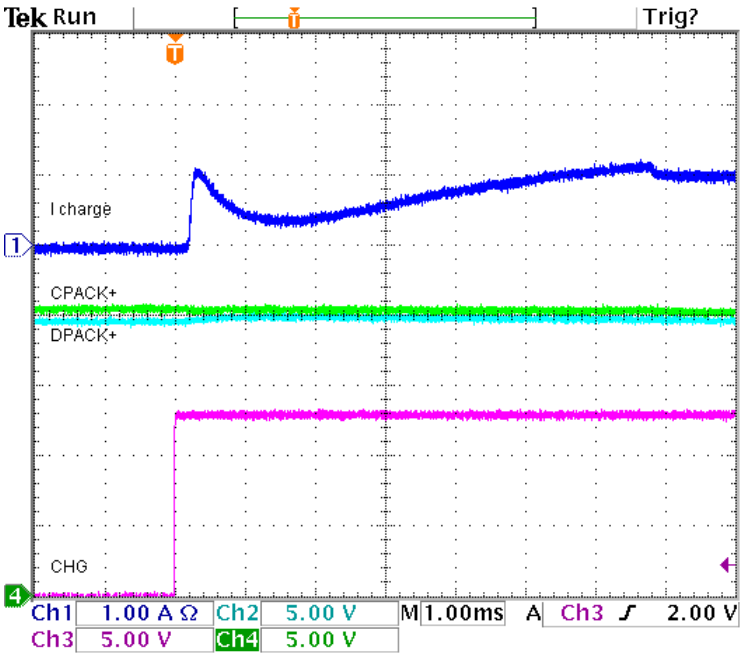

Figure 14. NPN Circuit Turn On

Another circuit option is to use a depletion type device to turn off the P-channel power FET gate. The depletion type device is on with no gate voltage and will turn off the charge FET more aggressively than the NPN example. Figure 15 shows an example of a N-channel JFET circuit. As the pack voltage changes with the circuit on, it operates in different regions as shown in Figure 16. In region 1 the JFET Q4 is on and has a low resistance. As the charger system voltage is raised, current develops a voltage across R_{GPD} and R_{GPD2} in series. When the voltage across R_{GPD2} reaches the Q4 V_{GSoff} voltage, Q4 turns off and the circuit operates in region 2. In region 2 Q4 is off and raising the system voltage creates a voltage drop across R_{GSC} with a slight increase in bias current. With sufficient voltage across R_{GSC}, Q1 will turn on. The minimum acceptable V_{GS} for Q1 and the circuit characteristics determines the minimum system voltage.

As the system voltage continues to increase, the circuit remains in region 2 until the zener diode conducts. Once the zener diode conducts the zener voltage is approximately the sum of the Q4 cutoff voltage and the Q1 gate-source voltage, or $V_Z = V_{GSoff}(Q4) + V_{GS}(Q1)$. Once the zener conducts, shown in region 3, as the system voltage increases the bias current increases as the voltage drop across R_{GPD} increases. These circuits are frequently designed to keep the zener conducting over the system voltage operating range, so bias current is high. When CHG and Q3 turn off, the Q4 V_{GS} is lost and Q4 turns on. Q1 turns off quickly. When the Q1 gate capacitance and the JFET ON resistance are low ringing can occur as shown in Figure 17. In some cases where Q4 has low R_{DSON} add additional resistance to the FET drain path or use another technique to slow the switching and avoid the ringing. This type circuit is typically used with higher current FETs having significant gate capacitance.

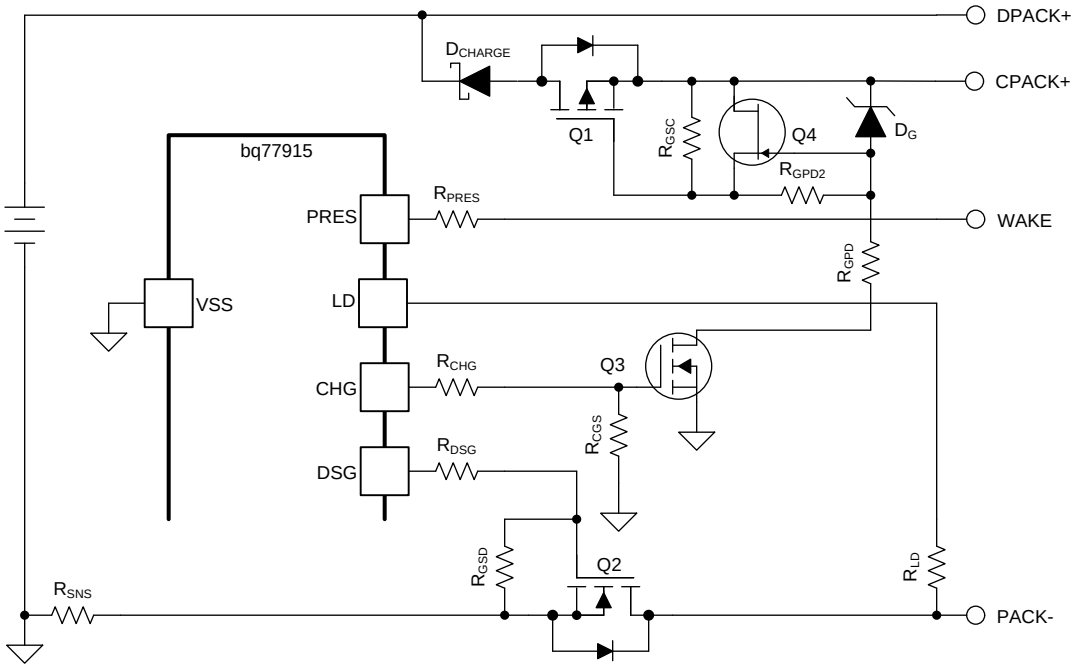

Figure 15. JFET Gate Drive Circuit

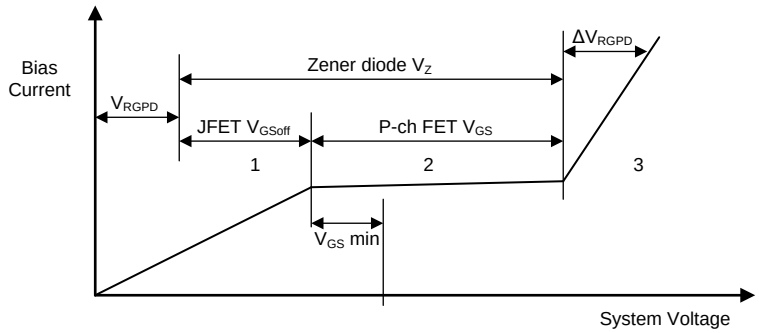

Figure 16. JFET Circuit Bias Current

A turn off example of a JFET test circuit using the values in Table 3 is shown in Figure 17. Compared to the resistive drive turn off in Figure 8, the turn off delay and speed is much faster. Figure 18 shows a turn on example with the JFET test circuit.

Table 3. JFET Test Circuit Values

Reference Designator	Value
R_{CHG}	4.7k Ω
R_{CGS}	10M Ω

Table 3. JFET Test Circuit Values (continued)

Reference Designator	Value
R_{GPD}	100k Ω
R_{GPD2}	205k Ω
R_{GSC}	1M Ω

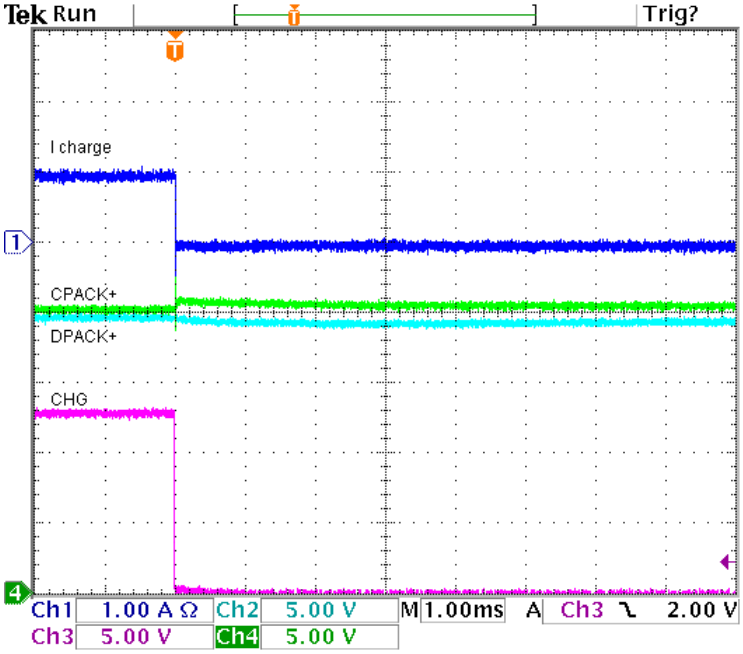

Figure 17. JFET Circuit Turn Off

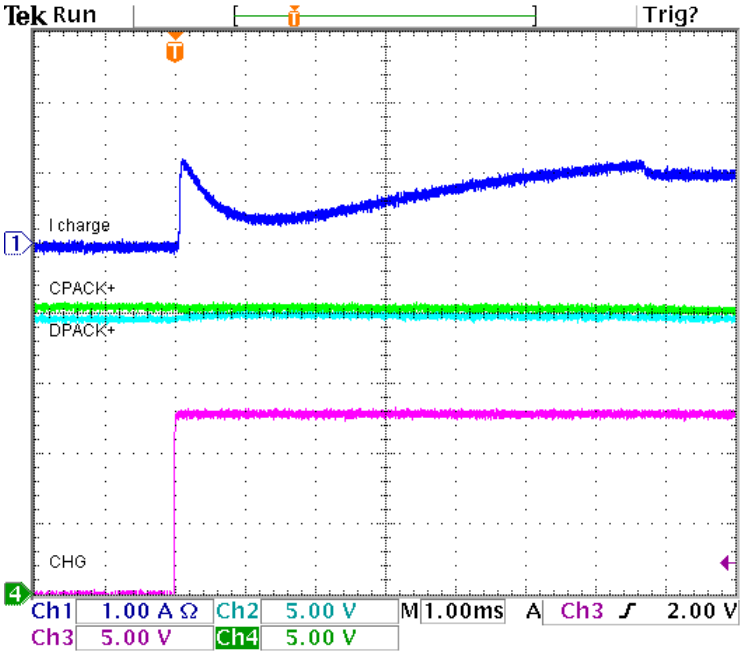

Figure 18. JFET Circuit Turn On

4 Overcurrent Charge Operation

The reader may be curious of the operation of the overcurrent charge (OCC) feature when using the high-side P-channel charge path since the LD pin connection remains on the low side. An OCC event is shown in Figure 19. The charger holds a voltage on the terminals until it recognizes a fault and turns off or is removed. Without other reference, the PACK- terminal remains low. In these test figures of course, the scope probes pull down both PACK- and CPACK+. Figure 20 shows recovery from the OCC fault by application of a 10 kΩ load long after the charger has been removed. R_{LD} forms a resistor divider with the internal R_{LD_INT} resistance. After some contact bounce the load brings PACK- high enough to bring the LD pin voltage above V_{LDT}, the part recovers from OCC and CHG is driven high. CPACK+ is floating in the figure, it is pulled down by the scope probe and pulled up by leakage of the Schottky diode. CPACK+ moves with PACK- due to ESD capacitors between the terminals and across the FET/diode. The alignment of CPACK+ before recovery with CHG after recovery is a coincidence.

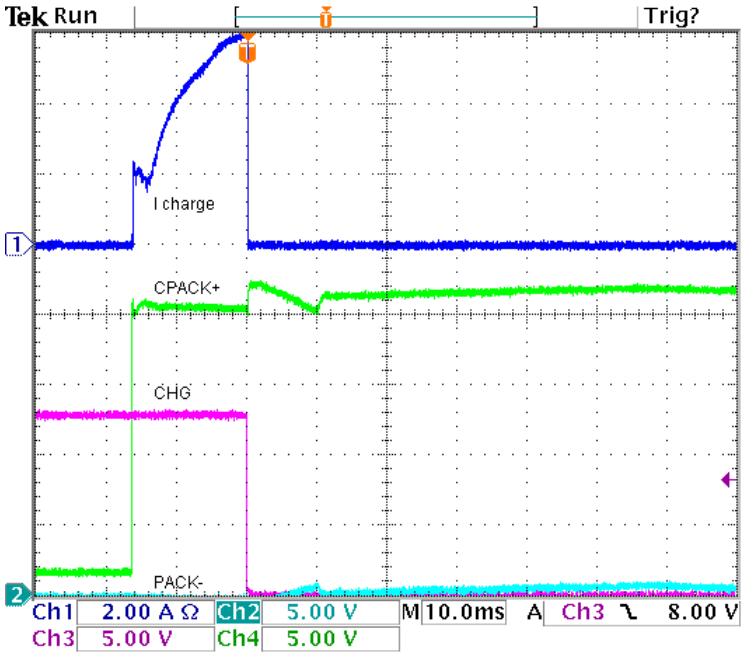

Figure 19. Overcurrent Charge Turn Off

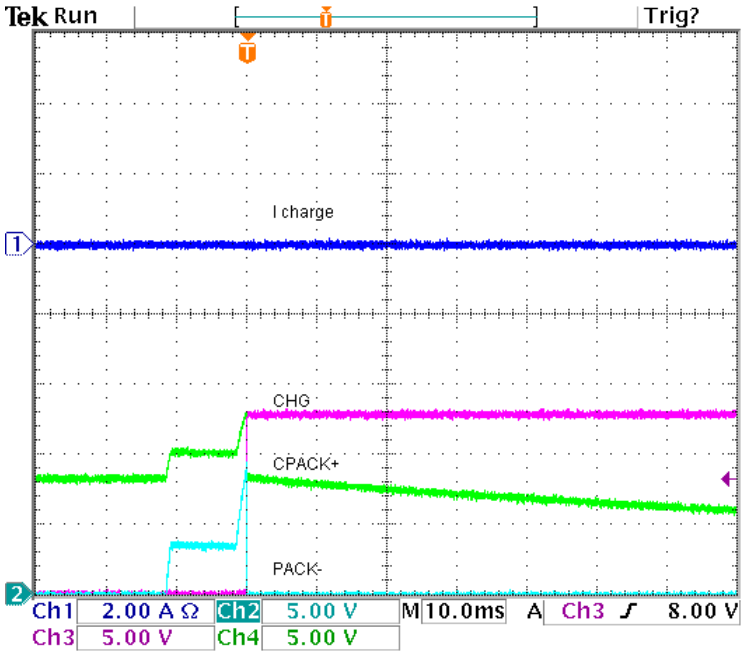

Figure 20. Overcurrent Charge Recovery

5 References

- Texas Instruments, *bq77915 3-5S Low Power Protector with Cell Balancing and Hibernate Mode* data sheet
- Texas Instruments, *bq77905, bq77904 3-5S Ultra Low-Power Voltage, Current, Temperature, and Open Wire Stackable Lithium-ion Battery Protector* data sheet
- Texas Instruments, *bq77905 Separate Current Paths* application report
- Texas Instruments, *bq77905 Using Multiple FETs* application report

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