Application Note

How to Access UCD90XXX Sequencers GPIO

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ABSTRACT

The UCD90xxx family devices are flexible and powerful enough to meet sequencing and monitoring needs. This application note addresses how to access UCD90xxx sequencers' GPIOs with PMBus™ commands. This document does not apply to the UCD9080 and UCD9081 devices.

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Trademarks

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1 Introduction

The UCD90xxx family of digital sequencers, also known as system health monitors, are flexible and powerful enough to meet user sequencing, monitoring, margining and other needs. The entire families of devices are designed to have similar behaviors, but with a different number of rails or some other minor features. Users only need to learn how to use the device once, and can then seamlessly switch to other devices within the family that best fit their future designs. This document is to help applications to access GPIOs from the devices. This document does not apply to the UCD9080 and UCD9081 devices. All commands listed in the document can be found in the publications listed in Section 5.

All byte values are represented in hexadecimal format. These are the codes to understand all I^2C communications that occur:

- [St] - This is the I^2C Start bit.
- [Sr] - This is the I^2C Restart bit. It is identical to the Start bit.
- [Sp] - This is the I^2C Stop bit.
- [A] - This is the I^2C Acknowledge bit.
- [N] - This is I^2C No Acknowledge bit or NACK.
- [AddrW] - This is the I^2C device address with the Write bit.
- [AddrR] - This is the I^2C device address with the Read bit.
- [W:x55] - This is an example of a write byte for value 55 hexadecimal.
- [W/R:Data_^{n}] - This is to indicate that a byte is being write/read by the I^2C master. The n subscript is an ordered integer use to distinguish multiple bytes read back. Data_1 is the MSB, and Data_2 is the LSB for two bytes read.

2 GPIO Capacity

UCD90xxx families of digital sequencers have different GPIO capacity. Please refer to Table 2-1 for the details.

Table 2-1. GPIO Capacity

Devices	UCD9090	UCD9090A	UCD90120A	UCD90124A	UCD90160/ UCD90160A	UCD90320/ UCD90320U
Number GPIO	23	23	26	26	26	100

3 PMBus™ Commands to Access GPIO

UCD90xxx sequencer provides a pair of commands to access GPIO pins. These two commands are GPIO_SELECT (command code 0xFA) and GPIO_CONFIG (command code 0xFB). Both commands follow read/write protocol defined by SMBUS as shown in Figure 3-1.

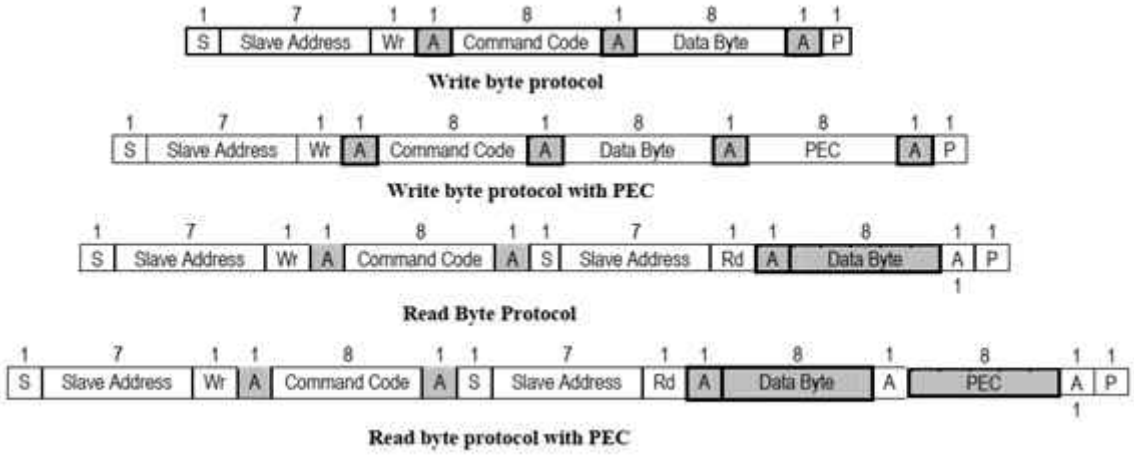

Figure 3-1. Write-Read Byte Protocol

3.1 (FAh) GPIO_SELECT (MFR_SPECIFIC_42)

This read and or write byte command determines to which GPIO that the GPIO_CONFIG command applies. The payload of this command is the **Pin ID** defined by the following Tables Table 3-1, Table 3-2, and Table 3-3.

Table 3-1. UCD9012X, UCD90160x, and UCD90910 PIn ID Definition

Pin ID	Pin Name	Pin Number
0	FPWM1_GPIO5	17
1	FPWM2_GPIO6	18
2	FPWM3_GPIO7	19
3	FPWM4_GPIO8	20
4	FPWM5_GPIO9	21
5	FPWM6_GPIO10	22
6	FPWM7_GPIO11	23
7	FPWM8_GPIO12	24
8	GPI1_PWM1	31
9	GPI2_PWM2	32
10	GPI3_PWM3	42
11	GPI4_PWM4	41
12	GPIO14	29
13	GPIO15	30
14	TDO_GPIO20	37
15	TCK_GPIO19	36
16	TMS_GPIO22	39
17	TDI_GPIO21	38
18	GPIO1	11
19	GPIO2	12
20	GPIO3	13
21	GPIO4	14
22	GPIO13	25

Table 3-1. UCD9012X, UCD90160x, and UCD90910 Pin ID Definition (continued)

Pin ID	Pin Name	Pin Number
23	GPIO16	33
24	GPIO17	34
25	GPIO18	35

Table 3-2. UCD9090x Pin ID Definition

Pin ID	Pin Name	Pin Number
0	FPWM1_GPIO5	10
1	FPWM2_GPIO6	11
2	FPWM3_GPIO7	12
3	FPWM4_GPIO8	13
4	FPWM5_GPIO9	14
5	FPWM6_GPIO10	15
6	FPWM7_GPIO11	16
7	FPWM8_GPIO12	17
8	GPI1_PWM1	22
9	GPI2_PWM2	23
10	GPIO14	21
11	TDO_GPIO19	28
12	TCK_GPIO18	27
13	TMS_GPIO21	30
14	TDI_GPIO20	29
15	GPIO1	4
16	GPIO2	5
17	GPIO3	6
18	GPIO4	7
19	GPIO13	18
20	GPIO15	24
21	GPIO16	25
22	GPIO17	26

Table 3-3. UCD90320x Pin ID Definition

Pin ID	UCD90320 Name	Pin Number
0	MAR_01	J13
1	MAR_02	L5
2	MAR_03	D8
3	MAR_04	K6
4	MAR_05	D4
5	MAR_06	E4
6	MAR_07	F5
7	MAR_08	N5
8	MAR_09	N6
9	MAR_10	K5
10	MAR_11	M6
11	MAR_12	L6
12	MAR_13	D11
13	MAR_14	C12
14	MAR_15	A13
15	MAR_16	B13

Table 3-3. UCD90320x PIn ID Definition (continued)

Pin ID	UCD90320 Name	Pin Number
16	MAR_17	D12
17	MAR_18	C13
18	MAR_19	E12
19	MAR_20	E13
20	MAR_21	M13
21	MAR_22	L12
22	MAR_23	M5
23	MAR_24	J12
24	EN1	M9
25	EN2	N9
26	EN3	L10
27	EN4	K10
28	EN5	L9
29	EN6	K9
30	EN7	N8
31	EN8	M8
32	EN9	L8
33	EN10	K8
34	EN11	N7
35	EN12	M7
36	EN13	K7
37	EN14	L7
38	EN15	N4
39	EN16	N3
40	EN17	K3
41	EN18	K4
42	EN19	J4
43	EN20	J2
44	EN21	J3
45	EN22	H4
46	EN23	H3
47	EN24	G4
48	EN25	F13
49	EN26	F12
50	EN27	G11
51	EN28	H10
52	EN29	H13
53	EN30	H12
54	EN31	H11
55	EN32	L13
56	LGPO1	C9
57	LGPO2	B9
58	LGPO3	A9
59	LGPO4	C8
60	LGPO5	D5
61	LGPO6	C5
62	LGPO7	C6

Table 3-3. UCD90320x PIn ID Definition (continued)

Pin ID	UCD90320 Name	Pin Number
63	LGPO8	C4
64	LGPO9	L3
65	LGPO10	M1
66	LGPO11	M2
67	LGPO12	M3
68	LGPO13	L4
69	LGPO14	N1
70	LGPO15	M4
71	LGPO16	N2
72	DMON1	F4
73	DMON2	F3
74	DMON3	G3
75	DMON4	D10
76	DMON5	L11
77	DMON6	N12
78	DMON7	N11
79	DMON8	M11
80	GPIO1	B11
81	GPIO2	B12
82	GPIO3	C11
83	GPIO4	A12

3.2 (FBh) GPIO_CONFIG (MFR_SPECIFIC_43)

This read/write byte command, when applications write, is to configured the GPIO pin assigned by the GPIO_SELECT(FBh) command to a command based GPIO. When application reads, it is to return the status of the assigned GPIO regardless how this pin is configured.

Table 3-4. GPIO_CONFIG(0xFBh) Command Payload Definition

BIT	7	6	5	4	3	2	1	0
Description	Reserved	Reserved	Reserved	Reserved	Status	Out_Value	Out_Enable	Enable

The Status bit is read-only and gives the current state of the pin. The Out_Enable bit determines if the pin is an output (1 – actively driven) or an input (0 – high impedance). The Out_Value bit determines the state of the pin when it is configured as an output. The Enable bit is a flag indicating whether this command should be processed. When the Enable bit is cleared, this command is ignored. If user wants to temporarily change to an output pin's state, this command should be written twice. In the first time, the Enable bit should be set to 1 such that the changes can be applied. In the second time, the Enable bit should be set to 0. This will not change the pin's state; and because the Enable bit is 0, STORE_DEFAULT_ALL command will ignore this command when storing configurations from RAM to flash. This way, the new temporary configuration will not overwrite the default configuration

NOTE: Configuring a pin that is also being used by another function (enable, fan control, LGPO, GPI and so forth) may likely result in unexpected and unwanted behavior

4 Examples

This section demonstrates how to use both GPIO_SELECT(FAh) and GPIO_CONFIG(FBh) commands to configure or read GPIOs.

4.1 Configure GPIO to Hi-Z

This section is to demonstrate how to configure a GPIO pin(FPWM2_GPIO6) to be a Hi-Z signal as shown in Figure 4-1.

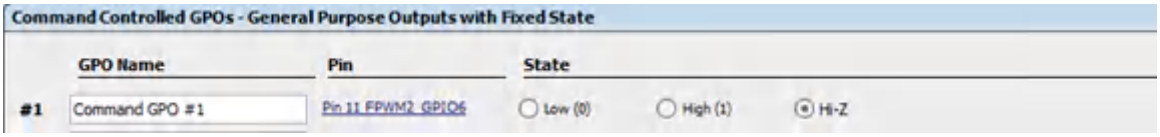

Figure 4-1. Configure GPIO to Hi-Z

The Pid ID of the **FPWM2_GPIO6** is 1 from Table 3-1 and Table 3-2.

Application need send out the following commands:

Write GPIO_SELECT command to choose the target GPIO. Payload 0x01 is to select FPWM2_GPIO6 pin.

- [St] [AddrW] [A] [W:**0xFA**] [A] [W:**0X01**][A][Sp]

Write GPIO_CONFIG command to output HIGH signal. Payload 0x1 is to enable the Pin without output disable.

- [St] [AddrW] [A] [W:**0xFB**] [A] [W:**0X01**][A][Sp]

4.2 Configure GPIO to Output HIGH or LOW

This section demonstrates how to configure a GPIO pin (FPWM8_GPIO12) to output HIGH or LOW signal as shown in Figure 4-2.

Figure 4-2. Configure GPIO to Output HIGH or LOW

The Pid ID of the FPWM8_GPIO12 is 7 from Table 3-1 and Table 3-2

Application need send out the following commands:

Write GPIO_SELECT command to choose the target GPIO. Payload 0x07 is to select FPWM8_GPIO12 pin

- [St] [AddrW] [A] [W:**0xFA**] [A] [W:**0X07**][A][Sp]

Write GPIO_CONFIG command to output HIGH signal. Payload 0x7 is to enable the Pin and output HIGH

- [St] [AddrW] [A] [W:**0xFB**] [A] [W:**0X07**][A][Sp]

Write GPIO_CONFIG command to output LOW signal. Payload 0x3 is to enable the Pin and output LOW

- [St] [AddrW] [A] [W:**0xFB**] [A] [W:**0X03**][A][Sp]

4.3 Read GPIO Status

This section demonstrates how to read status of a GPIO pin (FPWM8_GPIO12).

The Pid ID of the FPWM8_GPIO12 is 7 from Table 3-1 Table 3-2.

Application need sends out the following commands:

Write GPIO_SELECT command to choose the target GPIO. Payload 0x07 is to select FPWM8_GPIO12 pin,

- [St] [AddrW] [A] [W:**0xFA**] [A] [W:**0X07**][A][Sp]

Read GPIO_CONFIG command to get the status of FPWM8_GPIO12

- [St] [AddrW] [A] [W:**0xFB**] [A] [SR][Addr][A][R:data][N][Sp]

If the bit 3 of the return data is 1, the signal of the FPWM8_GPIO12 is HIGH otherwise it is LOW.

5 References

- Texas Instruments, *UCD90xxx Sequencer and System Health Controller PMBus Command Reference User's Guide*.
- Texas Instruments, *UCD90320 Sequencer and System Health Controller PMBus Command Reference User's Guide*.
- Texas Instruments, *UCD90320U Sequencer and System Health Controller PMBus Command Reference User's Guide*.
- System Management Bus(SMBus) Specification 2.0.
- *The PMBus Power System Management Protocol Specification Part II - Command Language, Revision 1.1,* 5 February 2007, available from www.pmbus.org.

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