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TMS320C62x/67x Power Supply Solutions for 1-2 DSPs: Using the TL5001A and TPS7133

Application Report

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TMS320C62x/67x Power Supply Solutions for 1–2 DSPs: Using the TL5001A and TPS7133

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ABSTRACT

This application report describes a low-cost power solution for Texas Instruments' TMS320C6000 DSP applications using the TL5001 PWM controller and the TPS7133 low drop-out voltage regulator. The reference design included in this report uses the TL5001AEVM-122 (SLVP122) evaluation module (EVM), which is available for customer testing and evaluation.

1 Introduction

The TMS320C6000 series of digital signal processors (DSPs) is Texas Instrument's highest performance DSP, ranging in operating frequency from 100 MHz to 250 MHz with an execution speed of up to 2000 MIPS. In order to maintain high performance and low power consumption a separate core and I/O supply must be supplied to the 'C6000. For the current generation of 'C6000 DSPs, the I/O supply is 3.3 V. The core supply requirement depends on the specific DSP, and for the current generation of 'C6000 devices is either 2.5 V or 1.8 V. Table 1 summarizes the voltage supply and consumption requirements for the current 'C6000 devices. For the most current and detailed information on the power requirements of the TMS320C6000 series of DSPs, refer to the application note entitled *TMS320C6000 Power Consumption Summary.*

Table 1. Summary of the Voltage Supply and Consumption Requirements

DEVICE	MAX FREQUENCY	CORE VOLTAGE	CURRENT REQUIRED	I/O VOLTAGE	CURRENT REQUIRED	TYPICAL I/O SYSTEM CURRENT
'C6201	200 MHz	2.5 V	~0 to 2.5 A	3.3 V	~0 to 130 mA	~430 mA
'C6201B	200 MHz	1.8 V	~0 to 800 mA	3.3 V	~0 to 130 mA	~430 mA
'C6202	250 MHz	1.8 V	~0 to 1.3 A	3.3 V	~0 to 160 mA	~460 mA
'C6211	150 MHz	1.8 V	~0 to 800 mA	3.3 V	~0 to 130 mA	~430 mA
'C6701	167 MHz	1.8 V	~0 to 800 mA	3.3 V	~0 to 160 mA	~460 mA
'C6711	150 MHz	1.8 V	~0 to 700 mA	3.3 V	~0 to 130 mA	~430 mA

In single-DSP applications, the power requirement is usually higher to cover the whole application. Another important note is that the start-up sequencing should be considered for TMS320C6000 DSPs. The specification states that both core and I/O supplies should be brought up simultaneously, but, if possible, the core should be brought up first. This specification prevents unknown values from being driven on the I/O pins due to the core not being fully powered up. Therefore, the design presented here assures that the core powers up before the I/O supply. The cost and the component count are also important for DSP users.

In systems including more than one DSP, the total power for the DSPs must be supplied in addition to the power required for the rest of the system. This increased power can exceed the current ratings for the design described in this application report. TI provides other solutions to cover higher output power. Table 2 shows available power supply products for a given output current requirement. Appropriate SVS (Supply Voltage Supervisors) products are shown in the table combined with LDO and SVS products from TI. The latest version of this table can be found at the URL http://www.ti.com/sc/docs/msp/c6000.htm.

Table 2. Power Supply Products for TMS320C6000 DSPs

DSP FAMILY	DSP SUPPLY VOLTAGE	DSP SUPPLY CURRENT (TYPICAL)	SVS	SUPPLY CURRENT					
				POWERING DSP ONLY	SYSTEM INCLUDING ONE OR MORE DSPs				
					<250 mA	250–500 mA		500 mA–3 A	3 A
					LDO	LDO	LDO+SVS	SMPS	SMPS
TMS320C6201	2.5 V core	2.5 A @ 200 MHZ	TPS3305-25	TL5001A				TL5001A	TPS5625
	3.3 V I/O	150 mA @ 200 MHz		TPS7133	TPS7233	TPS7133	TPS7333	TL5001A	TPS5633
TMS320C6201B	1.8 V core	830 mA @ 200 MHz	TPS3305-18	TL5001A				TL5001A	TPS5618
	3.3 V I/O	130 mA @ 200 MHz		TPS7133	TPS7233	TPS7133	TPS7333	TL5001A	TPS5633
TMS320C6202	1.8 V core	1.4 A @ 250 MHZ	TPS3305-18	TL5001A				TL5001A	TPS5618
	3.3 V I/O	160 mA @ 250 MHz		TPS7133	TPS7233	TPS7133	TPS7333	TL5001A	TPS5633
TMS320C6211	1.8 V core	830 mA @ 150 MHz	TPS3305-18	TL5001A				TL5001A	TPS5618
	3.3 V I/O	130 mA @ 150 MHz		TPS7233	TPS7233	TPS7133	TPS7333	TL5001A	TPS5633
TMS320C6701	1.8 V core	830 mA @ 167 MHz	TPS3305-18	TL5001A				TL5001A	TPS5618
	3.3 V I/O	160 mA @ 167 MHz		TPS7133	TPS7233	TPS7133	TPS7333	TL5001A	TPS5633

The design in this application report fully meets all the above requirements by using a low cost switching power supply using the TL5001A PWM controller and TPS7133 low dropout voltage regulator from Texas Instruments. The TL5001A PWM controlled power supply is implemented to offer 1.8 V at 3 A for core power, which is more than adequate for TI's current family of 'C6000 DSPs. For other 'C6000 DSP applications requiring 2.5 V for core power, the design is also capable of being configured for an output of 2.5 V at 3 A. The single output reference design using TL5001A (see references) is used for this application. The TPS7133 low dropout voltage regulator is used to offer 3.3 V at 0.50 A for I/O power. The total component count is minimized to approximately 36, including board and connectors. The TL5001A offers a 3% voltage reference tolerance. The input and the logic voltage for both outputs are 5 V.

The design shown in this application report is a reference design, and evaluation module (EVM), TL5001AEVM-122 (SLVP122), is available for customer testing and evaluation. The intent is to allow a customer to fully evaluate the given design using the plug-in EVM supply shown here. For subsequent customer board revisions, the EVM design can be copied onto the users' PCB to shorten design cycle time, component count, and board cost.

Table 3 summarizes the outputs of this design.

Table 3. Outputs

INPUT VOLTAGE	OUTPUT VOLTAGE	OUTPUT CURRENT
V_I = 4.5 ~ 5.5 V	V_{out1} = 1.8 Vor 2.5 V	I_{out1} = 3 A
	V_{out2} = 3.3 V	I_{out2} = 0.5 A

The design is also ready for the other output voltages. For example, output 1 can be 1.5 V or 1.3 V.

2 Circuit Diagram

Figure 1 shows the circuit diagram for supplying a core voltage of 1.8 V and an I/O voltage of 3.3 V.

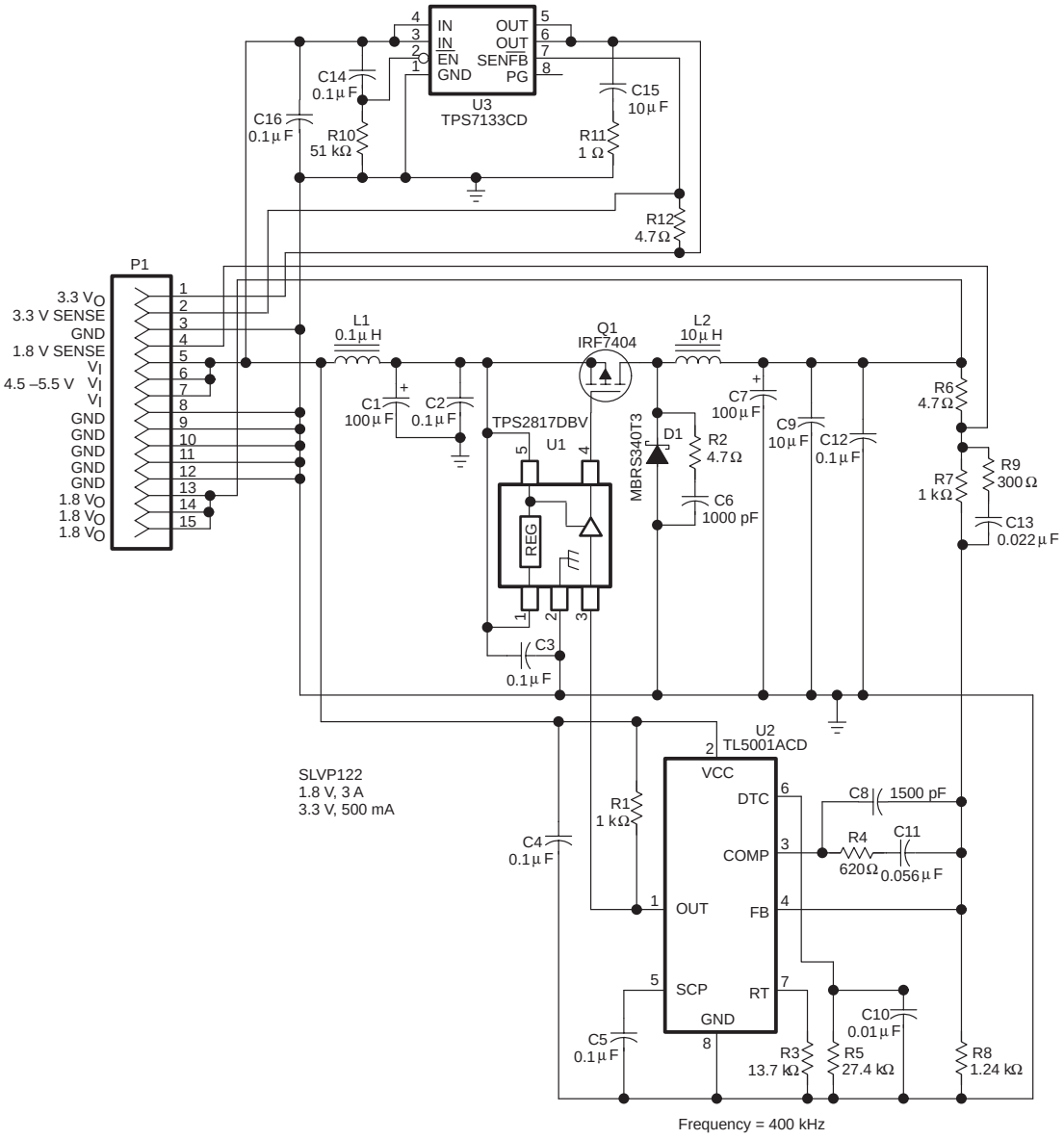

Figure 1. Circuit Diagram for 1.8 V Core/3.3 V I/O

The TL5001A PWM controller provides a cost-effective solution for supplying core power to a high performance DSP such as the TMS320C6201. This controller satisfies all requirements for powering this DSP, such as low cost, low parts count, good transient response, and excellent output voltage accuracy.

The TPS7133 is a nominal 5 V input to 3.3 V low dropout voltage regulator also designed by Texas Instruments. A 1 Ω resistor (R11) is in series with a 10 μF output capacitor (C15) to achieve the output voltage regulation stability. A resistor (R10) and capacitor (C14) are connected to the enable pin to get the correct start-up sequence.

Start-up sequencing is required by the TMS320C6000. The specifications state that to avoid potential I/O contention on a system level, the core and I/O supplies should come up simultaneously, or the core first, followed by the I/O supply. R10 and C14 in the circuit delay the 3.3V enough to assure the sequence. As seen in Figure 9 and Figure 10, this design satisfies that requirement. It can be seen from the start-up waveforms that the 1.8-V or 2.5-V output reaches the nominal voltage first, followed by the 3.3 V output.

Reset of both regulators due to fault conditions is accomplished automatically when the condition is removed.

These two supplies should be close to the DSP to minimize the trace resistance and inductance and the ground loop current between the two output grounds. Ground loop current can generate radiated EMI noise that can adversely affect any circuitry within the loop. Make the ground connection right on the DSP to minimize the problem.

3 Operating Conditions

The recommended operating conditions and electrical characteristics for the design circuit are described in 3.1 and 3.2.

3.1 Recommended Operating Conditions

	MIN	TYP	MAX	UNIT
V_I	4.5	5	5.5	V
Operating ambient temperature, T_A	0		85	°C

3.2 Electrical Characteristics Over Recommended Operating Conditions

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output voltage 1 setpoint tolerance, (1.8 V or 2.5 V)	Over all conditions		–1.5%		1.5%	
Output voltage 2 setpoint tolerance, (3.3 V)	Over all conditions		–1.5%		1.5%	
Load regulation of 1.8 V or 2.5 V	Over all conditions			0.01%	1.6%	
Load regulation of 3.3 V	Over all conditions			0.6%	2.1%	
Output current 1 (1.8 V or 2.5 V)	T_A = 25°C		0		3	A
Output current 2 (3.3 V)	T_A = 25°C		0		0.5	A
Efficiency	T_A = 25°C,	1.8 V/3.3 V		71% (full load)		
	T_A = 25°C,	2.5 V/3.3 V		76% (full load)		
Switching frequency of 1.8 or 2.5 V output	T_A = 25°C			400		kHz
Turnon input voltage	T_A = 25°C		4.30		4.49	V
Under voltage lockout	T_A = 25°C,	50% load	4.30		4.48	V
Over current 1	T_A = 25°C,	V_I = 5 V		3.25		A
Over current 2	T_A = 25°C,	V_I = 5 V		1.2		A
Short circuit current 1†	T_A = 25°C,	V_I = 5 V		0		A
Short circuit current 2†	T_A = 25°C,	V_I = 5 V		0		A

† Under short circuit condition, the outputs are turned off.

4 Bill of Materials

Table 4 lists the materials required to construct the design.

Table 4. Bill of Materials for 1.8 V Core/3.3 V I/O

REF.	DESCRIPTION	SIZE	PART NUMBER	MFR
C1	Capacitor, POSCAP, 100 μF, 10 V, 20%	D case	10TPB100M	Sanyo
C2	Capacitor, Ceramic, 0.1μF, 16 V, X7R, 20%	1206	GRM42–6X7R104M016A	muRata
C3	Capacitor, Ceramic, 0.1 μF, 16 V, X7R, 20%	1206	GRM42–6X7R104M016A	muRata
C4	Capacitor, Ceramic, 0.1 μF, 16 V, X7R, 20%	1206	GRM42–6X7R104M016A	muRata
C5	Capacitor, Ceramic, 0.1 μF, 16 V, X7R, 20%	1206	GRM42–6X75104M016A	muRata
C6	Capacitor, Ceramic, 1000 pF, 50 V, X7R, 20%	603	GRM39X7R104M050A	muRata
C7	Capacitor, POSCAP, 100 μF, 10 V, X7R, 20%	D case	10TPB100M	Sanyo
C8	Capacitor, Ceramic, 1500 pF, 50 V, X7R, 10%	603	GRM39X7R152K050A	muRata
C9	Capacitor, Ceramic, 10 μF, 16 V, Y5V,+80%–20%	1210	GRM235Y5V106Z016A	muRata
C10	Capacitor, Ceramic, 0.01 μF, 50 V, X7R, 20%	1206	GRM42–6X7R103M050A	muRata
C11	Capacitor, Ceramic, 0.056 μF, 50 V, X7R, 10%	805	GRM40X7R103M050A	muRata
C12	Capacitor, Ceramic, 0.1 μF, 16 V, X7R, 20%	1206	GRM42–6X7R104M016A	muRata
C13	Capacitor, Ceramic, 0.022 μF, 50 V, X7R, 10%	805	GRM40X7R223K050A	muRata
C14	Capacitor, Ceramic, 0.1 μF, 16 V, X7R, 20%	1206	GRM42–6X7R104M016A	muRata
C15	Capacitor, Ceramic, 10 μF, 16 V, Y5V, +80%–20%	1210	GRM235Y5V106Z016A	muRata
C16	Capacitor, Ceramic, 0.1 μF, 16 V, X7R, 20%	1206	GRM42–6X7R104M016A	muRata
D1	Diode, Schottky, 3 A, 40 V	SMC	MBRS340T3	Mot
L1	Inductor, SM, Shielded, 0.1 μH, 2.13A, 25 mΩ	1812	S1008–101K	Delevan
L2	Inductor, 10 μH, 3.9 A, 0.025 Ω	0.51 × 0.37	DO3316P–103	Coilcraft
P1	Header, Right Angle, 15-pin, 0.1 ctrs, 0.3” pins	0.1	PTC36SBBN	Sullins
Q1	MOSFET, P-Ch, 20 V, 0.040 Ω	SO–8	IRF7404	IR
R1	Resistor, SMD, MF, 1 kΩ, 1/16 W, 5%	603		
R2	Resistor, SMD, MF, 4.7 Ω, 1/16 W, 5%	603		
R3	Resistor, SMD, MF, 13.7 kΩ, 1/16 W, 1%	603		
R4	Resistor, SMD, MF, 620 Ω, 1/16 W, 5%	603		
R5	Resistor, SMD, MF, 27.4 kΩ, 1/16 W, 1%	603		
R6	Resistor, SMD, MF, 4.7 Ω, 1/16 W, 5%	603		
R7	Resistor, SMD, MF, 1 kΩ, 1/16 W, 1%	603		
R8†	Resistor, SMD, MF, 1.24 kΩ, 1/16 W, 1%	603		
R9	Resistor, SMD, MF, 300 Ω, 1/16 W, 5%	603		
R10	Resistor, SMD, MF, 51 kΩ, 1/16 W, 5%	603		
R11	Resistor, SMD, MF, 1 Ω, 1/16 W, 5%	603		
R12	Resistor, SMD, MF, 4.7 Ω, 1/16 W, 5%	603		
U1	Driver, high-speed, single channel, 2A	SOT25	TPS2817DBV	TI
U2	PWM controller	SO-8	TL5001AD	TI
U3	Low dropout voltage regulator	D case	TPS7133CD	TI

† The value of R8 for the 2.5 V core output is 665 Ω.

5 Test Results

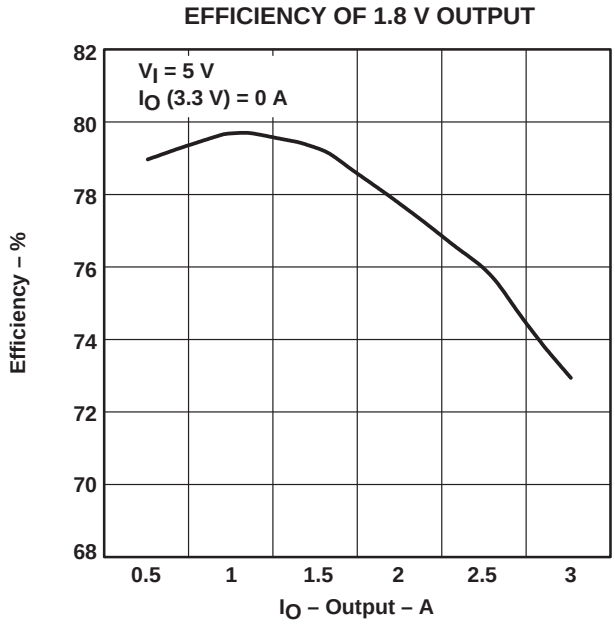

Figure 2. Efficiency of 1.8 V Output With 3.3 V/0 A

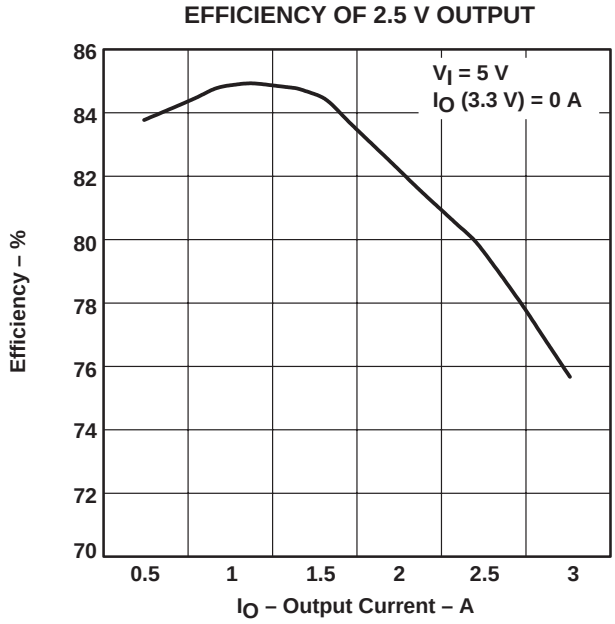

Figure 3. Efficiency of 2.5 V Output With 3.3 V/0 A

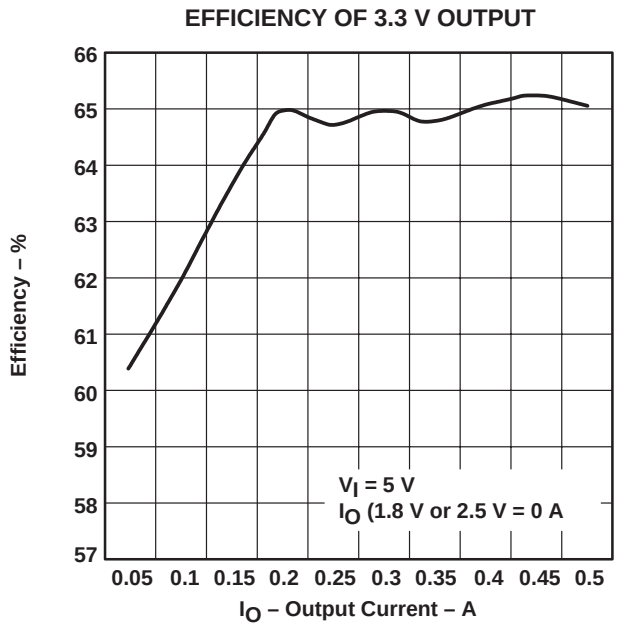

Figure 4. Efficiency of 3.3 V Output With 1.8 V or 2.5 V/0 A

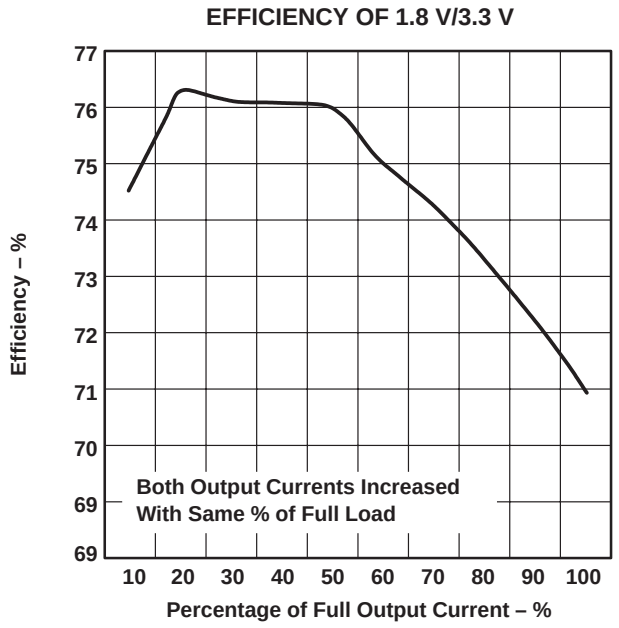

Figure 5. Efficiency of 1.8 V/3.3 V at Same Output Current Increasing Rate

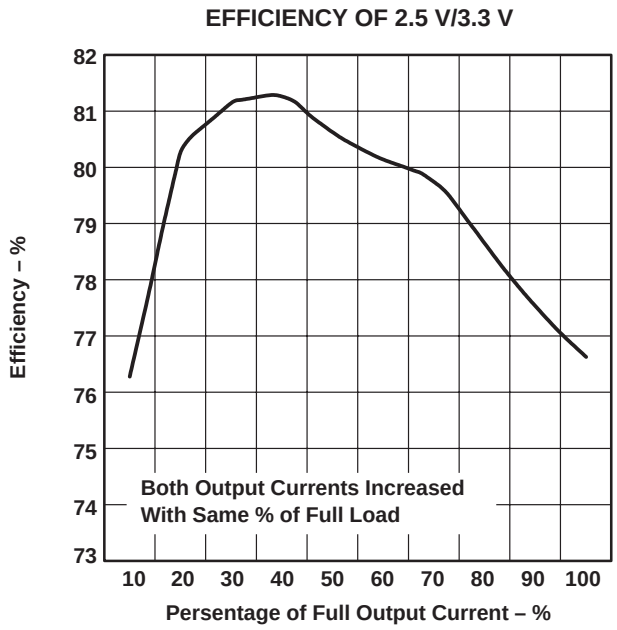

Figure 6. Efficiency of 2.5 V/3.3 V at Same Output Current Increasing Rate

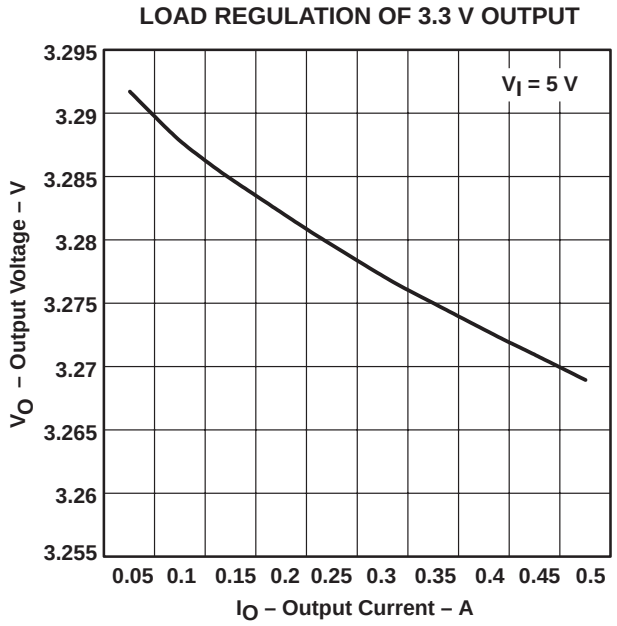

Figure 7. Load Regulation on 3.3 V Output

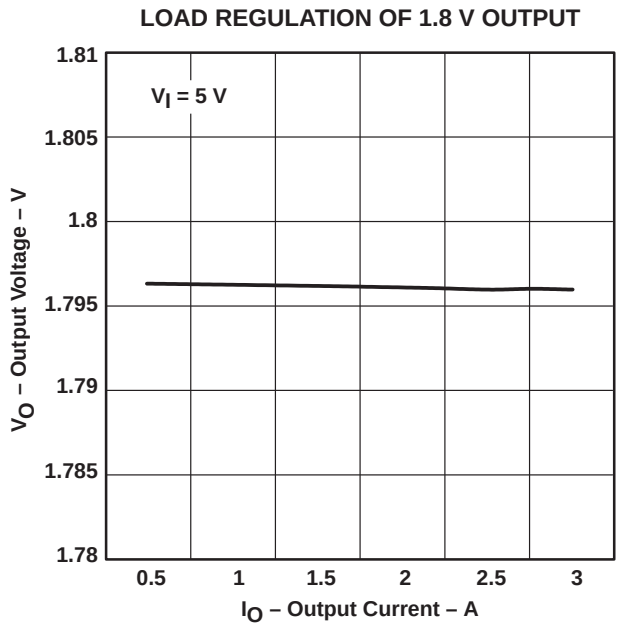

Figure 8. Load Regulation of 1.8 V Output

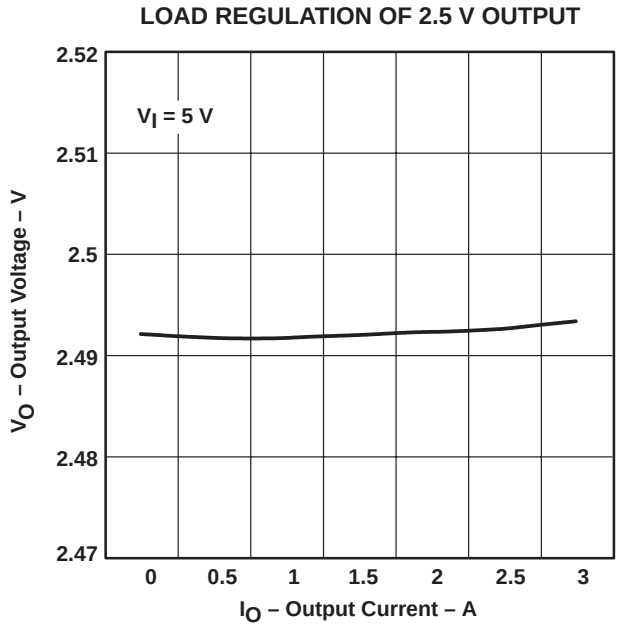

Figure 9. Load Regulation of 2.5 V Output

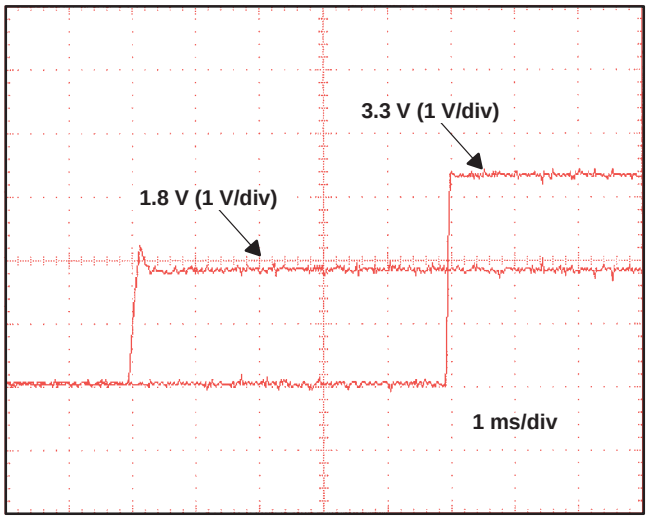

Figure 10. 1.8 V/3.3 V Output Voltage Start-Up Waveforms

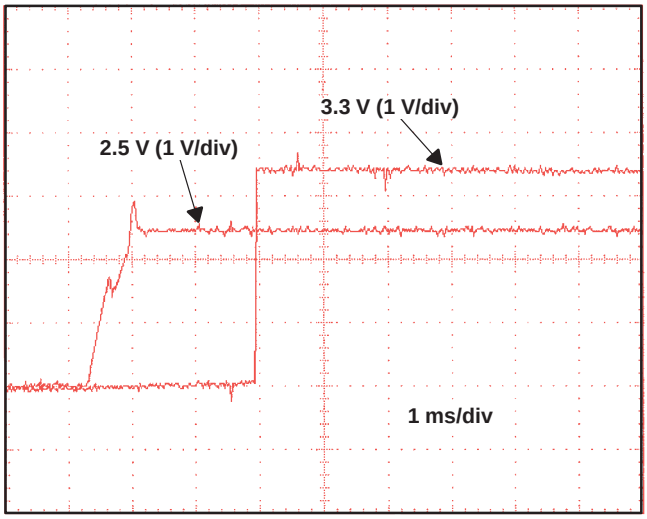

Figure 11. 2.5 V/3.3 V Output Voltage Start-Up Waveforms

6 Board Layouts

The board size is 2.10 (in) L × 0.875 (in) W × 0.375 (in) H.

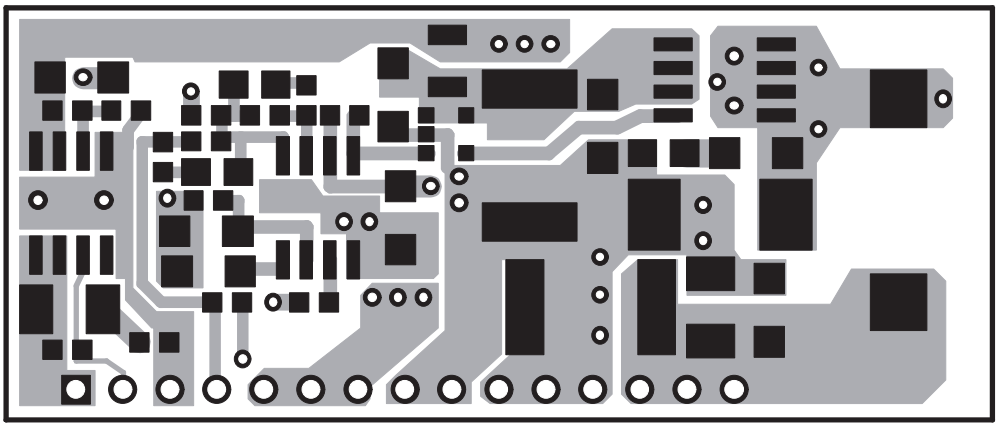

Figure 12. Board Layout (Top Side)

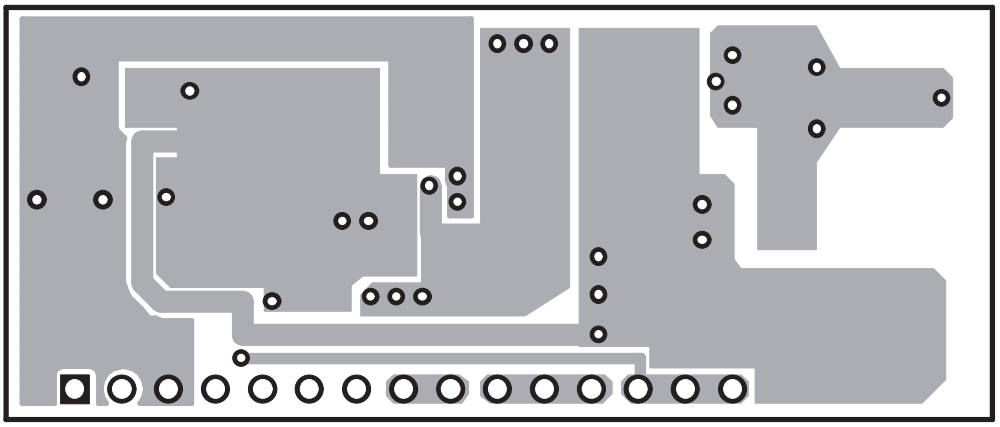

Figure 13. Board Layout (Bottom Side)

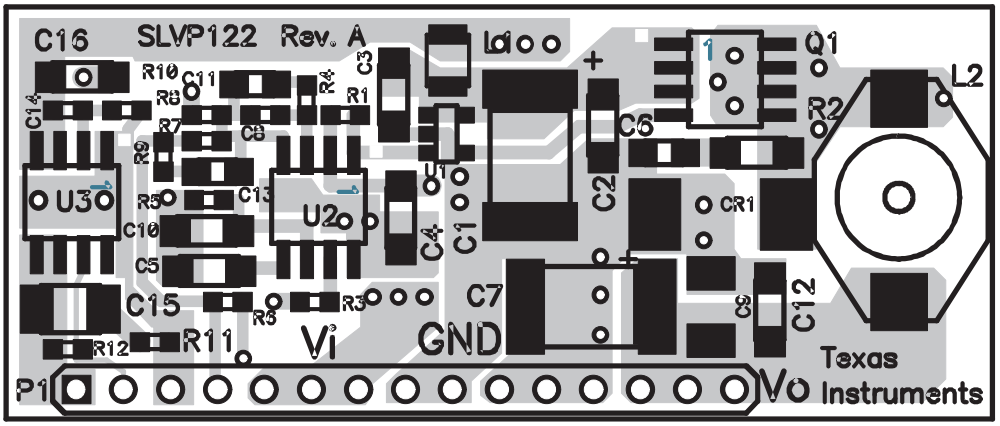

Figure 14. Board Assembly

7 Summary

The design in this application report provides a simple, cost-effective solution for powering high-performance DSPs.

8 References

1. TL5001, TL5001A, TL5001Y Pulse-Width-Modulation Control Circuits, Texas Instruments, revised 1998, Literature No. SLVS084D.
2. TPS7101Q, TPS7133Q, TPS7148Q, TPS7150Q, TPS7101Y, TPS7133Y, TPS7148Y, TPS7150Y Low-Dropout Voltage Regulators, Texas Instruments, revised 1997, Literature No. SLVS092F.
3. *SLVP101, SLVP102, and SLVP103 Buck Converter Design Using the TL5001 User's Guide*, Texas Instruments, 1998, Literature No. SLVU005.