Application Report
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DaVinci™ Sequencing Using The TPS65023

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ABSTRACT

The Texas Instruments DaVinci™ family of application processors has specific sequencing and reset requirements. The TPS65023, designed to supply the DaVinci™ family's power needs, has some built-in, but not immediately obvious, functions that can also easily and cheaply support the sequencing and reset requirements, eliminating the need for external comparators or supervisors. This document starts with a quick overview of the DaVinci™ family sequencing requirements. The TPS65023 features – two general-purpose comparators and a Power Good output – are then described individually. After the setup, the simple connections combining them to fulfill the power sequencing and reset requirements are detailed.

The DaVinci™ family of processors is forgiving in power sequencing. The only hard requirement, listed in Section 5.3.1 of the data sheets for TMS320DM6441 (SPRS359), TMS320DM6443 (SPRS282), and TMS320DM6446 (SPRS283), is the need for the ARM microcontroller core (1.2-V domain) to come up prior to the Memory (1.8-V domain) and I/O (3.3-V domain). The Memory and I/O voltages may come up in any order after the ARM core is powered. The DaVinci™ reset signal, $\overline{\text{RESET}}$, must also be held low until all three voltage domains are fully up.

These straightforward requirements are easy to implement using features built into the TPS65023. The next part of this document describes the features in more detail before presenting the application solution to DaVinci™ sequencing.

Two pairs of input/output pins, LOWBAT_SNS with $\overline{\text{LOWBAT}}$ and PWRFAIL_SNS with $\overline{\text{PWRFAIL}}$, are often overlooked in the TPS65023. These are the input/output pairs for two independent and stand-alone comparators, with a 1-V ±1% reference supplied internally by the TPS65023. The intended use of the pins was signaling to the processor when the battery supplying power reached a low threshold (LOWBAT) and when the system needed to be shut down (PWRFAIL) – this lead to the pin names. Using an external resistor divider network, the designer can set the voltage when each output pin activates, flagging the processor. The outputs are the open-drain inversion of the comparator output. Figure 1 shows a block diagram of the comparators and how they could be used as originally intended, with the $\overline{\text{LOWBAT}}$ signal going low at 3.27 V and the $\overline{\text{PWRFAIL}}$ signal going low at 3 V.

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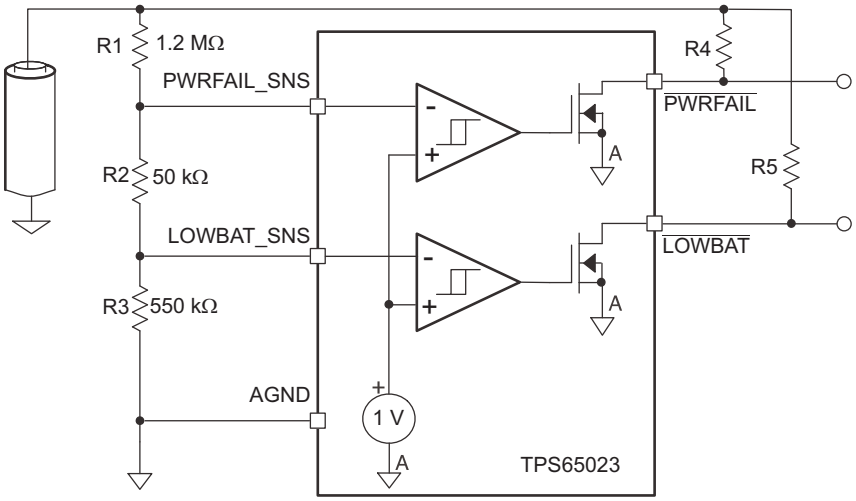

Figure 1. TPS65023 Comparators (Original Intended Use)

The comparators reference voltage and hysteresis specifications are given in document SLVS670 under the heading of Voltage Comparator Detectors.

The TPS65023 consists of three step-down converters and two linear regulators that default to the voltages needed by the DaVinci™ processor family. Each converter has a Power Good comparator that enables when the converter enables and toggles when the output voltage is 95% of the target voltage. The inverted output of each comparator is available as a flag in the memory map, accessible via I2C at register address 0x01 (PGOODZ register). In addition to the Power Good flags available in software, the $\overline{\text{INT}}$ pin is an open-drain output that is the logical AND of the Power Good comparator outputs for each enabled converter. When a converter is enabled and its output voltage is below 10% of the target voltage, the $\overline{\text{INT}}$ pin is pulled to ground. Figure 2 shows a logical representation of the $\overline{\text{INT}}$ function.

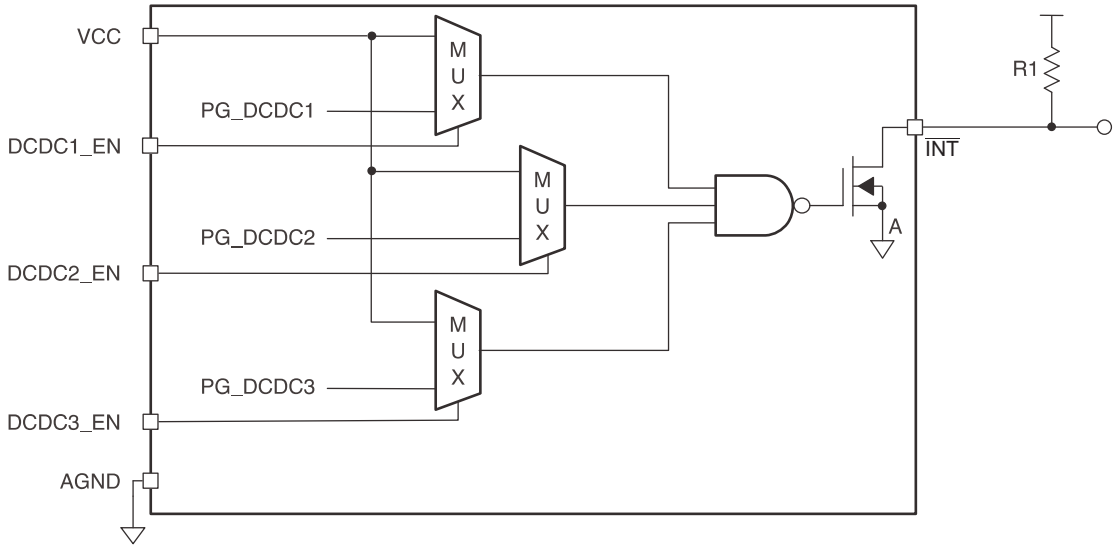

Figure 2. TPS65023 $\overline{\text{INT}}$ Pin Functional Diagram

To fulfill the DaVinci™ sequencing requirements, the 1.2-V output from the TPS65023 must be up prior to the 1.8-V and 3.3-V outputs. One way to achieve this is to connect the DCDC1 output directly to the DCDC2_EN, DCDC3_EN, and LDO_EN inputs. However, the digital V_{IH} of these input pins is 1.2 V minimum. This does not provide sufficient headroom in the event of transients on the DCDC1 output. But

one of the comparators previously described can be used to compare the 1.2-V output to the 1-V reference voltage. With the corresponding comparator output pulled up to VRTC, a voltage available whenever the V_{CC} voltage is present, and tied to the enables for the other converters and linear regulators, the sequencing requirements would be met. Figure 3 gives a schematic view of the connections to obtain the necessary sequencing .

NOTE: Not all TPS65023 pins are shown, only those needed for sequencing the converters.

Figure 4 shows the scope trace of the power up of DCDC1 and DCDC2, using the connections shown in Figure 3.

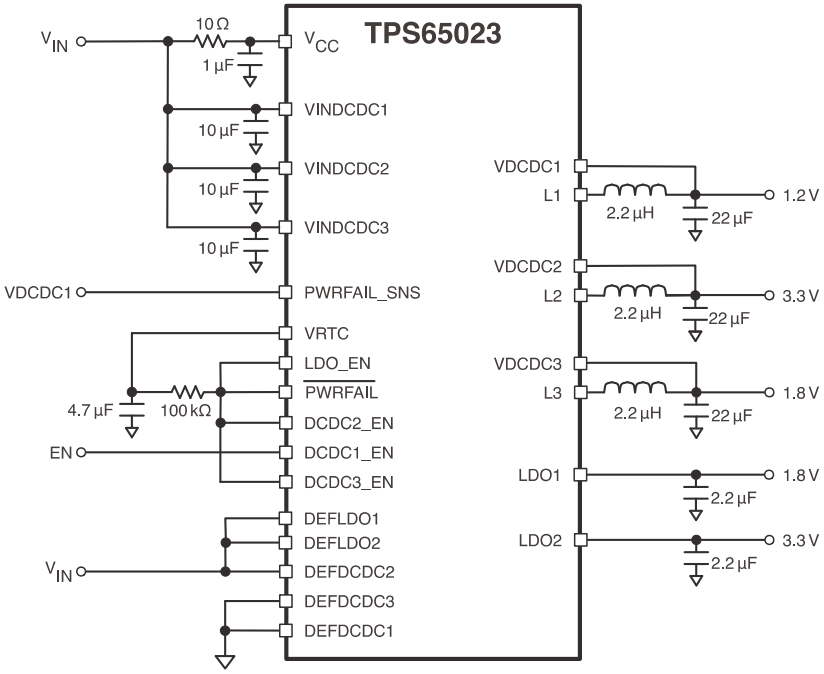

Figure 3. Sequencing Schematic

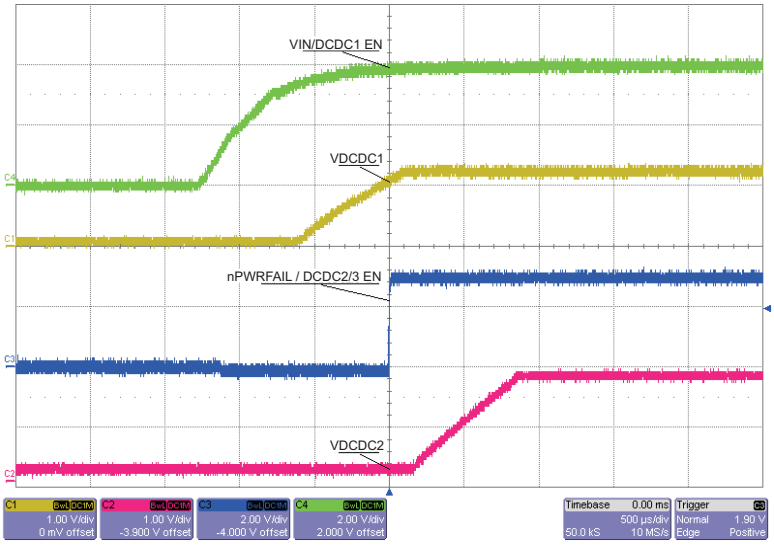

Figure 4. Sequencing Trace

Note in Figure 4 that DCDC2 is enabled before DCDC1 has reached the full 1.2 V (triggers at approximately 1 V). DCDC1 reaches 1.2 V prior to DCDC2 and DCDC3 ramping because of the delay time used to precharge to minimize inrush current, and this satisfies the DaVinci™ sequencing requirements.

The DaVinci™ reset requirement, that the $\overline{\text{RESET}}$ input be held low until all the voltages are available, can be met by using the Power Good logic that drives the $\overline{\text{INT}}$ pin on the TPS65023. Because $\overline{\text{INT}}$ stays low when an enabled converter is out of regulation, the $\overline{\text{INT}}$ pin can be pulled up to the 1.8-V converter ($\overline{\text{RESET}}$ on the DaVinci™ family is a 1.8-V input) and tied directly to $\overline{\text{RESET}}$. This works because the $\overline{\text{INT}}$ pin is low while DCDC1 ramps up. When DCDC1 hits approximately 1 V (still below valid regulation), DCDC2 and DCDC3 are enabled – thus holding $\overline{\text{INT}}$ low until all converters are within regulation. Figure 5 shows a full schematic for the TPS65023 connection to the DaVinci™ processors, and Figure 6 shows the scope trace with the $\overline{\text{INT}}$ signal (labeled nINT). The schematic in Figure 5 also shows a level shifter needed to enable the I2C from the DaVinci™ processor (1.8-V I/O) to the TPS65023 (3.3-V I/O).

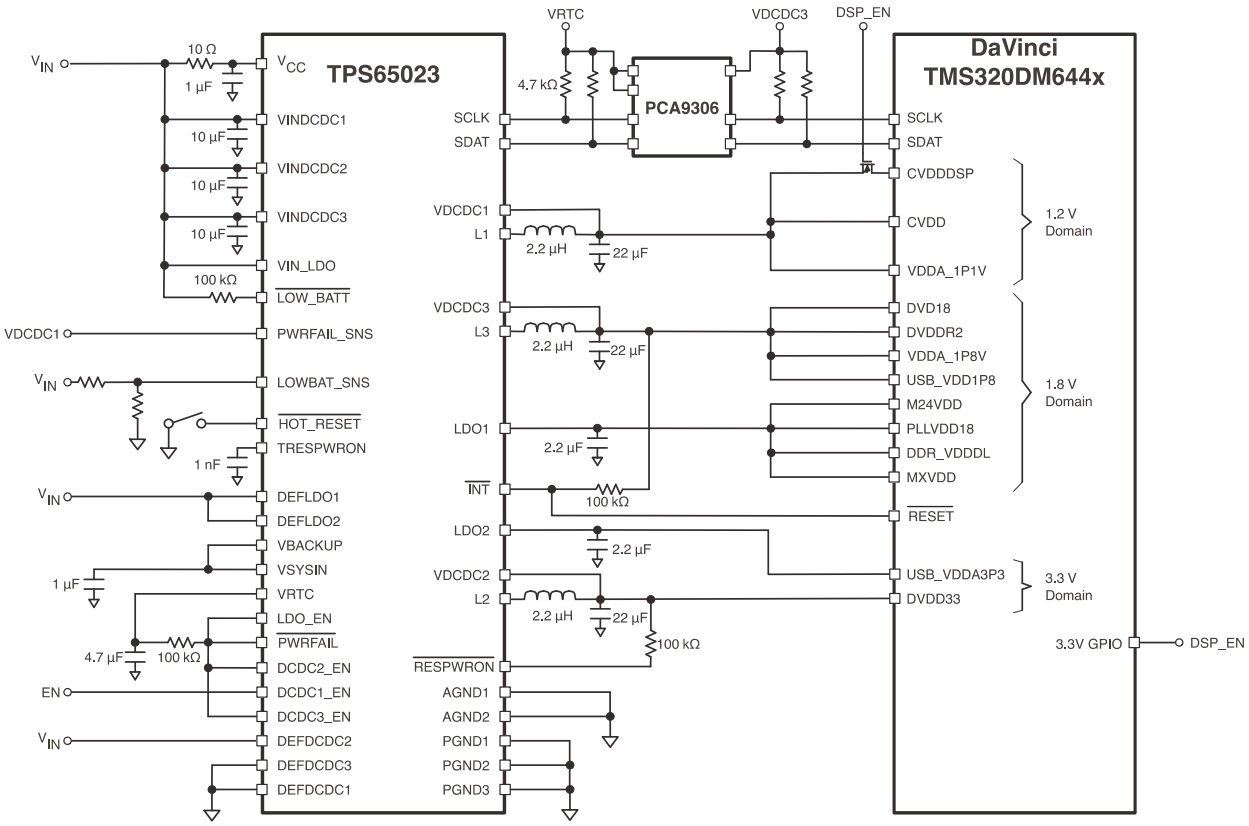

Figure 5. Full Schematic for Sequencing and Reset

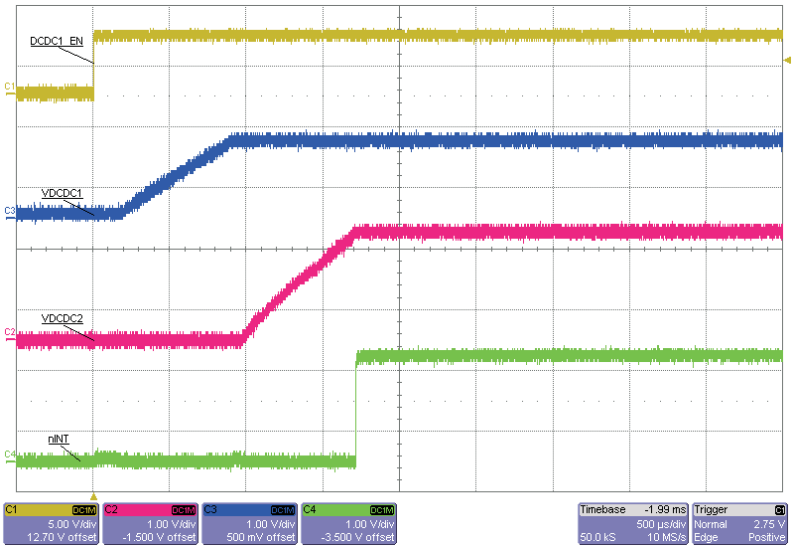

Figure 6. Scope Trace of $\overline{\text{INT}}$ Signal for DaVinci™ Reset

To summarize, the TPS65023 has two uncommitted comparators and a Power Good output that can be combined to fulfill the sequencing and reset requirements of the DaVinci™ family of processors. Using one comparator to monitor the output of the core voltage converter (DCDC1) and enable the other converters provides the necessary sequencing. Using the Power Good output, pin $\overline{\text{INT}}$, provides a simple way of holding the processor in reset until all the voltage rails are up and within regulation. This is a minimal design, eliminating the need for external voltage supervision and saving board space and component cost.

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