Powering the MSP430 from a High Voltage Input using the TPS62122

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Battery Power Applications

ABSTRACT

This reference design is presented to help designers and others who are using the MSP430 in a system with an input voltage range from 3.6V to 15V, and who are concerned with maintaining high efficiency and long battery life.

The TPS62122 is a highly efficient solution (up to 96% efficiency) capable of driving 75-mA loads. Its 11-µA quiescent current makes the TPS62122 an ideal choice in systems concerned over battery life.

Included in this document is a power solution for the MSP430. Power requirements, illustrated schematic, operation waveforms and bill of materials are included.

Contents

List of Figures

List of Tables

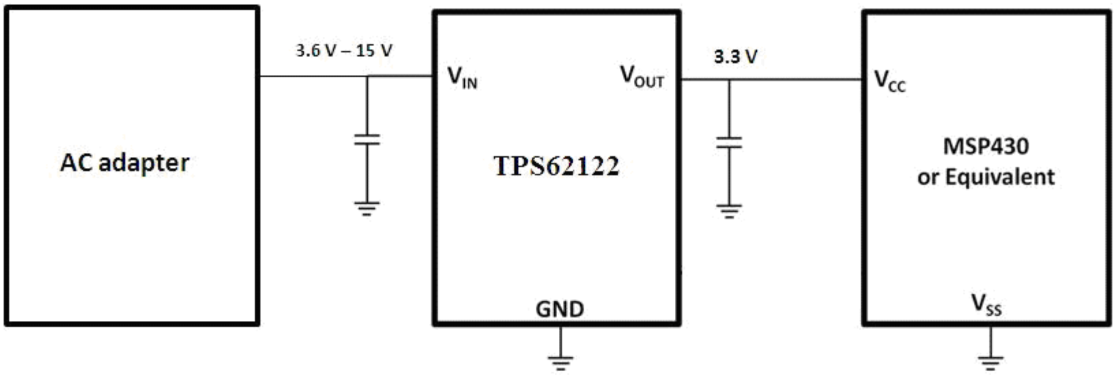

Figure 1. TPS62120 and MSP430 Simplified Block Diagram

1 Power Requirements

This reference design is for the MSP430 family of microcontroller devices and accounts for the voltage and current requirements as described herein. The MSP430 devices require only a single 3.3-V input; no sequencing is required. The operating input voltage for this reference design is 3.6V to 15V. This design is optimized for efficiency, high and wide input voltage range, small size, and low component count.

The power requirements for each MSP430 family are listed below in Tables 3 through 6. The power given is based on the amount of current the core consumes per megahertz (MHz). The Analog I_{MAX} column indicates the amount of current added if the additional functional blocks are used.

For more information and other reference designs, visit www.ti.com/processorpower.

Table 1. CC43 Family Power Requirements

DEVICE FAMILY	PIN NAME	VOLTAGE (V)		CPU I_{MAX} (µA/MHz)	ANALOG I_{MAX} (µA)	SEQUENCING ORDER	TIMING DELAY	COMMENTS
		MIN	MAX					
F613x, F513x	A_{VCC}, D_{VCC} (1)	1.8	3.6	250 (2)	I_{REF} = 140	n/a	n/a	+Maximum CPU speed of 20 MHz

(1) It is recommended to power A_{VCC} and D_{VCC} from the same source. A maximum difference of 0.3 V between A_{VCC} and D_{VCC} can be tolerated during power-up.

(2) Maximum value for CPU clocked at 20 MHz at 3 V shown. Actual value depends on supply voltage and MCLK/internal regulator settings. Does not include peripheral module supply current or GPIO source/sink currents, which must be added separately.

Table 2. MSP430x1xx Family Power Requirements (1)

DEVICE FAMILY	PIN NAME	VOLTAGE (V)		CPU I_{MAX} (µA/MHz) (2)	ANALOG I_{MAX} (µA)	COMMENTS
		MIN	MAX			
x11x1A	V_{CC}	1.8	3.6	350	Comp_A = 60	C11x1: 300 µA/MHz max
F12x	V_{CC}	1.8	3.6	350	Comp_A+ = 60	
F11x2, 12x2	V_{CC}	1.8	3.6	350	ADC10 = 1200, I_{REF} = 400	
F13x, 14x[1]	A_{VCC}, D_{VCC} (3)	1.8	3.6	560	Comp_A = 60, ADC12 = 1600, I_{REF} = 800	F13x, 14x: Comp_A, ADC12 F14x1: Comp_A
F15x, 16x, 161x	A_{VCC}, D_{VCC} (3)	1.8	3.6	600	Comp_A = 60, ADC12 = 1600, I_{REF} = 800, DAC12 = 1500	DAC outputs not loaded; DAC12 currents for a single DAC, max of two DAC12s in device)

(1) Additional 7-mA maximum required when writing/erasing Flash In-system.

(2) 8-MHz maximum CPU clock speed (ex. Imax_x11x1 = 8 MHz × 350 µA = 2.8 mA). $V_{CC} = D_{VCC} = A_{VCC}$ = 3 V. Actual value depends on supply voltage. Does not include peripheral module supply current or GPIO source/sink currents, which must be added separately.

(3) It is recommended to power A_{VCC} and D_{VCC} from the same source. A maximum difference of 0.3 V between A_{VCC} and D_{VCC} can be tolerated.

Table 3. MSP430x2xx Family Power Requirements[(1)]

DEVICE FAMILY	PIN NAME	VOLTAGE (V)		CPU I_{MAX} [(2)] (μA/MHz)	ANALOG I_{MAX} (μA)	COMMENTS
		MIN	MAX			
F20xx	V_{CC}	1.8	3.6	370	Comp_A+ = 60 ADC10 = 1200, ADC10_I_{REF} = 400 SD16_A + I_{REF} = 1700 RefBuffer = 600	20x1: Comp_A+ 20x2: ADC10 20x3: SD16_A
F21x1	V_{CC}	1.8	3.6	410	Comp_A+ = 60	
F21x2	A_{VCC}, D_{VCC}	1.8	3.6	350	Comp_A+ = 60 ADC10 = 1200, I_{REF} = 400	
F22xx	A_{VCC}, D_{VCC} [(3)]	1.8	3.6	550	ADC12 = 1200, I_{REF} = 400 OA = 290	22x2: ADC10 22x4: ADC10, 2 OAs OA currents for a single amplifier
F23x0	A_{VCC}, D_{VCC} [(3)]	1.8	3.6	550	Comp_A + = 60	
F23x, 24x[1], 2410	A_{VCC}, D_{VCC} [(3)]	1.8	3.6	445	Comp_A + = 60, ADC12 = 1000, I_{REF} = 700	224x1: Comp_A+ 23x, 24x, 2410: Comp_A+, ADC12
F241x, 261x	A_{VCC}, D_{VCC} [(3)]	1.8	3.6	560	Comp_A + = 60, ADC12 = 1000, I_{REF} = 700 DAC12 = 1500	241x: Comp_A+, ADC12 261x: Comp_A+, ADC12, two DAC12s DAC12 outputs not loaded; DAC12 currents for a single DAC

(1) Additional 7-mA maximum required when writing/erasing Flash In-system.
(2) 16 MHz maximum CPU clock speed (ex. Imax_20xx = 16 MHz × 370 μA = 5.90 mA). V_{CC} = D_{VCC} = A_{VCC} = 3 V. Actual value depends on supply voltage. Does not include peripheral module supply current or GPIO source/sink currents, which must be added separately.
(3) It is recommended to power A_{VCC} and D_{VCC} from the same source. A maximum difference of 0.3 V between A_{VCC} and D_{VCC} can be tolerated during power-up.

Table 4. MSP430x4xx Family Power Requirements[(1)]

DEVICE FAMILY	PIN NAME [(2)]	VOLTAGE (V)		CPU I_{MAX} (μA/MHz) [(3)]	ANALOG I_{MAX} (μA)	COMMENTS
		MIN	MAX			
x41x	A_{VCC}, D_{VCC}	1.8	3.6	350	Comp_A = 60	C41x: 300 μA/MHz max
FW42x	A_{VCC}, D_{VCC}	1.8	3.6	350	Comp_A = 60 Scan IF = 650	
F42x	A_{VCC}, D_{VCC}	1.8	3.6	500	SD16 + I_{REF} = 1550 Ref Buffer = 600	SD16 current is for a single A/D (three on device)
FE42x[a], 42x2	A_{VCC}, D_{VCC}	1.8	3.6	500	ESP430CE1 = 4900 Ref Buffer = 600	ESP430 current for 4-MHz operation
F43x[1], F44x	A_{VCC}, D_{VCC}	1.8	3.6	560	Comp_A = 60, ADC12 = 1600, I_{REF} = 800	
F42x0	A_{VCC}, D_{VCC}	1.8	3.6	520	SD16_A + I_{REF}=1800 Ref Buffer = 600 DAC12=1500	DAC12 output not loaded
FG42x0	A_{VCC}, D_{VCC}	1.8	3.6	560	SD16_A + I_{REF}=1800 Ref Buffer = 600 DAC12 = 1500, OA = 290	DAC12 output not loaded; OA current for a single amplifier (two OAs in device)

(1) Additional 7-mA maximum required when writing/erasing Flash In-system.
(2) It is recommended to power A_{VCC} and D_{VCC} from the same source. A maximum difference of 0.3 V between A_{VCC} and D_{VCC} can be tolerated.
(3) 8 MHz maximum CPU clock speed (ex. Imax_x41x = 8 MHz × 350 μA = 2.8 mA). (F47xx max CPU clock = 16 MHz) V_{CC} = D_{VCC} = A_{VCC} = 3 V. Actual value depends on supply voltage. Does not include peripheral module supply current or GPIO source/sink currents, which must be added separately. LCD current not included.

Table 4. MSP430x4xx Family Power Requirements[(1)] (continued)

DEVICE FAMILY	PIN NAME [(2)]	VOLTAGE (V)		CPU I_{MAX} (µA/MHz) [(3)]	ANALOG I_{MAX} (µA)	COMMENTS
		MIN	MAX			
FG43x	A_{VCC}, D_{VCC}	1.8	3.6	570	Comp_A = 60, ADC12 = 1600, I_{REF} = 800, DAC12 = 1500, OA = 490	DAC12 outputs not loaded; OA and DAC12 currents for a single amplifier/DAC (three OAs, two DACs in device)
FG46xx	A_{VCC}, D_{VCC}	1.8	3.6	740	Comp_A = 60, ADC12 = 1600, V_{REF} = 800, DAC12 = 1500, OA = 490	DAC12 outputs no loaded; OA and DAC12 currents for a single amplifier/DAC (three OAs, two DACs in device)
F47xx	A_{VCC}, D_{VCC}	1.8	3.6	560	Comp_A = 60, SD16_A + I_{REF} = 1700 Ref Buffer = 600	16 MHz max CUP frequency; SD16 current is for a single A/D (four on device)

Table 5. MSP430x5xx Family Power Requirements[(1)]

DEVICE FAMILY	PIN NAME	VOLTAGE (V)		CPU I_{MAX} (µA/MHz) [(2)]	ANALOG I_{MAX} (µA)	COMMENTS
		MIN	MAX			
F54xx	A_{VCC}, D_{VCC} [(3)]	2.2	3.6	348	ADC12_A = 220, I_{REF} = 190	18 MHz maximum CPU clock speed

(1) Additional 5-mA maximum required when writing/erasing Flash In-system.
(2) 16 MHz maximum at 3-V CPU clock speed. Actual value depends on supply voltage and MCLK/internal regulator settings. Does not include peripheral module supply current or GPIO source/sink currents, which must be added separately.
(3) It is recommended to power A_{VCC} and D_{VCC} from the same source. A maximum difference of 0.3 V between A_{VCC} and D_{VCC} can be tolerated during power-up.

2 Schematic, Waveforms, and Bill of Materials

2.1 Schematic

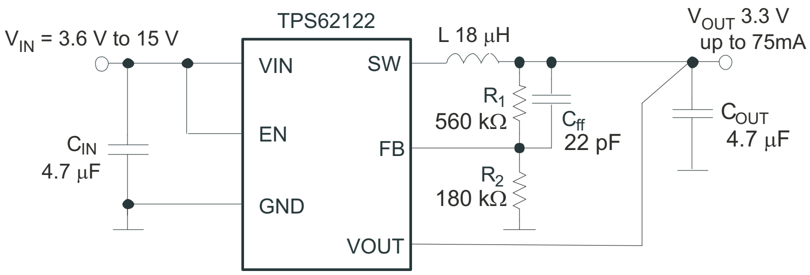

Figure 2. TPS62122 Schematic Diagram

2.2 Waveforms

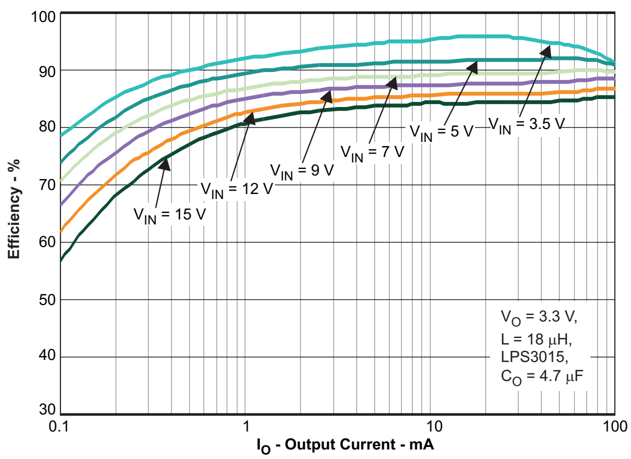

Figure 3. Efficiency vs Output Current I_{OUT} (V_{OUT} = 3.3 V)

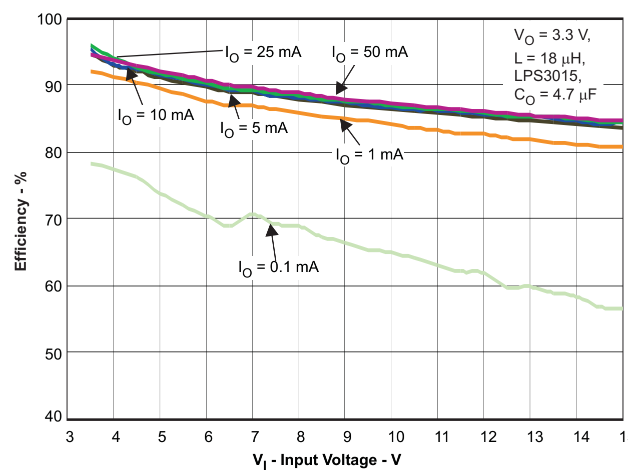

Figure 4. Efficiency vs Input Voltage V_{IN} (V_{OUT} = 3.3 V)

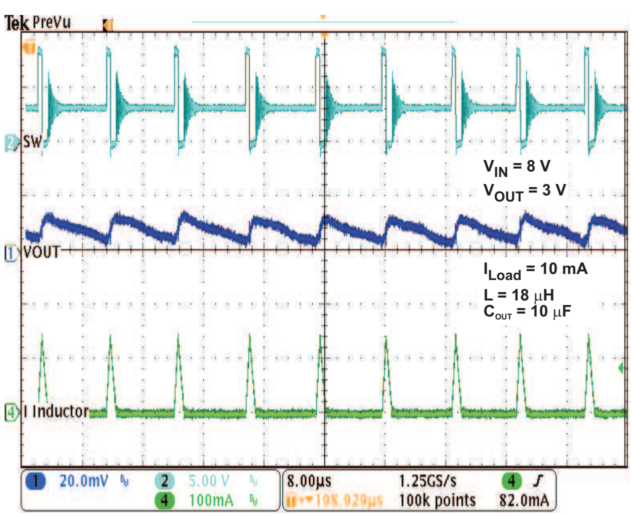

Figure 5. Typical Operation I_{OUT} 10 mA

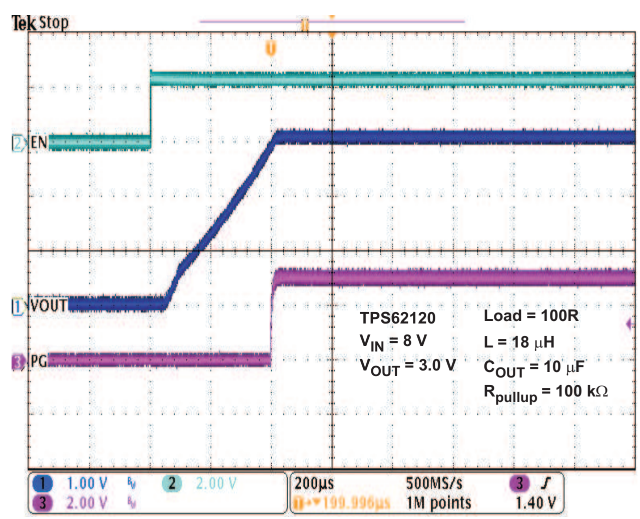

Figure 6. Power Good Output During Startup

2.3 Bill of Materials

Table 6 shows the bill of materials (BOM) for the 3.3 V_{OUT} design shown in Figure 2.

Table 6. TPS62122 List of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
1	C_{IN}	4.7μF	Capacitor, Ceramic, 25V, X5R, 20%	0805	GRM21BR61E475MA12L	muRata
1	C_{OUT}	4.7μF	Capacitor, Ceramic, 6.3V, X5R, 20%	0603	GRM188R60J475ME19D	muRata
1	C_{FF}	22pF	Capacitor, Ceramic, 50V, C0G-NP0, 5%	0603	Standard	Standard
1	L	18μH	Inductor, SMT, 0.56A, 750mΩ	3 mm x 3 mm	LPS3015-183ML	Coilcraft
1	R1	560kΩ	Resistor, Chip, 1/16W, 1%	0603	Standard	Standard
1	R2	180kΩ	Resistor, Chip, 1/16W, 1%	0603	Standard	Standard
1	U1	TPS62122	IC, 15-V, 75-mA High-Efficiency Buck Converter	8SOT-23	TPS62122DCN	TI

3 Further Applications

Multiple devices or subsystems can share the 3.3-V rail with the MSP430; this may require additional output current (exceeding 75mA). The TPS621xx family contains alternative devices capable of driving up to 3A. These devices also support higher input voltages, which better suits them for applications powered by 4 cell lithium-ion batteries. All of the devices shown in Table 7 support 3-V to 17-V inputs and drive output currents ≥ 500 mA. Table 7 lists the voltage, current, and packaging information for the various TPS621xx devices.

Table 7. TPS621xx Family Features

	TPS62120	TPS62122	TPS62130	TPS62140	TPS62150	TPS62160	TPS62170
I_{OUT} (Max) (A)	0.075	0.075	3	2	1	1	0.5
V_{IN} (Min) (V)	2	2	3	3	3	3	3
V_{IN} (Max) (V)	15	15	17	17	17	17	17
V_{OUT} (Min) (V)	1.2	1.2	0.9	0.9	0.9	0.9	0.9
V_{OUT} (Max) (V)	5.5	5.5	6	6	6	6	6
Iq (Typ) (mA)	0.011	0.011	0.017	0.017	0.017	0.017	0.017
Package Size	3mm X 3mm 8SOT-23	2mm X 2mm 6WSON	3mm X 3mm 16QFN	3mm X 3mm 16QFN	3mm X 3mm 16QFN	2mm X 2mm 8WSON	2mm X 2mm 8WSON

MSP430 devices have integrated power management systems to regulate internal startup and shutdown procedures. However, the power good and SGND pins available on the TPS62120 further increase the robustness of the system on startup. When VOUT has reached regulation (3.3V in this example), the TPS62120 signals the MSP430 through the PG (power good) pin. The TPS62120's SGND pin provides additional protection during the shutdown process. During shutdown mode, SGND provides a discharge path from the output capacitor to ground. This feature prevents lingering output voltages from discharging through the MSP430.

4 Conclusion

The TPS62122 efficiently powers an MSP430 in a system with input voltages ranging from 3.6V to 15V. The 11-µA quiescent current reduces overall power consumption and prolongs battery life in the application.

Similar devices within the TPS621xx family allow for even wider input voltage ranges and drive loads up to 3A. These higher current alternatives make room for additional subsystems to share the 3.3-V output power rail.

5 References

1. TPS62122 Datasheet – *15-V, 75-mA, 96% Efficiency Step-Down Converter* (SLVSAD5)
2. TPS62122 EVM User Guide – *TPS62122EVM User's Guide* (SLVU388)