Application Report
SLVA616–March 2014

Using the TPS62150 in a Split Rail Topology

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ABSTRACT

The need for creating a positive and a negative output supply rail for symmetrical loads is an everyday engineering need for powering loads such as operational amplifiers, sensors, and data converters. This application report demonstrates a method of generating a split rail supply with the TPS62150 easy-to-use, synchronous buck converter. The wide operating input voltage range of 3 V to 17 V is ideal for creating output voltages from ±0.9 V up to ±6 V. This application note is applicable to any of the TPS62130, TPS62140, and TPS62150 devices.

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1 Introduction

The objective is to design a non-isolated power supply which is capable of generating a positive and a negative supply rail from a 3.3- to 5-V input voltage rail for symmetrical loads, such as analog-to-digital converters or amplifiers. Specifically, this application note creates ±6-V output rails with 100-mA load current capability; the rails are then post regulated with LDOs for clean, very low noise ±5-V rails. See Figure 1 for the system block diagram.

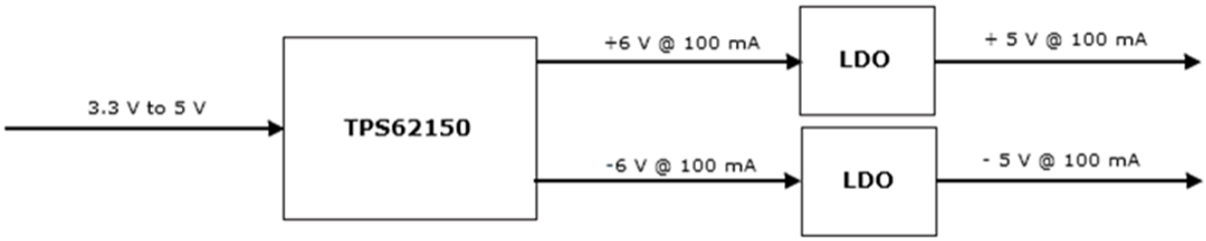

Figure 1. Block Diagram

2 Split Rail Topology

2.1 Concept

The split rail topology shown in Figure 2 is very similar to the inverting buck-boost topology. (See application report SLVA469 for a description on the inverting buck-boost topology with the TPS6215x). The IC ground is used as the negative output voltage (labeled as –Vout). What used to be the positive output in the buck configuration is used as GND. The positive rail is created with a standard, off-the-shelf coupled inductor, a rectifying diode (D1) and a second output capacitor. The feedback resistors are connected between the negative and the positive outputs to regulate the voltage across the positive and negative output rails.

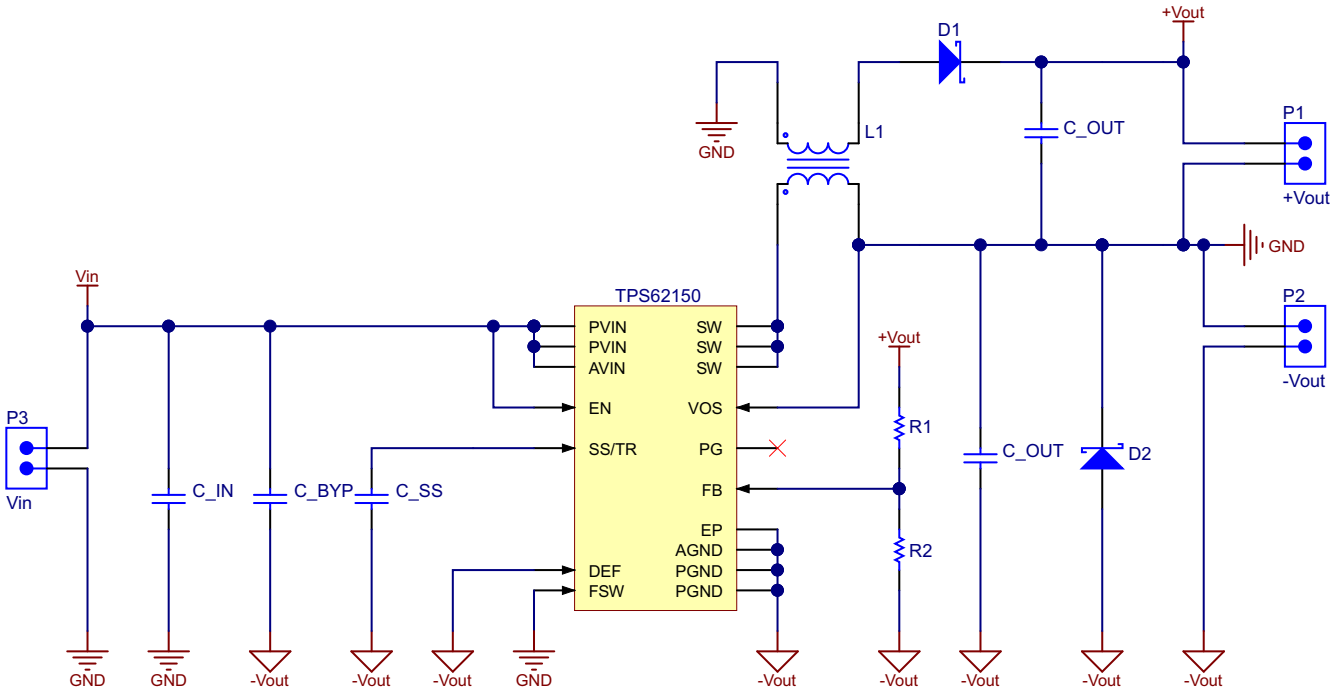

Figure 2. TPS62150 Split Rail Topology

2.2 Inductor Currents

Figure 3 shows the primary (ILo,neg) and secondary (ILo,pos) currents in the coupled inductor during continuous conduction mode (CCM) when assuming an ideal coupling coefficient (= 1). When the high-side MOSFET turns on, current ramps up in the primary winding. The secondary winding's diode blocks current flow in it during the on time. Once the high-side MOSFET turns off, the low-side MOSFET turns on to ramp down the inductor current. Now, the secondary winding's diode is forward biased and current flows equally in both windings.

To estimate the maximum rms current for the inductor, calculate Ipt1 to Ipt6 using Equation 1 to Equation 6, and substitute into, and solve Equation 7 and Equation 8. D is the duty cycle and calculated as: D = Vout / (Vout + Vin) where Vout refers to the absolute value of the negative output voltage, 6 V in this application report's circuit. Dmax refers to the maximum duty cycle which occurs at the lowest Vin. Dmax should be used to estimate the worst case rms current in the inductor.

Ipt2 must be less than the 1.4-A minimum forward current limit of the TPS62150. The difference between Equation 2 and Equation 1 is the inductor ripple current.

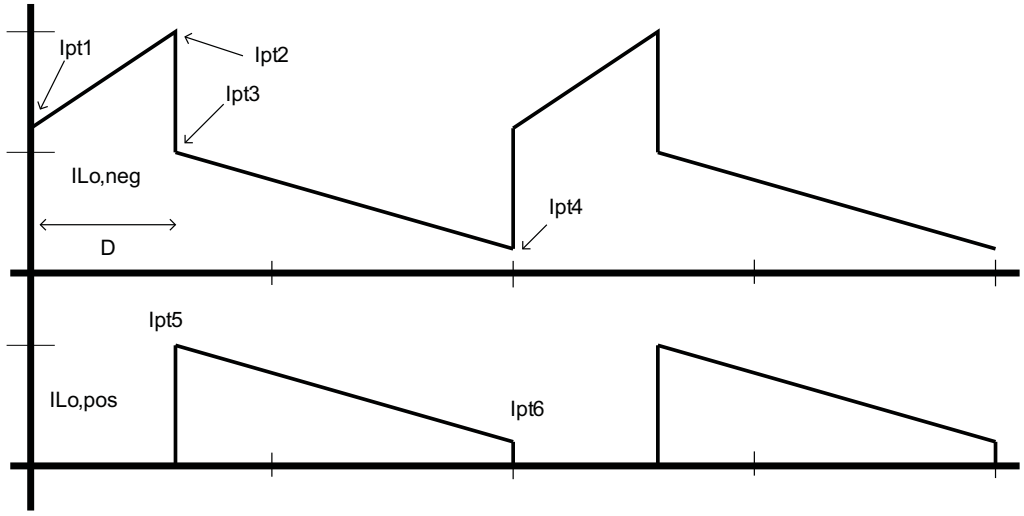

Figure 3. Current in Primary and Secondary Winding

$$Ipt1 = \frac{Iopos + Ioneg}{1 - Dmax} - \frac{Vinmin \times Dmax}{2 \times fsw \times L} \quad (1)$$

$$Ipt2 = Ipt1 + \frac{Vinmin \times Dmax}{fsw \times L} \quad (2)$$

$$Ipt3 = \frac{Ipt2}{2} \quad (3)$$

$$Ipt4 = Ipt3 - \frac{1}{2} \times \left(\frac{Vinmin \times Dmax}{2 \times fsw \times L} \right) \quad (4)$$

$$Ipt5 = Ipt3 \quad (5)$$

$$Ipt6 = Ipt5 - \frac{1}{2} \times \left(\frac{Vinmin \times Dmax}{2 \times fsw \times L} \right) \quad (6)$$

$$ILo,negrms = \sqrt{\frac{D}{3} \times \left(Ipt1^2 + Ipt1 \times Ipt2 + Ipt2^2 \right) + \frac{1-D}{3} \times \left(Ipt3^2 + Ipt3 \times Ipt4 + Ipt4^2 \right)} \quad (7)$$

$$ILo,posrms = \sqrt{\frac{1 - D}{3} \times \left(Ipt5^2 + Ipt5 \times Ipt6 + Ipt6^2 \right)} \quad (8)$$

2.3 Output Current Calculations

The average inductor current is affected by this topology. In the buck configuration, the average inductor current is equal to the average output current because the inductor always supplies current to the load during both the on and off times of the high-side MOSFET. However, in the split rail configuration, the load is supplied with current only from the output capacitors and is completely disconnected from the inductor during the on time of the high-side MOSFET. During the off time, both the primary and secondary inductor windings connect to each output cap and each load. Knowing that the off time is 1 – D of the switching period, then the average inductor current is:

$$I_{L(Avg)} = I_{OUT} / (1 - D) \quad (9)$$

Where Iout is the sum of Iopos and Ioneg:

$$I_{OUT} = Iopos + Ioneg \quad (10)$$

The duty cycle for a split rail converter is:

$$D = Vout / (Vout + Vin) \quad (11)$$

Where Vout refers to the absolute value of the negative output voltage, 6 V in this application report's circuit. The peak-to-peak inductor ripple current is calculated as:

$$\Delta I_L = Vin \times D / (Fsw \times L) \quad (12)$$

Where,

ΔI_L: Peak-to-peak inductor ripple current in the primary winding
D: Duty cycle
Fsw: switching frequency
L: inductance
Vin: Input voltage with respect to ground (instead of IC GND which is –Vout)

Finally, the maximum inductor current becomes:

$$I_{L(Max)} = I_{L(Avg)} + \Delta I_L / 2 \quad (13)$$

Rearranging this equation and setting $I_{L(Max)}$ to $I_{LIMF(Min)}$, the switching current limit as specified in the datasheet, gives:

$$I_{L(Avg)} = I_{LIMF(Min)} - \Delta I_L / 2 \quad (14)$$

This result is then used to calculate the maximum output current:

$$I_{OUT} = I_{L(Avg)} \times (1 - D) \quad (15)$$

For a negative output voltage of –6 V and a 3.3-µH inductor, Figure 4 shows the calculated maximum output currents at different input voltages with the TPS62150's minimum switch current limit of 1.4 A. Since DCS-control™ topology devices are not running on a fixed frequency control scheme, the switching frequency used for the calculations are 1 MHz (FSW pin set high) and 2 MHz (FSW pin set low) respectively, for taking some variation into consideration. The output current shown is between the positive and the negative power rail. For example, 200 mA on Figure 4 means 200-mA current flowing from +Vout to –Vout. The higher switching frequency circuit obtains a higher load current, because it has a lower inductor current ripple.

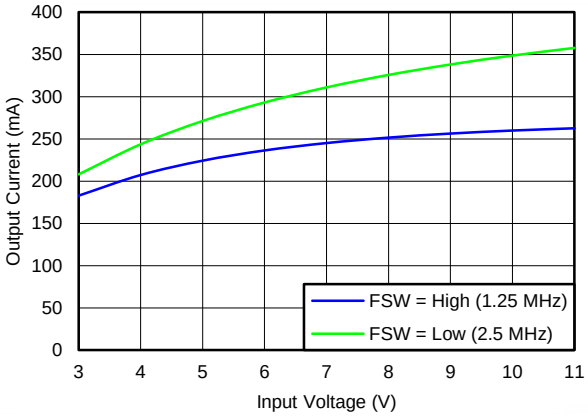

Figure 4. Output Current versus Input voltage

2.4 Vin and Vout Range

The input voltage that can be applied to a split rail converter IC is less than the input voltage that can be applied to the same buck converter IC. This is because the ground pin of the IC is connected to the negative output voltage. Therefore, the input voltage across the device is Vin to –Vout, not Vin to ground. Thus, the input voltage range of the TPS62150 is reduced to 3 V to (17 + –Vout), where –Vout is a negative value.

The output voltage range for both outputs is set by a voltage divider to the FB pin between +Vout and –Vout. Ground is not used in regulating the output voltage; rather, the voltage between the outputs is regulated. The voltage should be set to give at least 1.8 V and at most 12 V from +Vout to –Vout. See Diode Selection for more details on setting the output voltage.

3 External Component Selection

The inductor and output capacitor need to be selected based on the needs of the application and the stability criteria of the device. The selection criterion for the inductor and output capacitor is different from the buck converter. See Section 3.3, Selecting L and Cout for Stability for a discussion of stability.

3.1 Inductor Selection

When selecting the inductor value for the inverting buck-boost topology, the equations provided in Output Current Calculations should be used instead of the ones provided in the data sheet. $I_{L(Max)}$ should be kept below the minimum current limit value of the device (1.4 A) for a reliable design. Also, the inductor should have a saturation current above the maximum current limit of the device. The LPD4012-332MLB inductor from Coilcraft® is selected for the coupled inductor. Coilcraft offers many other off-the-shelf coupled inductors in a variety of standard values, saturation currents, and sizes, for example, MSD1260, MSD1278, MSD7243 and LPD3015. See Selecting L and Cout for Stability for the stability impact of the inductor selection.

3.2 Input Capacitor Selection

An input capacitor, C_IN and a bypass capacitor, C_BYP are required to provide a local bypass for the input voltage source. Low ESR input capacitors are best for input voltage filtering and minimizing interference with other circuits. For most applications, 10-µF ceramic capacitors are recommended from Vin to ground and from Vin to –Vout. The C_IN and C_BYP capacitor values can be increased without any limit, for better input voltage filtering.

C_BYP provides an AC path from Vin to –Vout. When Vin is applied to the circuit, this dV/dt across C_BYP from Vin to –Vout creates a current that must return to ground (the return of the input supply) to complete its loop. This current might flow through the internal low-side MOSFET's body diode and the inductor to return to ground. Flowing through the body diode pulls the SW pin and VOS pin more than 0.3 V below IC ground, violating their absolute maximum rating. Such a condition might damage the TPS62150 and is not recommended. Therefore a Schottky diode, D2, should be installed on the output and startup testing should be conducted to ensure that the VOS pin is not driven more than 0.3 V below IC ground when Vin is applied.

3.3 Selecting L and Cout for Stability

Since the VOS and FB pins connect to different voltages on the output, it is not possible to measure the full control loop with a bode plot. Load transient response is a good test for stability, as described in the SLVA381 application report.

The recommended nominal inductance and output capacitance values to use for this topology are in the range of 2.2 µH to 3.3 µH and from 44 µF to 100 µF, respectively. In this application report, a 3.3-µH inductor and two 22-µF capacitors are used per output rail.

In contrast to the buck topology, the inverting buck-boost topology contains a Right Half Plane (RHP) zero which significantly and negatively impacts the control loop response by adding an increase in gain along with a decrease in phase at a high frequency. This can cause instability. Equation 16 estimates the frequency of the RHP zero:

$$f_{RHP} = -(1 - D)^2 \times Vout / (D \times L \times I_{OUT} \times 2 \times \pi) \quad (16)$$

It is recommended to keep the loop crossover frequency to 1/10th of the RHP zero frequency. Doing this requires either decreasing the inductance to increase the RHP zero frequency or increasing the output capacitance to decrease the crossover frequency. Note that the RHP zero frequency occurs at lower frequencies with lower input voltages, which have a higher duty cycle. The RHP zero for a 3-V input voltage and the highest output current of 183 mA is at approximately 264 kHz.

3.4 Diode Selection

The D1 diode reverse voltage needs to be greater than the difference between the maximum input voltage and the negative output voltage. For the TPS62150, a 20-V diode covers the complete input voltage range of the device. For a more detailed description on the input voltage range in the split rail topology, see Section 2.4.

The D1 diode must be capable of handling the output current calculated from Equation 15. As well, the forward voltage drop of the D1 rectifying diode (which varies based on load current) offsets the output rails such that the magnitude of the positive output is always lower than the negative output. The coupling coefficient of the coupled inductor also affects this voltage difference between the outputs. A low forward voltage diode should be selected for D1 to keep this voltage difference to a minimum. Doing this allows the negative output to remain below its 6-V operating range while at the same time allowing the positive rail to be high enough to give the LDO enough headroom to sufficiently clean up the output voltage. To keep the negative output voltage (the output voltage seen by the device between the IC ground and the VOS pin) within the recommended 0.9- to 6-V operating range, the difference between the two output voltage rails has been reduced to 11.5 V for this application report. For measurement results on load regulation see Figure 10 and Figure 11.

The D2 diode is necessary to ensure that the VOS pin is not driven more than 0.3 V below IC ground when VIN is applied. During normal operation D2 is reverse biased; therefore a low-leakage Schottky diode should be selected. For a more detailed description, see Section 3.2.

3.5 Soft Start Capacitor Selection

Placing a small ceramic capacitor on the SS/TR pin to the IC GND (that is, –Vout) adjusts the soft start time of the TPS62150. The soft start capacitor is calculated using Equation 17:

$$C_{SS} = t_{SS} \times \frac{2.5\ \mu A}{1.25\ V}\ [F] \quad (17)$$

where

C_{SS} is the capacitance (F) required at the SS/TR pin and

t_{SS} is the desired soft-start ramp time (s).

Careful selection of the soft start capacitor is important because the device in the split rail topology has a significantly increased current flowing through the switching elements of the device during startup. Too short of a soft start time results in entering current limit operation during startup, which causes an overvoltage on the output rails if a light load is present. Voltage measurements during startup with the lightest applied load should be conducted to ensure the voltage on the outputs does not exceed the recommended ±6 V limit. In this application report, a 10-nF C_SS is used for a smooth startup.

3.6 Digital Pin Configuration (EN, PG, FSW, and DEF)

Because –Vout is the IC ground in this configuration, these pins must be referenced to –Vout instead of ground. See Section 2.2 in the application report SLVA469 for interfacing with these pins. The same level shifters can be used in the split rail topology.

4 Typical Performance and Waveforms

The application circuit shown in Figure 5 is used to generate the data presented in Figure 6 — Figure 12. The output capacitors used are 22-µF, 16-V, 0805, X5R ceramic capacitors. Loss of capacitance from the DC bias effect can be significant. Unless otherwise specified, Vin = 5 V and Vout = ±6 V.

Figure 6 shows the startup behavior in the split rail configuration. After EN is taken high, the device starts switching after about a 50-µs delay and both output rails rise with a slope controlled by an external capacitor connected to the SS/TR pin.

Figure 7 shows the shutdown behavior in the split rail configuration. After EN is taken low, the device stops switching and both output rails decline to 0 V, based on their load.

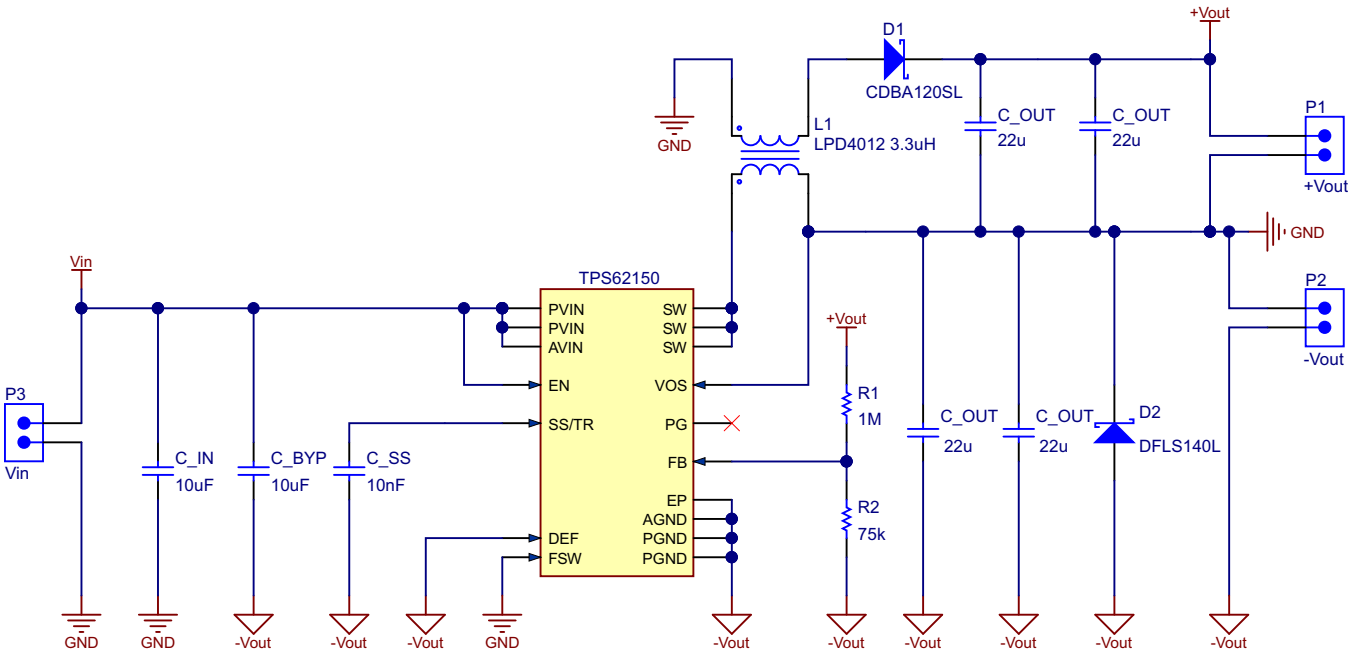

Figure 5. Schematic of the Tested Circuit

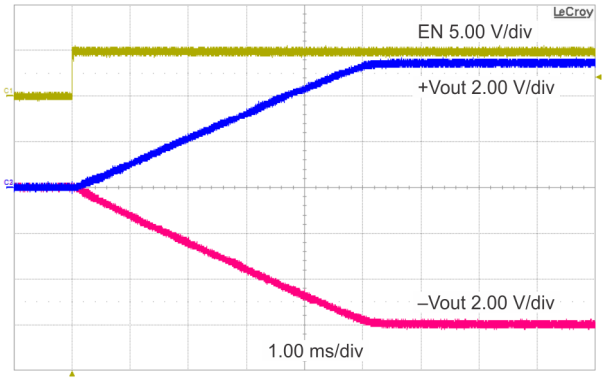

Figure 6. Startup Behavior in the Split Rail Topology into a 150-mA Load

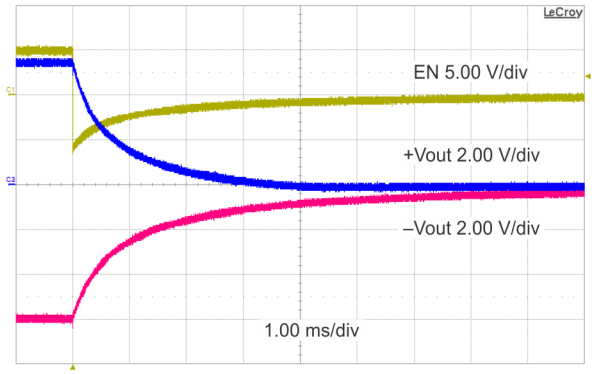

Figure 7. Shutdown Behavior in the Split Rail Topology with a 150-mA Load

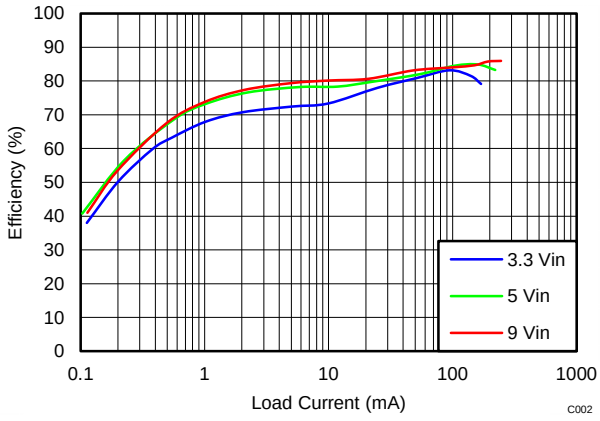

Figure 8. Efficiency versus Load Current

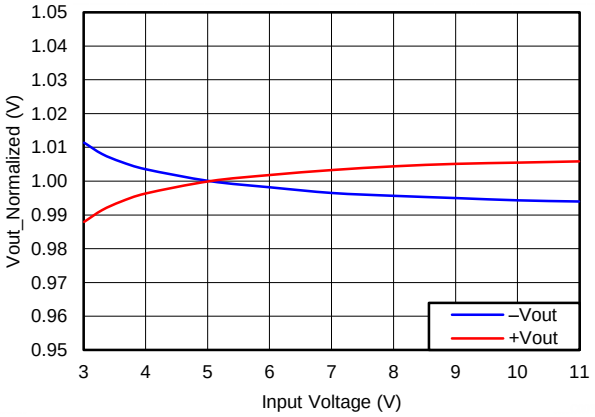

Figure 9. Line Regulation with 150-mA Load

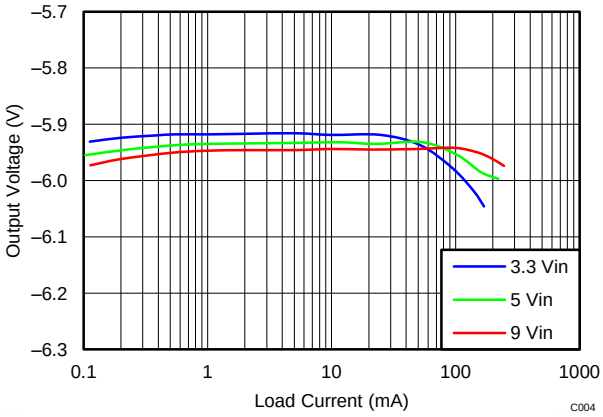

Figure 10. Load Regulation on –Vout

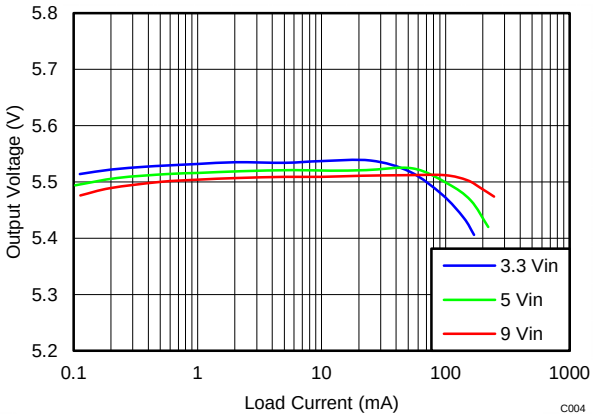

Figure 11. Load Regulation on +Vout

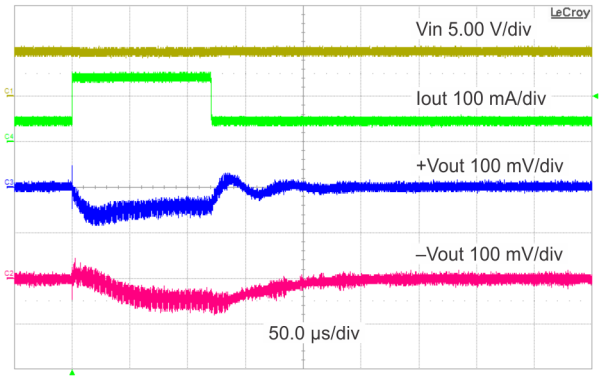

Figure 12. Load Transient Response 50 mA to 150 mA

5 Conclusion

The TPS62150 can be configured as a split rail converter to generate a positive and a negative output supply rail for symmetrical loads. The split rail topology changes some system characteristics, such as input voltage range and maximum output current. The desired 100-mA load current can be supported by the topology with an input voltage down to 3.3 V, keeping the negative output within the –6-V voltage limit of the IC while having approximately 5.5 V on the positive rail. This leaves enough headroom for ±5-V post regulation by an LDO. This application report explains the split rail topology and how to select the external components with the changed system characteristics. Measured data from the example design are provided. This report also applies to the TPS62130 and TPS62140 devices.

5.1 References

1. TPS62150 Datasheet (SLVSAL5)
2. *Using the TPS6215x in an Inverting Buck-Boost Topology* (SLVA469)
3. *Creating a Split-Rail Power Supply With a Wide Input Voltage Buck Regulator* (SLVA369)

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