

Practical Feedback Loop Analysis for Voltage-Mode Boost Converter

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Power Management

ABSTRACT

The boost converter offers a new set of complications in analysis and characteristics and can be a challenging converter to stabilize when operating with voltage-mode control. A Type III compensator is needed to design the loop for a voltage-mode boost converter operating in continuous conduction mode (CCM). Right-half-plane (RHP) zero has additional constraints on the design of loop compensation and crossover frequency, but they can be managed well as long as the RHP zero frequency is understood and placed properly by appropriate power stage component selection. This application report describes how to select the placement of poles and zeros with several rules.

Contents

1	Introduction	2
2	Boost Converter (Voltage Mode) Transfer Function Plots using TINA-TI™	4
3	Important Boost Characteristics	6
4	Compensation for Voltage-Mode Boost Converter	7
5	Voltage Mode Compensation Summary	9
6	Conclusion.....	12
	Appendix A. Voltage-Mode PWM Switch Model.....	13

Figures

Figure 1.	Boost Converter with Voltage Mode Control	2
Figure 2.	RHP Zero Frequency Changing Range with the Given Conditions.....	3
Figure 3.	Control-to-Output Transfer Function of the Voltage-Mode Boost Converter	4
Figure 4.	Effect of Changing Loads on the Control Characteristic of the Boost Converter	5
Figure 5.	Effect of Input Voltage Variation on the Control Characteristic of the Boost Converter.....	6
Figure 6.	Boost Converter with Feedback Amplifier and Duty-Cycle Modulator	7
Figure 7.	Feedback Block Diagram for the Power System of Figure 6	8
Figure 8.	Type III Compensator with Gain Curve.....	9
Figure 9.	Control-to-Output Transfer Function with the Given Parameters	9
Figure 10.	Appropriate Compensator Design Example	10
Figure 11.	Simulation Schematic with the Given Parameters	11
Figure 12.	Loop Gain and Phase Margin.....	11

1 Introduction

The boost converter belongs to the family of indirect energy transfer converters. The power process involves an energy-storing phase and an energy-release phase. During the on time, the inductor stores energy and the output capacitor alone powers the load. At the switch opening, the stored inductive energy appears in series with the input source and contributes to supply the output.

Figure 1 shows the boost converter with power stage elements and parasitic resistances. For the boost converter of Figure 1, the equation for the control-to-output transfer function is:

$$\frac{\widehat{v}_o}{\widehat{d}} = \frac{V_g}{D'^2} \times \frac{(1+sCR_C) \times \left(1 - s \frac{L_e}{R_L}\right)}{1 + \frac{s}{\omega_0 Q} + \frac{s^2}{\omega_0^2}} \quad (1)$$

Where the resonant frequency is given by:

$$\omega_0 = \frac{1}{\sqrt{L_e C}} \quad (2)$$

and the equivalent inductance is determined by the duty cycle:

$$L_e = \frac{L}{D'^2} \quad (3)$$

and

$$\omega_0 Q = \frac{R_{LOAD}}{L_e} \quad (4)$$

The Q of the filter is a complex combination of the parasitic resistance shown in the circuit and the load resistance. At light load, Q has its highest value and at full load, its lowest value.

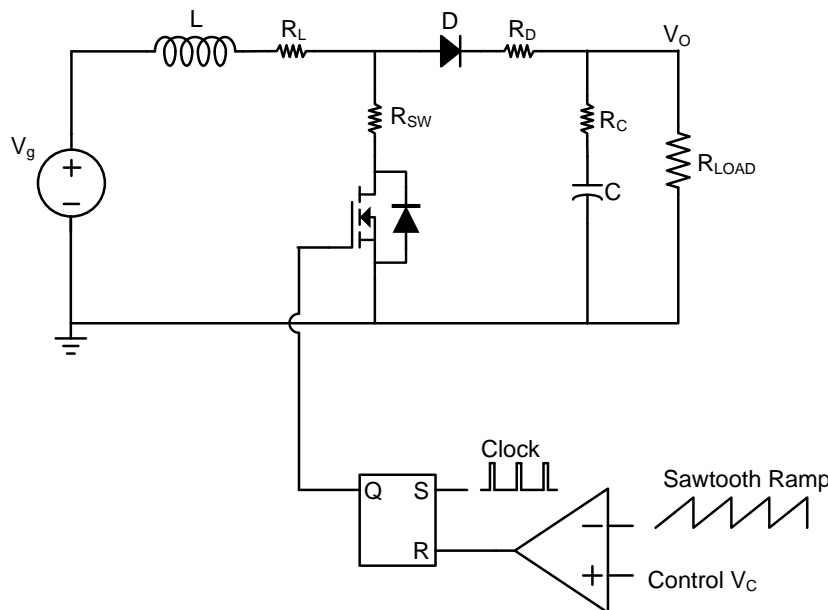


Figure 1. Boost Converter with Voltage Mode Control

The boost converter also adds a new complexity to the control problem, an RHP zero. This is caused by the fact that when the boost converter switch is turned on for a longer period of time, the inductor is disconnected from the load for a longer period of time. This means that the output initially drops, even though the control command is trying to make it increase.

This is exactly the characteristic of a class RHP zero. An increase in the command signal to the control system causes an initial decrease in the output response. After the time constant associated with the RHP zero has elapsed, the output starts moving in the same direction as the control. As a result, if you have a system with an RHP zero in the control-to-output transfer function, you cannot expect the control loop to respond immediately to change the output. The bandwidth of the loop must be limited to considerably less than the frequency of the RHP zero if the system is to be stabilized properly.

The frequency location of the boost converter RHP zero is:

$$f_{RHP} = \frac{R_{LOAD}(1-D)^2}{2\pi L} \tag{5}$$

Figure 2 shows the RHP zero frequency variation range depends on output loads ($R = R_{LOAD}$) with the design parameters ($V_{in} = 5\text{ V}$, $V_{out} = 18\text{ V}$, $L = 20\text{ }\mu\text{H}$).

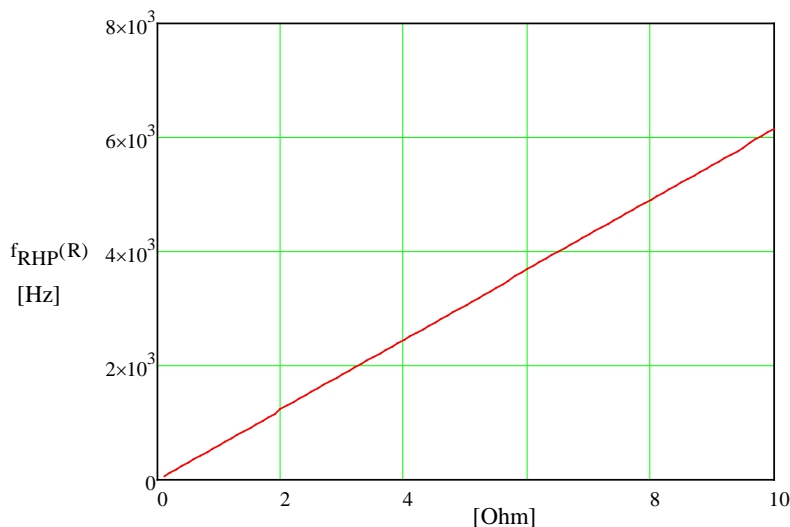


Figure 2. RHP Zero Frequency Changing Range with the Given Conditions

Note that the very existence of the RHP zero can be traced back to the fact that is the case where an actual LC post-filter doesn't exist on the output. Though, by using the canonical modeling technique, we have managed to create an effective LC post-filter, the fact that in reality there is a switch or diode connected between the actual L and C of the topology is what is ultimately responsible for creating the RHP zero.

The RHP zero can occur at any duty cycle. However, note that its location is at a lower frequency as D approaches 1 (that is, at lower input voltages). It also moves to a lower frequency if L is increased. That is one reason why bigger inductances are not preferred in boost topology. For this reason, it is called the moving RHP zero in boost converter.

The impacts of the moving RHP zero, as far as the magnitude of the transfer function is concerned, has the same effect as that of regular zero. However, it causes a 90 degrees phase delay in contrast to the 90 degrees phase boost in the case of a regular zero. Thus, the RHP zero increases the gain slope by 20 dB/decade while bringing down the phase by 90 degrees.

2 Boost Converter (Voltage Mode) Transfer Function Plots using TINA-TI™

Figure 3 shows the SPICE implementation of the small-signal model using a simple voltage-controlled voltage source as an error amplifier. On this small-signal boost, the voltage-controlled voltage source amplifies by about 69.5 dB the difference between a portion of V_{out} and the 2.5 V reference. In order to avoid running the circuit in a closed-loop configuration, we can install an LC filter featuring an extremely low cutoff frequency.

The error amplifier can be a simple voltage-to-voltage amplification device, that is, the traditional Op-Amp. This type of Op-Amp requires local feedback (between its output and inputs) to make it stable. Under steady DC conditions, both the input terminals are virtually at the same voltage, and this determines the output voltage setting. However, though both resistors of the voltage divider affect the DC level of the converter's output, from the AC point of view, only the upper resistor enters the picture. So the lower is considered just a DC biasing resistor, and therefore it is usually ignored in control loop (AC) analysis.

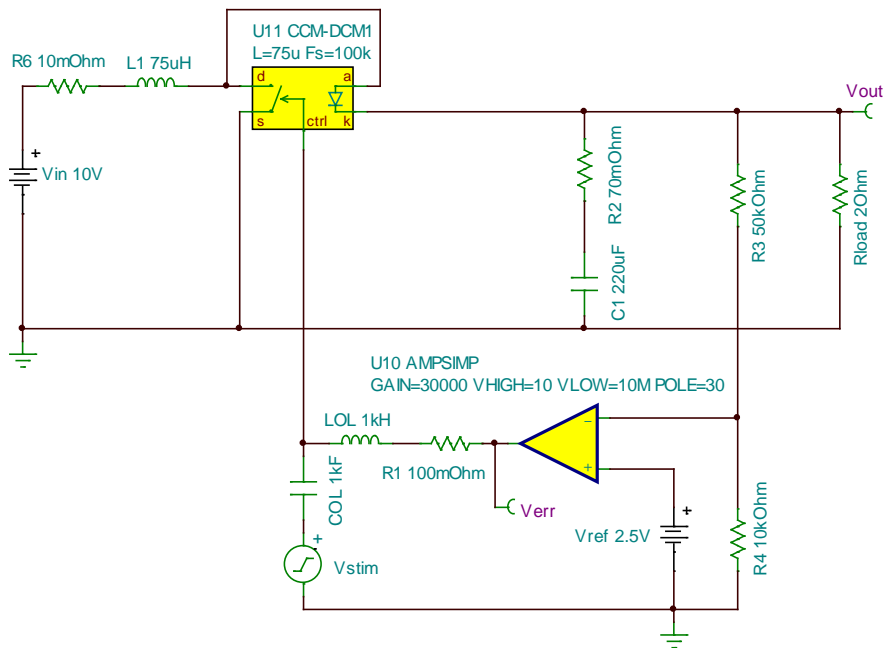


Figure 3. Control-to-Output Transfer Function of the Voltage-Mode Boost Converter

Figure 4 shows the effect on the gain and phase of the RHP zero with this small-signal model. At heavy loads, the RHP zero frequency is the lowest, and the phase delay is the greatest. At light loads, the RHP zero frequency is higher, and the converter is easier to control. Notice the large change in phase with different loads.

Notice that the expression for the RHP zero, given in Equations (1) and (5), shows that it is a function of the load, as shown in the plot of Figure 4, and of the value of the inductor chosen for the boost converter. If a large value of inductor is used, the RHP zero moves to a lower frequency, and the converter is more difficult to control. Reducing the value of the inductor increases the value of the RHP zero, and the converter is easier to control.

A typical value of inductor choice to make the converter controllable is one where the peak-to-peak ripple current in the inductor at full load is about 50% of the dc output current of the converter. Be sure that it is not necessary to reduce the inductor to such a small value that the converter operates in discontinuous conduction mode.

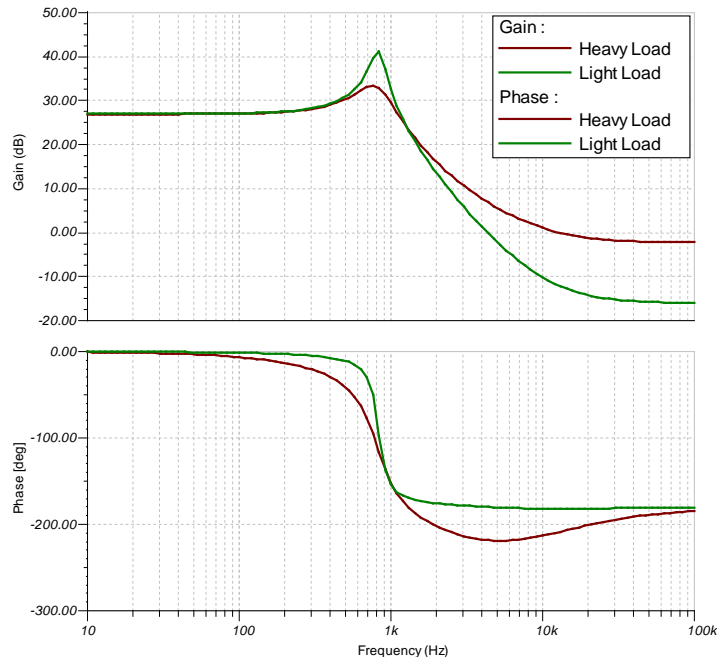


Figure 4. Effect of Changing Loads on the Control Characteristic of the Boost Converter

The boost converter also has a resonant frequency which changes with the input voltage as is shown in the control equations. Figure 5 shows graphically how the characteristics of the boost converter can vary dramatically with a wide input voltage. A guideline for converters with RHP zero is to design at the lowest input line and the maximum load. This causes the lowest value of RHP zero, and the lowest value of resonant frequency. However, when using voltage-mode control, the moving resonant frequency can create problems at different operating points, and the whole range of operation should be carefully checked with both predictions and measurements.

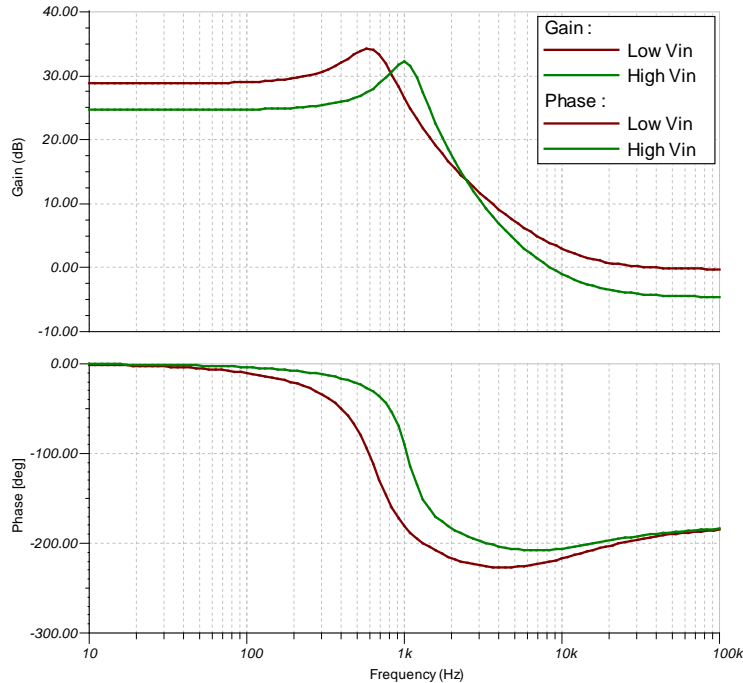


Figure 5. Effect of Input Voltage Variation on the Control Characteristic of the Boost Converter

More equations are created when the boost converter operates in discontinuous-conduction mode (DCM). When this happens, the double pole of the LC filter is heavily damped, and the converter exhibits essentially a single-pole response.

3 Important Boost Characteristics

Several important points to remember about the boost converter operating in CCM are as follows:

1. There is a double pole at the resonant frequency of the LC filter. The frequency of this double pole will move with the operating point of the converter since it is determined by the equivalent inductance of the circuit, and this is a function of duty cycle. At low line, the resonant frequency has its lowest value.
2. As with all switching power supplies, there is a zone in the control-to-output transfer function corresponding to the ESR of the output filter capacitor.
3. The boost converter has a right-half-plane zero which can make control very difficult. This RHP zero is a function of the inductor (smaller is better) and the load resistance (light load is better than heavy load). The bandwidth of the control feedback loop is restricted to about one-fifth the RHP zero frequency.

In discontinuous conduction mode, the resonant frequency of the filter is eliminated from the control characteristic. As with the buck converter, the LC filter is heavily damped in DCM operation and the converter has essentially a first-order response. This simplifies the control loop design, but it is not necessarily recommended as a solution to control problems. Higher power boost converters are usually designed to operate in CCM for efficiency reasons and the inductor should be chosen to optimize the converter efficiency, size, and thermal performance.

4 Compensation for Voltage-Mode Boost Converter

Now we are ready to design the feedback loop of the boost converter understanding the power stage and obtaining the proper transfer function. In order to control the boost converter, it is now necessary to design a feedback amplifier to compensate for the naturally-occurring characteristics of the power stage.

Figure 6 shows a typical boost converter circuit with feedback and the duty cycle modulator with voltage-mode control. The power stage is fed with a duty cycle pulse train and this is typically generated by comparing the output of a feedback error amplifier with a sawtooth ramp waveform. As the output voltage of the boost converter increases, the output of the inverting error amplifier decreases, and the duty cycle fed to the power supply input is decreased.

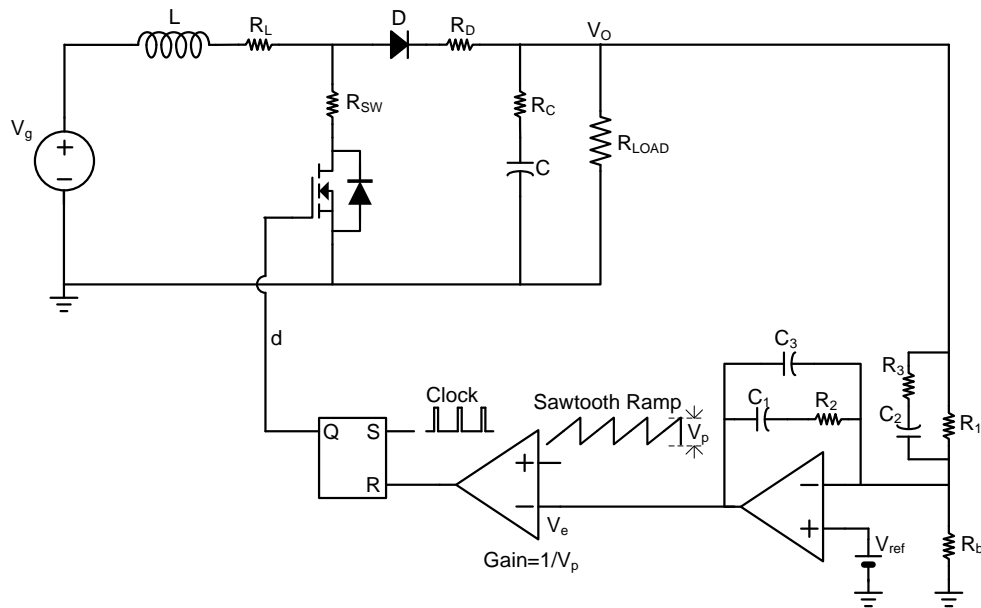


Figure 6. Boost Converter with Feedback Amplifier and Duty-Cycle Modulator

The system block diagram for this feedback arrangement is shown in Figure 7. This is something of an unusual arrangement since all of the gain blocks are in the forward path of the signal diagram. They are not separated into forward gain and feedback gain blocks. This is how a power supply feedback system actually works.

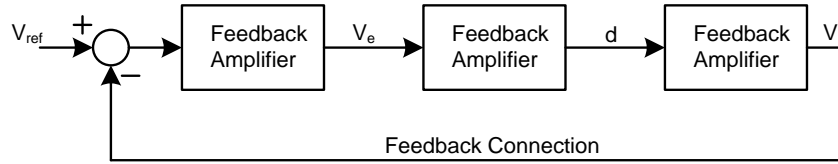


Figure 7. Feedback Block Diagram for the Power System of Figure 6

The output voltage is compared to the reference voltage, and the error between the two is amplified by the compensated operational amplifier. This signal is then fed into the duty cycle modulator and the resulting duty cycle is used to drive the gate of the power switch.

There are three gain blocks in [Figure 7](#). The modulator gain block is a very simple function, equal to the reciprocal of the height of the sawtooth ramp, as shown in [Figure 6](#). It has long been known that this naturally-sampled modulator function has no phase delay or frequency dependence, which is one of the reasons that it has been used successfully to control converters for many decades. It is still the predominant feedback scheme used in most power supplies today.

The compensator gain block is what we must now design in order to complete the loop around the control system. There are three different choices (Type I, Type II and Type III) of types of compensator that are used for switching power supply design. However, the Type III amplifier is the one used to compensate the voltage-mode boost converter operating in CCM.

[Figure 8](#) shows the conventional Type III compensation using voltage Op-Amp. There are two poles (f_{p1} and f_{p2} , besides the pole-at-zero f_{p0}) and two zeros (f_{z1} and f_{z2}) provided by this compensation. Note that several of the components involved play a dual role in determining the poles and zeros. So, the calculation can become fairly cumbersome and iterative. But a valid simplifying assumption that can be made is that C_1 is much greater than C_3 . So the locations of the poles and zeros are finally:

$$f_{p0} = \frac{1}{2\pi \times R_1 (C_1 + C_3)} \approx \frac{1}{2\pi \times R_1 C_1} \quad (6)$$

$$f_{p1} = \frac{1}{2\pi \times R_3 C_2} \quad (7)$$

$$f_{p2} = \frac{1}{2\pi \times R_2 \left(\frac{C_1 C_3}{C_1 + C_3} \right)} = \frac{1}{2\pi \times R_2} \left(\frac{1}{C_1} + \frac{1}{C_3} \right) \approx \frac{1}{2\pi \times R_2 C_3} \quad (8)$$

$$f_{z1} = \frac{1}{2\pi \times (R_1 + R_3) C_2} \quad (9)$$

$$f_{z2} = \frac{1}{2\pi \times R_2 C_1} \quad (10)$$

And the transfer function ($H(s)$) for the feedback block with Type III is

$$H(s) = \frac{(sC_2(R_1 + R_3) + 1)(sC_1 R_2 + 1)}{(sR_1(C_1 + C_3))(sC_2 R_3 + 1)\left(s\frac{C_1 C_3 R_2}{C_1 + C_3} + 1\right)} \approx \frac{(sC_2(R_1 + R_3) + 1)(sC_1 R_2 + 1)}{(sR_1 C_1)(sC_2 R_3 + 1)(sR_2 C_3 + 1)}, \quad \text{if } C_1 \gg C_3 \quad (11)$$

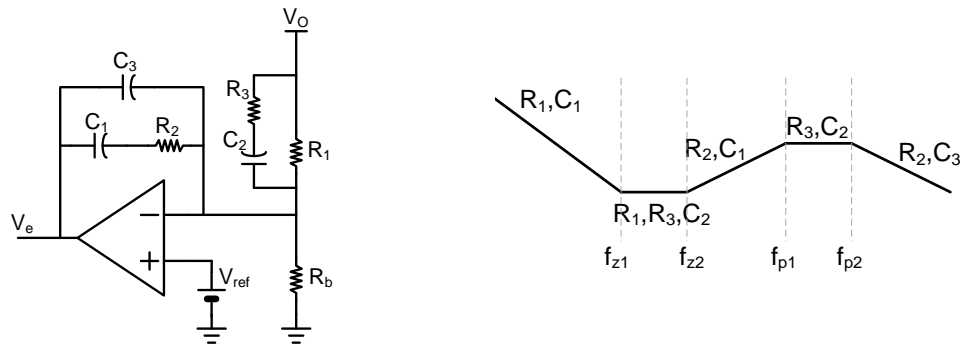


Figure 8. Type III Compensator with Gain Curve

5 Voltage Mode Compensation Summary

If we consider a practical feedback loop design with the following parameters ($V_{in} = 5\text{ V}$, $V_{out} = 18\text{ V}$, $I_{out} = 3\text{ A}$, $L = 20\text{ }\mu\text{H}$, $f_s = 200\text{ kHz}$), Figure 9 shows its control-to-output transfer function.

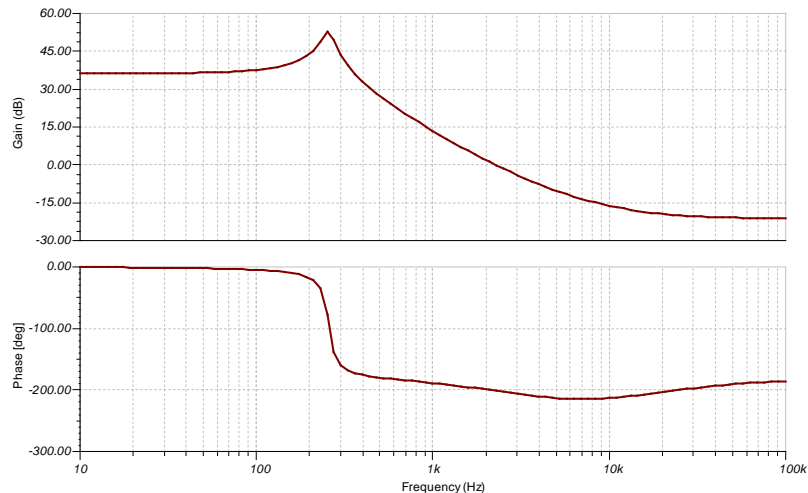


Figure 9. Control-to-Output Transfer Function with the Given Parameters

In selecting values for the Type III compensator, the following rules are applied when designing the compensator for the boost converters:

1. The first pole of the compensator is placed at the origin from an integrator.
2. Compensator zeros are placed around the power stage resonant frequency.
3. The second pole of the compensator is placed coincident with the ESR zero frequency of the power stage.
4. The third pole of the compensator is placed coincident with the RHP zero frequency of the power stage.
5. If the RHP zero or ESR zero is higher than half the switching frequency, the corresponding compensation pole is placed at half the switching frequency.

6. The crossover frequency should be less than about one-tenth the switching frequency.
7. The crossover frequency should be less than about one-fifth the RHP zero frequency.
8. The crossover frequency should be at least twice the resonant frequency.

Based on these rules, [Figure 10](#) shows an example for the compensator which has an appropriate shape, and usually a good phase margin.

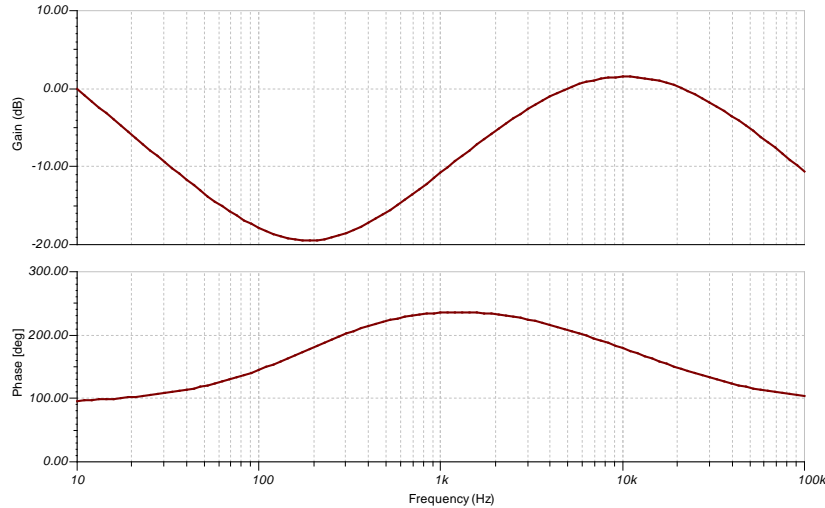


Figure 10. Appropriate Compensator Design Example

[Figure 11](#) and [Figure 12](#) show the schematic and the loop gain of applying these rules to a boost converter example. The converter switches at 200 kHz. The crossover frequency is limited to about 1.5 kHz passing it through with -1 gain slope, and the phase margin measured to be 45 degrees at this crossover frequency. The phase drops off quite rapidly to the right of the crossover frequency due to the approach of the RHP zero and its compensating pole, however, the loop gain is very good, as shown in [Figure 12](#).

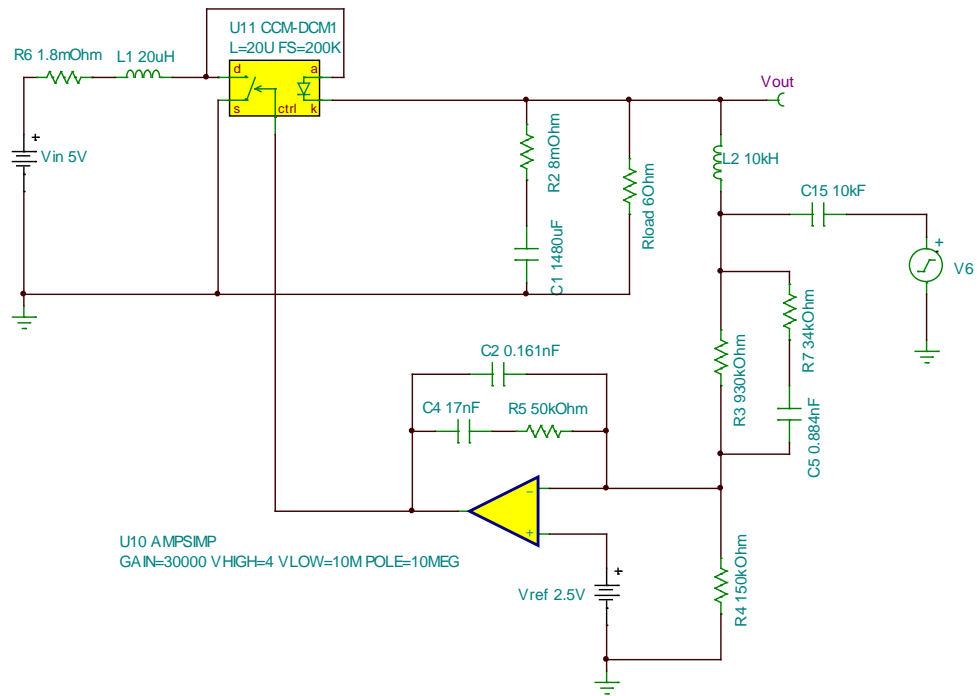


Figure 11. Simulation Schematic with the Given Parameters

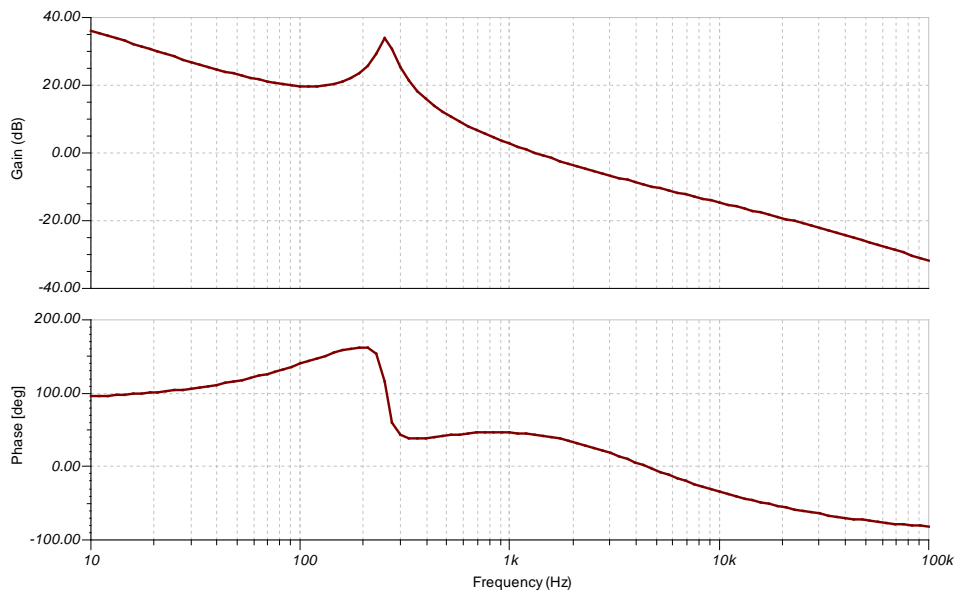


Figure 12. Loop Gain and Phase Margin

6 Conclusion

A Type III compensator is needed to design the loop for voltage-mode boost converter operating in CCM. The phase boost of this type of compensator is very helpful to offset the sharp phase drop that occurs after the resonant frequency of the power stage. RHP zero has additional constraints on the design of the loop compensation & crossover frequency, but they can be managed well as long as the RHP zero frequency is understood and placed properly by appropriate power stage component selection.

Appendix A. Voltage-Mode PWM Switch Model

The voltage-mode PWM switch model (transitioning from DCM to CCM automatically), which is used for TINA-TI™ simulation in this document is shown here:

```

*****
.SUBCKT PWMVM a c p d params: L=20u Fs=200k
*
* auto toggling between DCM and CCM, voltage-mode
*
Xd d dc limit params: clampH=0.99 clampL=16m
EVcp 6 p Value = { (V(dc)/(V(dc)+V(d2)))*V(a,p) }
GIap a p Value = { (V(dc)/(V(dc)+V(d2)))*I(VM) }
Ed2 d2X 0 value = { (2*{L}*{Fs}*I(VM)/(V(dc)*V(a,c)+1u)) - V(dc)
}
Xd2 d2X dc d2 limit2
VM 6 c
*
.ENDS
*****
.subckt limit d dc params: clampH=0.99 clampL=16m
Gd 0 dcx VALUE = { V(d)*100u }
Rdc dcx 0 10k
V1 clpn 0 {clampL}
V2 clpp 0 {clampH}
D1 clpn dcx dclamp
D2 dcx clpp dclamp
Edc dc 0 value={ V(dcx) }
.model dclamp d n=0.01 rs=100m
.ENDS
*****
.subckt limit2 d2nc d d2c
*
Gd 0 d2cx d2nc 0 100u
Rdc d2cx 0 10k
V1 clpn 0 7m
E2 clpp 0 Value = { 1-V(d)-6.687m }
D1 clpn d2cx dclamp
D2 d2cx clpp dclamp
Edc d2c 0 value={ V(d2cx) }
.model dclamp d n=0.01 rs=100m
.ENDS
    
```

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