Step-Down Converter with Input Overvoltage Protection

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ABSTRACT

DCDC converters typically are used to reliably and precisely regulate a supply voltage for an application circuit ensuring best operation performance of this application circuit. Very often the DCDC converters are powered from voltage rails where the voltage varies to a large extent. This voltage variation usually defines the topology of the DCDC converters and the parameters for its input circuit, mainly the power switches connected to the input voltage rails.

If a wide input voltage range needs to be covered, the power switches need to be able to handle the high current at low input voltage as well as the high voltage. This makes them big and expensive. Bigger switches also need more power for switching them – this directly translates in a potentially lower efficiency of the DCDC converter circuit. So, if the high voltage only occurs for short periods of time it may make sense to use a lower voltage rated DCDC converter. The converter can be perfectly sized for the nominal operating voltage range and an overvoltage protection circuit can be added at its input to handle the high voltage events. This overvoltage protection may clamp the voltage at the input of the DCDC converter, or just disconnect the DCDC converter from its supply. Disconnecting the supply is only possible if the supply of the application circuit can be maintained using a buffer.

In case the overvoltage events are predictable and the application circuit does not need to operate during the overvoltage events, the circuit could also be turned off by the overvoltage protection circuit. A nice example for such a configuration is the supply of any electronic circuit in a car which does not need to be active during starting of the engine. This application report describes a circuit which addresses the input overvoltage problem this way using a highly efficient and small step-down converter which is typically used in such environments. It also details the design and selection of the key components and provides measurement results showing the performance of the circuit.

1 Overview

In this example the overvoltage protection circuit is designed for a step-down converter implemented based on the TPS62130. The complete circuit is shown in Figure 1.
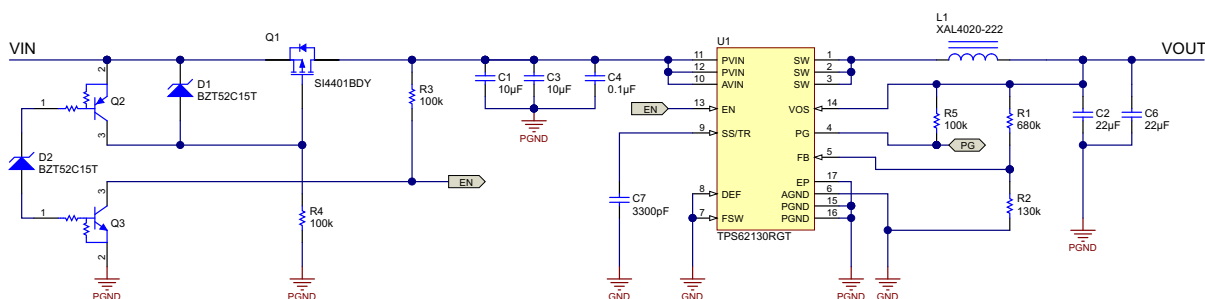

Figure 1. Circuit Schematic

The objective of this circuit is to provide an accurate 5-V supply at the output of the DCDC converter and disconnect the supply voltage of the converter in case the supply exceeds the maximum recommended operating input voltage of the TPS62130. An example of an implementation is in the TI reference designs library.

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2   Detailed Description

As shown in Figure 1, the circuit consists of a step-down converter design based on the TPS62130 in its default configuration. It is supplied through the overvoltage protection circuit. The overvoltage protection circuit is using a path transistor, Q_1, to connect the input voltage to the supply voltage at normal operation and disconnect it in the event of an overvoltage. For Q_1, a p-channel MOSFET is used. Q_1 must be able to block the input overvoltage, so its maximum drain-to-source voltage should be higher than the maximum overvoltage expected. Since Q_1 needs to handle the complete input current of the circuit, its on-resistance needs to be low enough to allow the input current flow without adding excessive losses and lowering the efficiency of the whole circuit too much. The on-resistance of Q_1, R_{DSonQ1}, for given maximum losses, P_{LQ1}, can be estimated using Equation 1:

$$R_{DSonQ1} = \frac{P_{LQ1}}{I_{IN\max}{}^2}$$

(1)

I_{INmax} is the maximum input current. The maximum input current is expected to flow at minimum input voltage.

The gate of Q_1 is pulled to ground with the resistor R_4 turning Q_1 on by default. The Zener diode D_1 protects the gate of Q_1 from overvoltage. So the Zener voltage of D_1, V_{ZD1} must be selected lower than the maximum gate-to-source voltage of the MOSFET Q_1. The maximum current flowing through D_1, I_{D1max} is limited by the resistance of R_4. It can be calculated using Equation 2:

$$I_{D1\max} = \frac{V_{IN\max} - V_{ZD1}}{R_4}$$

(2)

In this equation V_{INmax}, is the maximum input voltage expected, V_{ZD1} is the Zener voltage of the Zener diode, D_1 and R_4 is the resistance of the resistor R_4.

The losses in the Zener diode D_1, P_{LD1} can be calculated using Equation 3:

$$P_{LD1} = V_{ZD1} \cdot I_{D1}$$

(3)

The PNP transistor Q_2 is used to turn off the path transistor Q_1. If current is flowing through the base emitter diode it will discharge the gate of Q_1, turning Q_1 off. In this state, current is flowing through emitter and collector of Q_2. This current is limited by the resistance of resistor R_4. To calculate the resistance value for a given maximum current I_4 flowing through the resistor R_4, Equation 4 can be used. The maximum losses P_{LR4} in R_4 can be calculated using Equation 5:

$$R_4 = \frac{V_{IN\max}}{I_4}$$

(4)

$$P_{LR4} = R_4 \cdot I_4{}^2$$

(5)

I_4 has its maximum value at the maximum input voltage V_{INmax} at the overvoltage condition.

If there is current flowing through emitter and base of Q_2 this current is also flowing through base and emitter of Q_3. This is turning the NPN transistor Q_3 on with the effect that the enable signal of the DCDC converter TPS62130 is pulled low. This is turning the DCDC converter off and keeping it off. The current I_3 flowing through collector emitter of Q_3 is limited by the resistance of resistor R_3. This current is also the dominating current discharging the input capacitors of the DCDC converter TPS62130 in case the overvoltage protection circuit has disconnected the input voltage. It can be calculated using Equation 6:

$$I_3 = \frac{V_{IN}}{R_3}$$

(6)

V_{IN} is the voltage across the input capacitors of the TPS62130 and R_3 is the resistance value of the resistor R_3.

The threshold voltage at which the overvoltage protection circuit triggers is defined by the Zener voltage of the Zener diode D_2, the voltage drop across the emitter base diode of Q_2, the voltage drop across the base emitter diode of Q_3, and the voltage drop across the base resistors of Q_2 and Q_3. Compared to the voltage drop across the diodes, the voltage drop across the resistors close to the threshold voltage is low due to the low current flowing. This simplifies the calculation of the required Zener voltage V_{ZD2} of D_2 to Equation 7:

$$V_{ZD2} = V_{OVP} - V_{BEQ2} - V_{BEQ3} \tag{7}$$

V_{OVP} is the threshold voltage at which the overvoltage protection circuit triggers the supply voltage disconnect. The voltages V_{BEQ2} and V_{BEQ3} are the base emitter voltages of the bipolar transistors Q_2 and Q_3.

The current I_{D2} flowing through the Zener diode during overvoltage events is limited by the resistance of the base resistors at Q_2 (R_{BQ2}) and Q_3 (R_{BQ3}). It can be calculated using Equation 8:

$$I_{D2} = \frac{V_{IN} - V_{BEQ2} - V_{BEQ3}}{R_{BQ1} + R_{BQ2}} \tag{8}$$

This also allows calculation of the losses P_{LD2} the Zener diode D_2 needs to handle. Equation 9 shows the details:

$$P_{LD2} = V_{ZD2} \cdot I_{D2} \tag{9}$$

3   Example

In the current example the TPS62130 should be protected against overvoltage at its input. The protection should be capable of handling an input voltage up to a maximum of 40 V (V_{INmax}). The nominal operating input voltage in this example is in the range from 12 V up to 16 V. According to the TPS62130 datasheet (SLVSAG7), it can supply up to 3 A at its output, so its maximum DC input current is in this range. If the output voltage of the TPS62130 is programmed to 5 V, its maximum output power is 15 W. Assuming that the overvoltage protection circuit should not cause more than 1% in efficiency loss, the maximum power dissipated in the path transistor, Q_1, must be lower than 150 mW. All the control currents in the circuit should be in the range between 0.1 mA to 1 mA to keep the losses low and maintain a reasonable noise immunity of the protection circuit.

With those parameters the specification for Q_1 can be determined:

- R_{DSonQ1} = 17 mΩ (Equation 1)
- Minimum drain to source breakdown voltage for Q_1 (V_{INmax} = 40 V).

The resistor R_4 is limiting the current flowing through Q_2. For a given current of 0.4 mA, its parameters are calculated:

- R_4 = 100 kΩ (Equation 4)
- P_{LR4} = 16 mW (Equation 5)

The resistor R_3 is limiting the input capacitor discharge current. For a given resistance of 100 kΩ (same as R_4), the current is calculated:

- I_3 = 0.2 mA (Equation 6)

If the Zener diode D_1 is used to protect the gate of Q_1, the parameters for selecting D_1 are:

- V_{ZD1} is the maximum gate voltage of Q_1, 15 V is selected
- I_{D1max} = 0.25 mA (Equation 2)
- P_{LD1} = 3.75 mW (Equation 3).

The Zener diode D_2 defines the overvoltage protection threshold. Its parameters are calculated as follows:

- V_{ZD2} = 15 V (Equation 7, with 0.7 V for V_{BEQ2} and V_{BEQ3})
- I_{D2} = 1.2 mA (Equation 8 with 10 kΩ for R_{BQ2} and R_{BQ3})
- P_{LD2} = 18 mW (Equation 9)

4   Test Result

Figure 2 shows the voltages at different nodes in the overvoltage protection circuit of this circuit example at a line transient from 20 V to 12 V and back to 20 V. The transient time is 1 ms. The load current at the output of the DCDC converter is set to 2 A.
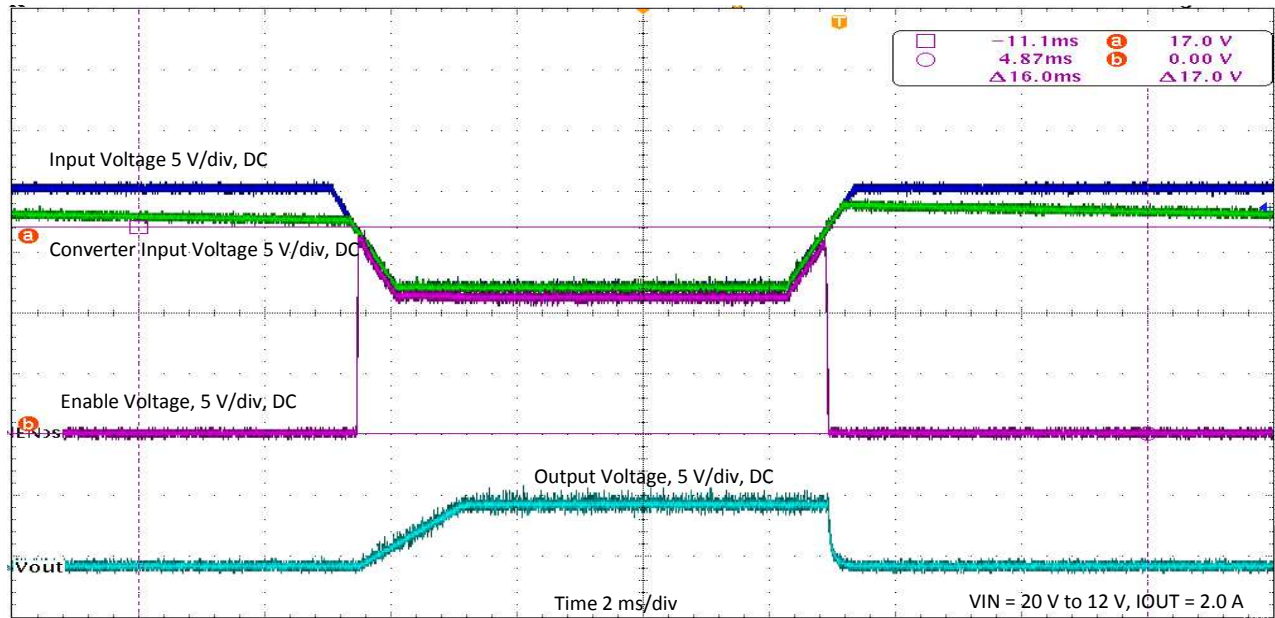

Figure 2. Line Transient

In Figure 2: the input voltage, the voltage at the input of the converter, the voltage at the EN pin of the converter, and the output voltage of the converter is shown. As soon as the input voltage drops below the overvoltage protection threshold, the converter is enabled. It starts operating and smoothly ramps up its output voltage to the nominal regulated voltage of 5 V. When the input voltage increases again and the overvoltage protection threshold is reached, the enable voltage is pulled low and the converter immediately stops operating. Since there is no significant load anymore during turn off of the path switch Q_1, the input voltage is still increasing until Q_1 is completely off. The maximum voltage reached during this turn off delay is still below the absolute maximum input voltage rating so the converter is protected.

5   Circuit Optimization

The threshold of the overvoltage protection circuit obviously was set to the correct voltage level. Above 16 V, the overvoltage protection circuit turns the TPS62130 off. But why did Q_1 not disconnect the converter at the same time?

For Q_3 to pull EN low, only a small current is required (I_3 = 0.2 mA). This means as soon as current starts to flow through the base emitter diode of Q_3 the collector current will be immediately at the required level to pull EN low. There is also no significant capacitance at the EN input of the TPS61230 which could delay turning off the converter.

At Q_1 this is different. It will not turn off until the gate voltage has decreased below its turn off threshold voltage, which is in the range of 1.5 V for a typical MOSFET. Since Q_1 needs to handle up to 3 A current at an on resistance in the range of 15 mΩ, a power MOSFET has been selected. Those MOSFETs have a significant capacitance from gate to source. This capacitance needs to be discharged below the turn off threshold voltage. The current drawn from the capacitor defines the speed of discharge. Higher current means faster discharge. The discharge current flows through Q_2 and is defined by the gain of Q_2 and the base current.

Due to a very low voltage across the base resistors of Q_2 and Q_3 at the time the input voltage reaches the overvoltage protection threshold, the base current in Q_2 is limited to a very low level. The gain of Q_2 further limits the discharge current for the gate of Q_1. This finally means Q_1 will be turned off with a significant delay.

If for Q_2, a transistor with a higher gain is selected, the turn off will be faster. Allowing a higher base current in Q_2 has a similar effect. To reduce the delayed turn off to a minimum, MOSFETs with a low gate charge should also be selected for Q_1. If the gate charge of Q_1 is further reduced by limiting the gate voltage to a lower value for turn on, it can be turned off faster as well. This can be done by using a Zener diode with a lower Zener voltage for D_1, for example using 5.1 V instead of 15 V.

Figure 2 shows the turning off of Q_1 with the modifications described. The input voltage change time in this experiment was set to 5 µs. The converter input voltage waveform does not show a significant overshoot anymore. Almost at the same time the converter is disabled, the supply voltage of the TPS62130 is disconnected from the input voltage and does not increase further.
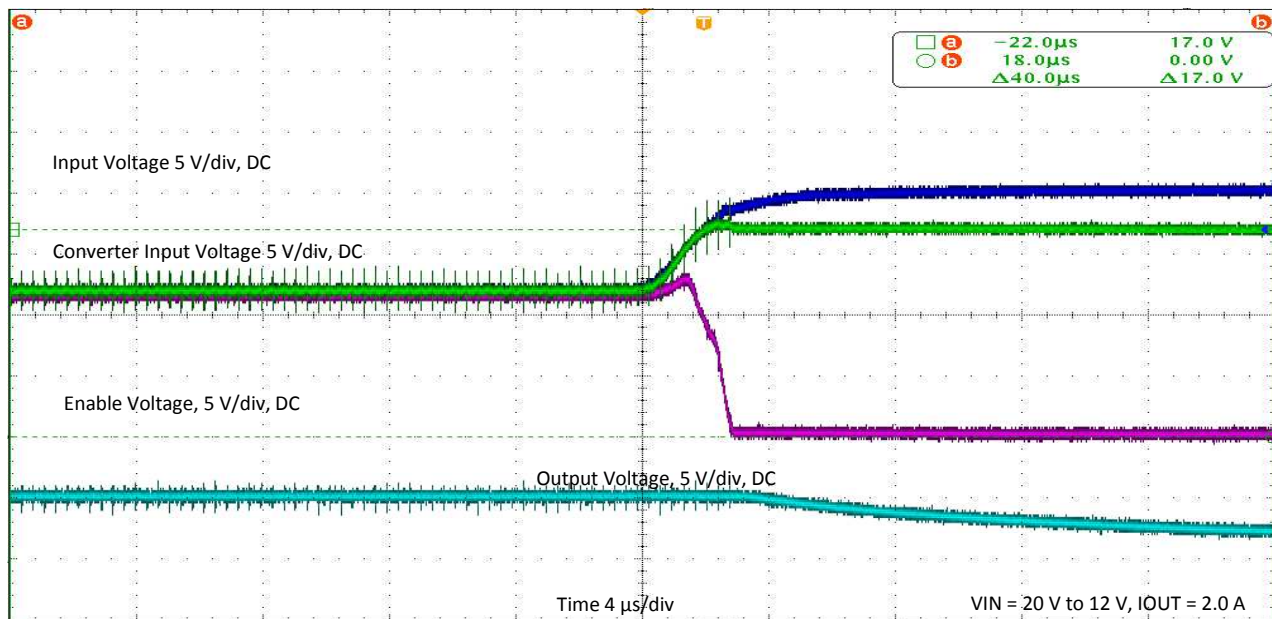

Figure 3. Line Transient after Optimization

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