How to Generate a Regulated VGL Supply Using the TPS65642A

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ABSTRACT

LCD panels require a single or bipolar supply for the source driver and two supply voltages for the gate driver. The TPS65642A device integrates two boost converters to supply the source driver and the positive supply voltage for the gate driver. The negative supply voltage for the gate driver is not integrated but is easily generated with an external negative charge pump which requires only a few additional components. This application note describes the design steps of a regulated negative charge pump and presents the load transient and load regulation measurement results.

Contents

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1   Application Circuit Description

Figure 1 shows the TPS65642A in a typical application circuit including the regulated negative charge pump with the following design parameters:

- Input Voltage V_I = 3.3 V
- Output voltage for source driver AVDD = 10 V at 400 mA
- Positive output voltage for gate driver VGH = 24 V at 10 mA
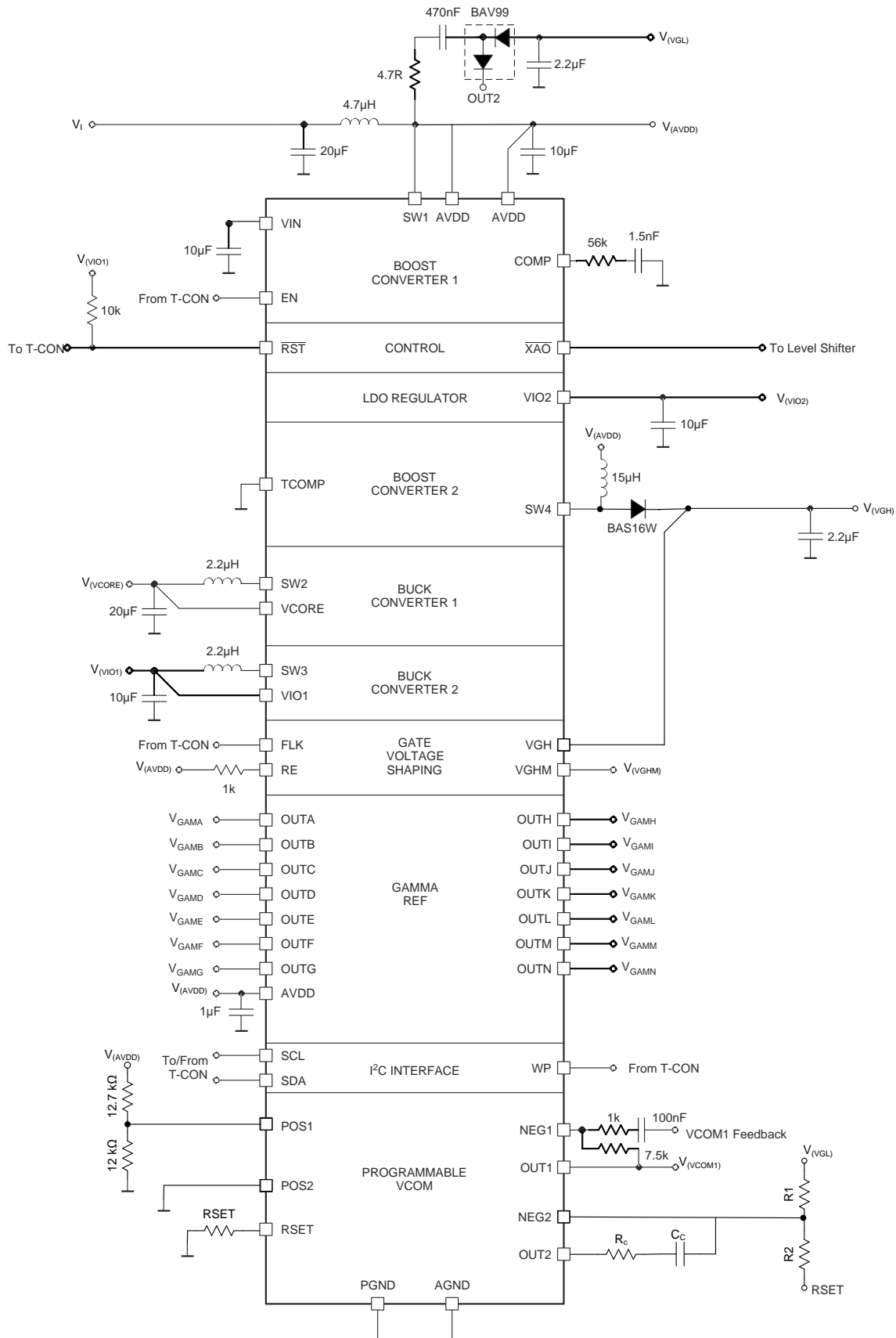- Negative output voltage for gate driver VGL = −2.2 V at 10 mA

Figure 1. TPS65642A Application Circuit With Regulated VGL

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1.1 Regulated VGL Supply

The negative rail for the gate driver VGL is not integrated in the TPS65642A but the requirements for this rail in terms of output current are limited. Therefore, the switch node of the AVDD Boost converter (SW1) is used to drive a negative charge pump in order to generate this rail. For the output regulation, one of the two VCOM amplifiers included in the TPS65642A is used (see Figure 2).
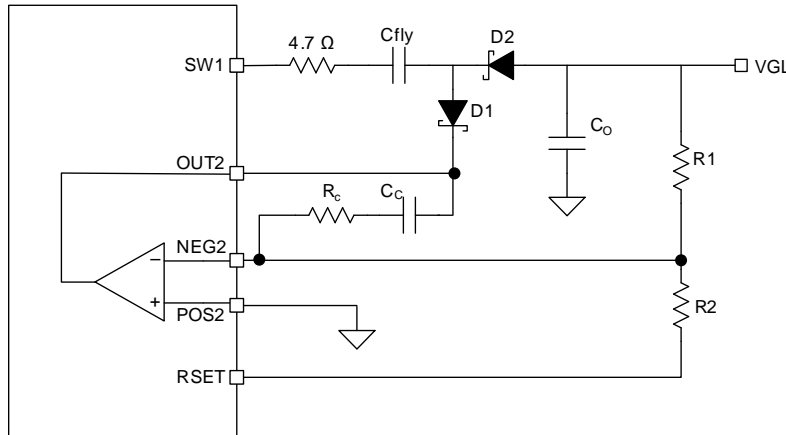
Figure 2. Regulated VGL

Figure 3 shows the basic configuration of a negative charge pump which operates as follows:

- First, the switch node is high and the flying capacitor Cfly charges up to a voltage of V_I - V_F through the diode D1

- Then in the second phase, the switch node which is the positive terminal of the flying capacitor is low and the negative terminal of the flying capacitor becomes $-V_I + V_F$. This causes D1 to block and D2 to open, allowing the flying capacitor to discharge through the output capacitor. This gives an output voltage
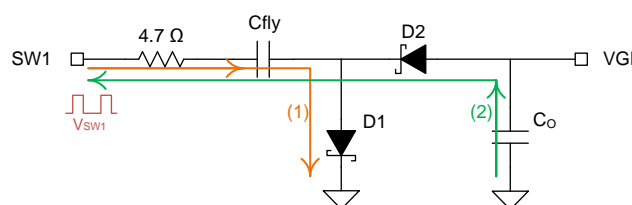
$$V_{(VGL)} = -V_I + 2V_F$$

(1)

Figure 3. Negative Charge Pump Basic Operation

To regulate the output of the negative charge pump, one of the VCOM amplifiers is used as an error amplifier. The output voltage is fed back through R1 and R2 to the error amplifier that controls the current flowing in the flying capacitor so that the output voltage is regulated at the desired value.

V_{GL} is set with the resistors R1 and R2 and is given by Equation 2,

$$V_{(VGL)} = -\left(\frac{R1}{R2}\right)V_{(RSET)}$$

where

- $V_{(RSET)}$ = 1.25 V is the voltage on the RSET pin. (2)

A series R-C network connected between the VCOM negative input pin and its output pin is added as shown in Figure 2 for the feedback loop compensation.

1.1.1 Component Requirements

The main elements of this circuit are: the flying capacitor, the output capacitor, and the diodes. The size of the flying capacitor determines how much output current the charge pump can deliver without drop of the output voltage. If the flying capacitor is too small, the output voltage will drop under heavy load. Equation 3 permits to estimate the size of the effective capacitance. A 2.2 Ω to 10 Ω resistor is added in series with the flying capacitor to reduce current spikes on the switch node.

$$V_{Cfly(PP)} = \frac{I_O}{2f(Cfly)}$$

where

- I_O is the negative charge pump output current.
- Cfly is the negative charge pump flying capacitance.
- f = 1.2 MHz or 750 kHz is the switching frequency of Boost1 and the negative charge pump. (3)

The diodes D1 and D2 need to fulfill the following requirements:

- Average forward current $I_F \geq I_O$
- Peak forward current $I_{FRM} \geq 2I_O$
- And reverse voltage $V_R \geq |V_{GL}|$.

The output capacitor helps reduce and smooth out the output voltage and also defines the startup time for the negative charge pump. The effective capacitance is determined as follows:

$$V_{(VGL)(PP)} = \frac{I_O}{2fC_O}$$

where

- I_O is the negative charge pump output current.
- C_O is the negative charge pump output capacitance.
- f = 1.2 MHz or 750 kHz is the switching frequency of Boost1 and the negative charge pump. (4)

2   Application Example

2.1   Component Selection

Using Equation 1 through Equation 4, the components values are determined as shown in Figure 4. From Equation 3 and Equation 4 a minimum capacitance of 42 nF is estimated for C_O and Cfly assuming a ripple of 100 mV. 330-nF capacitors were used instead to account for the dc bias effect and allow higher output currents. Rearranging Equation 2 to Equation 5 permits to select R1 = 82 kΩ and R2 = 45 kΩ which gives a nominal output voltage of V_{GL} = –2.21 V.

$$R1 = -\left(\frac{V_{(VGL)}}{V_{(RSET)}}\right) R2 = -\left(\frac{-2.2}{1.213}\right) R2 = (1.814) R2$$

(5)
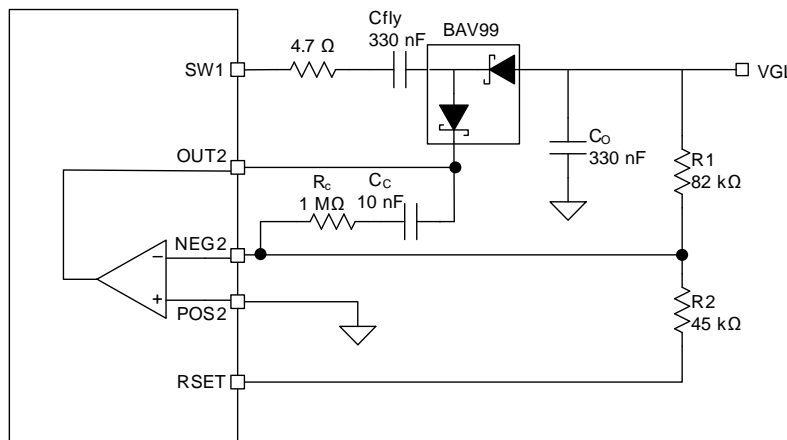
Figure 4. Regulated VGL

2.2   Performance Evaluation

The results of the performance evaluation from the regulated VGL circuit of Figure 4 are presented in this section. Figure 5 shows that the VGL charge pump is stable under a load transient from <1 mA to 20 mA. Figure 6 shows the load regulation curve which indicates less than 0.5% variation of the VGL voltage at 50 mA load.
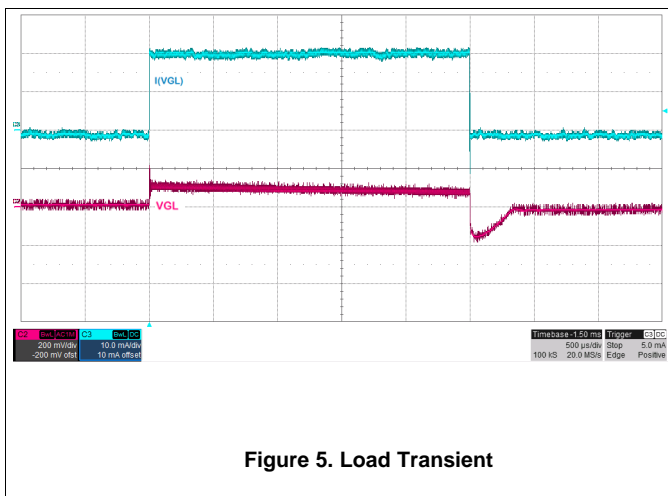
Figure 5. Load Transient
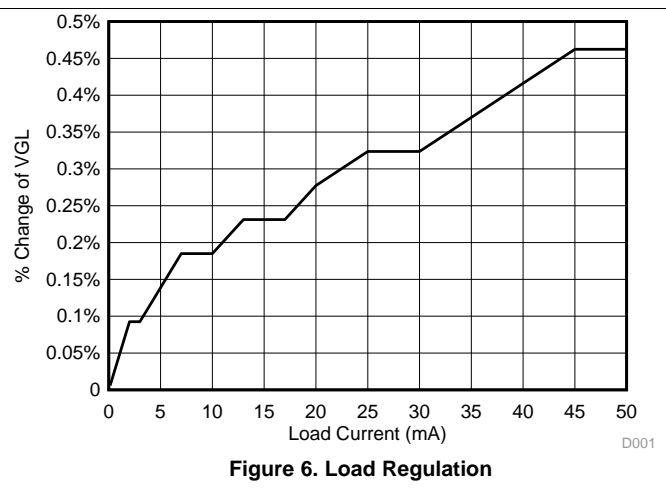
Figure 6. Load Regulation

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