Application Report
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How to Improve the Loading Capability of TLV61046A During Start-up

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ABSTRACT

In order to protect the IC and power supply at short circuit condition, the TLV61046A limits the current when the output voltage is lower than 4 V. In the meantime, this feature limits the loading capability during start-up. This application note introduces several solutions to improve the load capacity.

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Trademarks

1 Introduction

The TLV61046A is a highly integrated boost converter. It can supply up to a 28 V output from a Li+ battery as input.

The TLV61046A limits the output current when the output voltage is below 4 V. The lower output voltage, the smaller output current limit. The device can guarantee only 20 mA output current when the output voltage is 3.3 V. This function protects the device and the power supply from being damaged when the output is shorted to ground. It also limits the loading capability when the device starts up.

This application note proposes several solutions to improve the loading start-up capability and analyzes the benefits and shortage.

2 Analysis

Table 1. Specification

SPECIFICATION	MIN	TYP	MAX	UNIT
Vin	1.8	3.3	3.6	V
Iout	-	-	150	mA
Vout	-	6	-	V

Table 1 shows a specification for common usage. For this target, the circuit was designed like Figure 1. The analysis in this application note is similar for different output voltages recommended in the data sheet.

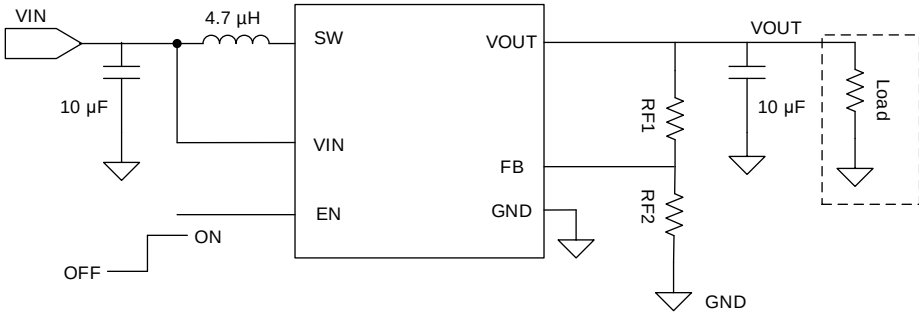

Figure 1. Schematic of the TLV61046 Referred to EVM

There are several phases for the converter start-up, as shown in Figure 2.

1. At the beginning, the circuit does not operate until the EN pin changes to high (Period I). The output voltage is zero because the device has a true disconnection function.
2. After that, the converter starts into the soft-start period. There is about a 2 ms pre-charge phase with 30 mA through the isolation FET (Period II).
3. The TLV61046 starts switching after the pre-charge phase (Period III). While the output voltage is below 3 V, the peak current of the inductance is typically limited to 140 mA. Along with the output voltage going up from 3 V to 5 V, the peak current limit is gradually increased to normal value.

The device fails to start up if the loading is too large, as shown in Figure 3 with a 100 Ω resistor in the output. It successfully starts up with a 1 kΩ resistance load but fails with a 100 Ω resistance. Figure 2 and Figure 3 show these details.

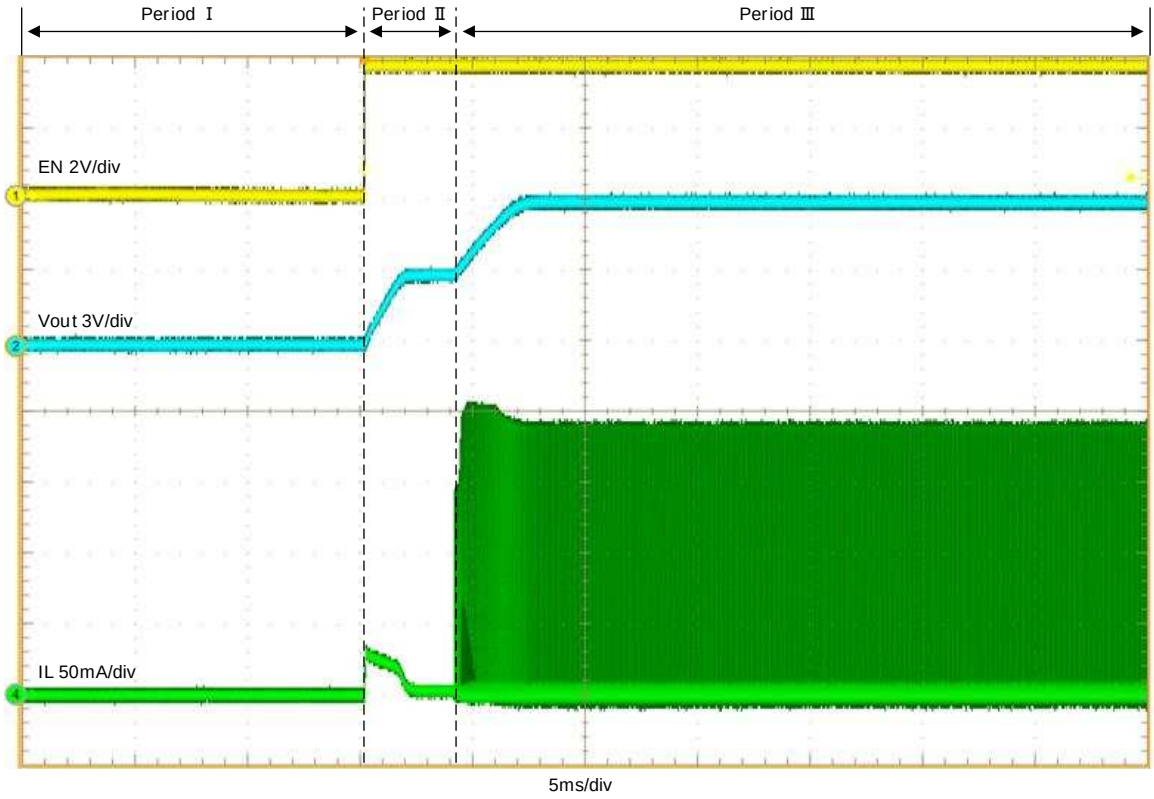

Figure 2. Start-up with 1 kΩ (Vin = 3.3 V)

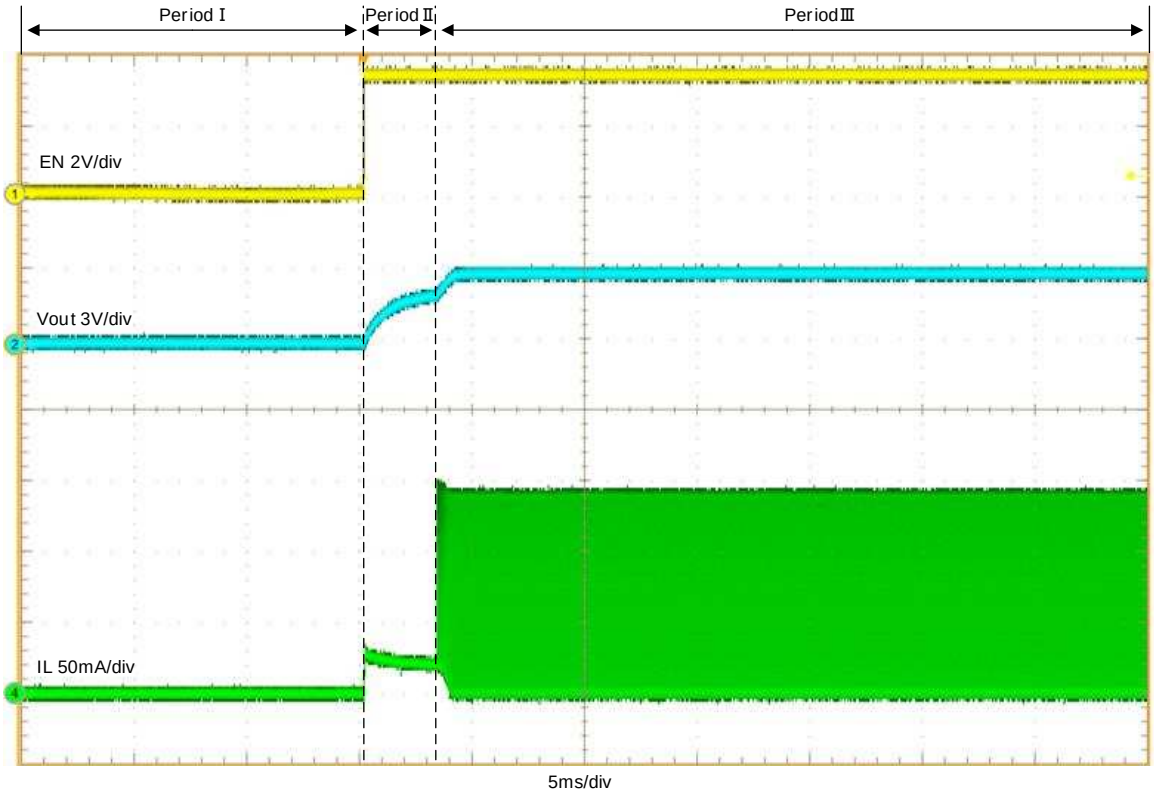

Figure 3. Start-up with 100 Ω Resistance Load (Vin = 3.3 V)

If the load exceeds the capability of the converter during the start-up period, the TLV61046A stays at a voltage below the target. The worst condition would be that the device starts up with a full load under minimum input voltage. A simple calculation of the inductor current is derived from Equation 1 and Equation 2.

$$I_{in} = \frac{V_{out} \times I_o}{V_{in} \times Eff} \quad (1)$$

$$I_{peak} = I_{in} + \frac{V_{in} \times \left(V_{out} - V_{in}\right)}{2 \times L \times V_{out} \times F_{sw}} \quad (2)$$

Setting the Vin to 1.8 V and the output current target Io to 150 mA , the lin would be larger than 140 mA at VOUT = 3.3 V, even assuming 100% efficiency. This is why the convert fails to start up.

3 Solutions

From the start-up principle of the TLV61046A, it is suggested to reduce the output current when VOUT is lower than 5 V. This section introduces several easy, low-cost solutions.

3.1 Solution I: Enable the Load After Start-up

One of the solutions is to disable the load until the start-up is completed. The converter is easy to start up without a load. After the VOUT rises to the target, the current limit is high enough for the normal load, then enable the load. Figure 4 shows the block diagram of this control logic.

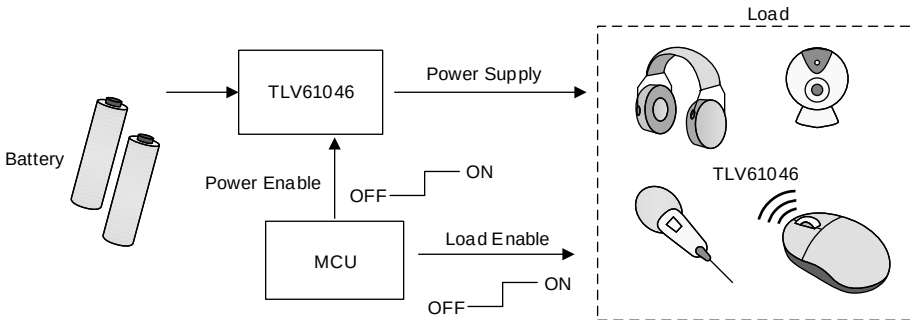

Figure 4. System Block Diagram

The benefit of this solution is that it is easy and there is no need for additional circuit, but it is only suitable for the application where the load can be disabled/enabled.

3.2 Solution II: Use External FET to Disconnect Load Until Vout Rise to High

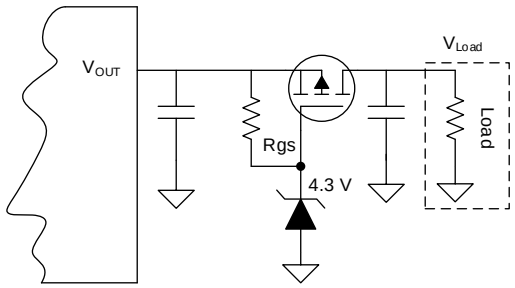

Figure 5. The Circuit with an External Fet and Zener Diode

One of the solutions is connecting the load after the VOUT pin voltage is higher than 5 V. Adding a switch between the VOUT pin and load can implement this solution conductive state.

Figure 5 shows a part of the schematic based on a P-FET with a Zener diode. The P-FET only turns on when the voltage between the gate and source is larger than $V_{gs(th)}$. The gate voltage of the P-FET is clamped by the Zener diode to 4.3 V. When properly designed for P-FET, Zener, and Rgs, the P-FET is not conductive until the VOUT pin reaches the target value.

In this case, FDN306P is chosen as the P-FET with $V_{gs(th)}$ = 0.6 V(typ.). Using the DDZ9687 as the Zener diode with Vz = 4.3 V, the P-FET turns on at approximately 4.3 V + $V_{gt(th)}$, which is approximately 4.9 V. From the Zener diode data sheet, the Izt should be more than 50 µa, then the Rsd can be calculated through Equation 3:

$$R_{gs} < \frac{V_{gs(th)}}{I_{zt}} = 12k\Omega \tag{3}$$

Figure 6 shows the start-up waveform with a 40 Ω load and Vin = 1.8 V. When the VOUT reaches approximately 5 V, the P-FET starts to turn on and the load connects to the VOUT pin, then the current of the inductor increases and completes the start-up.

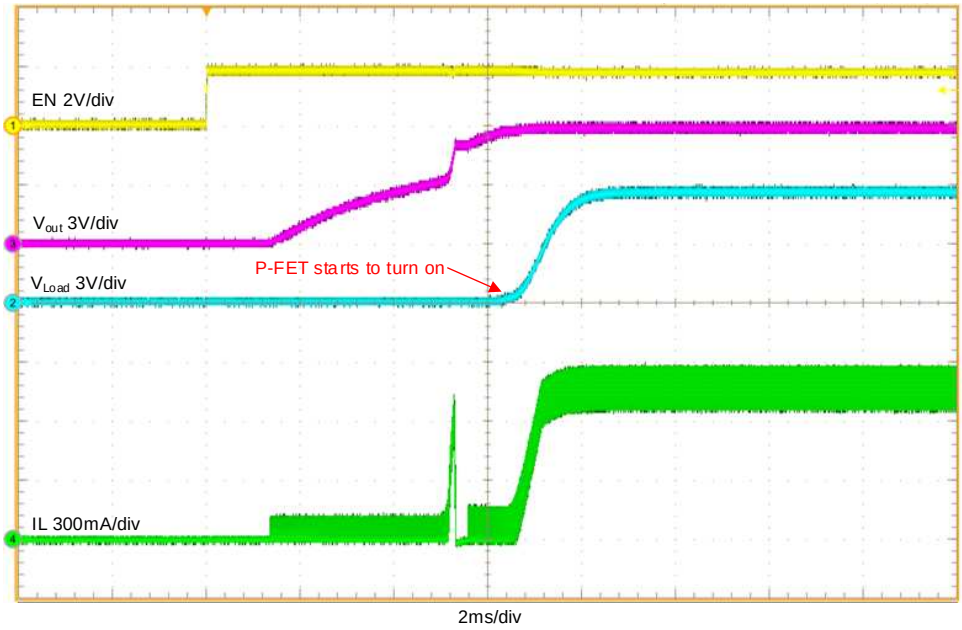

Figure 6. Circuit Start-up with 40 Ω with Vin = 1.8 V

Compared to solution one, the disadvantages of this method are the addition power loss and cost of the Zener and the P-FET. The additional power loss is divided into P-FET conductive loss and Zener circuit loss.

The power loss caused by the P-FET can be calculated as:

$$P_{mos} = I_o^2 \times R_m \tag{4}$$

The power loss caused by the R_{gs} and Zener can be calculated as:

$$P_z = V_{out} \times I_z = V_{out} \times \frac{V_{out} - V_z}{R_{gs}} \tag{5}$$

This reduces the system efficiency of this circuit.

3.3 Solution III : Use External FET to Disconnect Load After the Gap of Vin and Vout Rise

Figure 7 shows another solution using an external FET. The gate of the P-FET is connected to Vin. It is similar to the second solution. The signal from Vin lifts up the conductive voltage of VOUT pin like the Zener does.

The P-FET turns on when the VOUT pin voltage meets Equation 6.

$$V_{out} > V_{in} + V_{gs(th)} \quad (6)$$

where

- $V_{gs(th)}$ is negative for P channel MOSFET

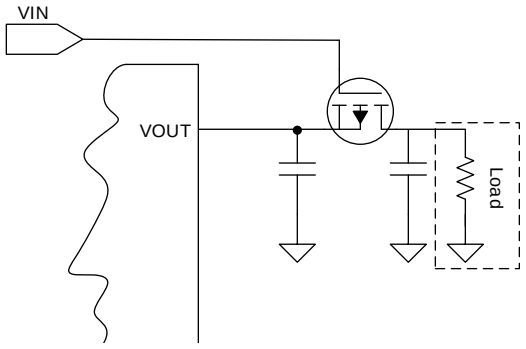

Figure 7. The Circuit Using External FET Controlled by the Gap Between Vin and Vout

It is not easy to optimize the voltage that turns on the P-FET. If you choose FDN306P as the P-FET, the voltage is Vout > Vin + 0.6. It is possible that Vout is not high enough to ensure the converter has enough current capability for the load. If you choose a larger gate threshold P-FET, it is possible that Vgs is not high enough to fully turn on the P-FET, which results in a large conductive resistor.

An easy RC circuit can help increase the VOUT before the P-FET turns on as shown in Figure 8. When the boost converter is disabled, the Vout is zero and the voltage of the Cg is equal to Vin. Thus, the external P-FET stays shut down. When the converter is enabled, the voltage of the Vout pin rapidly rises to the target value. However, the voltage of Cg changes slowly since the Rg limits the charge current. When the Vgs reaches $V_{gs(th)}$, the P-FET starts to turn on and connects the load to the VOUT pin.

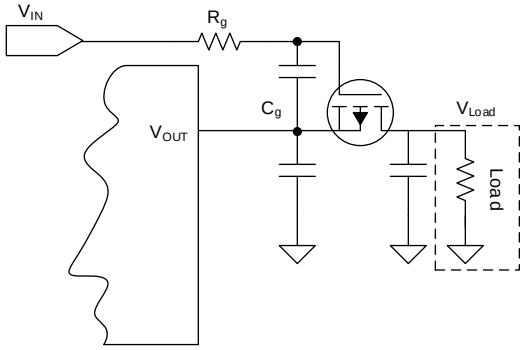

Figure 8. The Circuit with an RC Delay Adding

The value of the delay time can be calculated as:

$$t = R_g C_g \ln \frac{V_{in} - V_{out}}{V_{in} - V_{out} - V_{gs(th)}} \quad (7)$$

It must be modified to ensure the Vout pin rises high enough. Typically, the start-up function inside the TLV61046 is 10 ms, so a 100 ms delay is enough. Take R1 = 499 K and C1 = 220 nF in this design. Figure 9 shows the respective waveform.

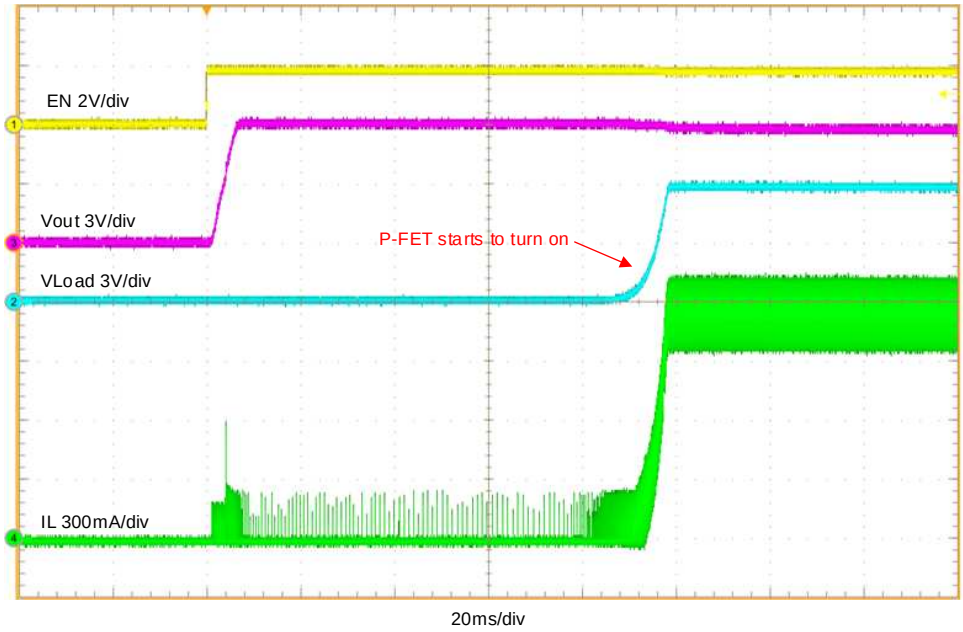

Figure 9. The Solution 3 Circuit Start-up with 40 Ω and Vin = 1.8 V

The additional power loss for this solution is only the P-FET conductive loss in stable operation. The conductive resistance is determined mainly by the Vgs. Equation 8 shows the typical value to calculate it:

$$P_{mos} = I_o^2 \times R_m \quad (8)$$

where

- Rm is the on-state resistor of the P-FET at Vgs = VIN - VOUT

Since the Vgs is higher, the Rm is smaller in solution 3 compared to solution 2.

3.4 Restart Solution for Solution 3

With the solution 3 circuit, there is risk that the converter fails to start if the device is toggled on and off with high frequency since the RC circuit is not fully discharged before the converter is enabled.

Figure 10 details the risk of the failure with solution 3.

1. The device is disabled for a long time and the Cgs is fully discharged. The voltage at the Gate pin is equal to VIN.
2. The first time the converter is enabled, the Vgate of the P-FET is lifted up as the Vout rapidly rises. Then, the Vgate decreases and is finally equal to the VIN. In stable status, Vgs = Vin - Vout.
3. Once the converter with loading is disabled, Vout quickly decreases to zero. The Vgate is a negative value. Then, the Vgate increases and tends to reach VIN. However, the P-FET stays conductive for a while as Vgs slowly changes with the RC delay.
4. If the converter restarts before the Cg recovers to the initial status, the P-FET can still be conductive and the start-up fails.

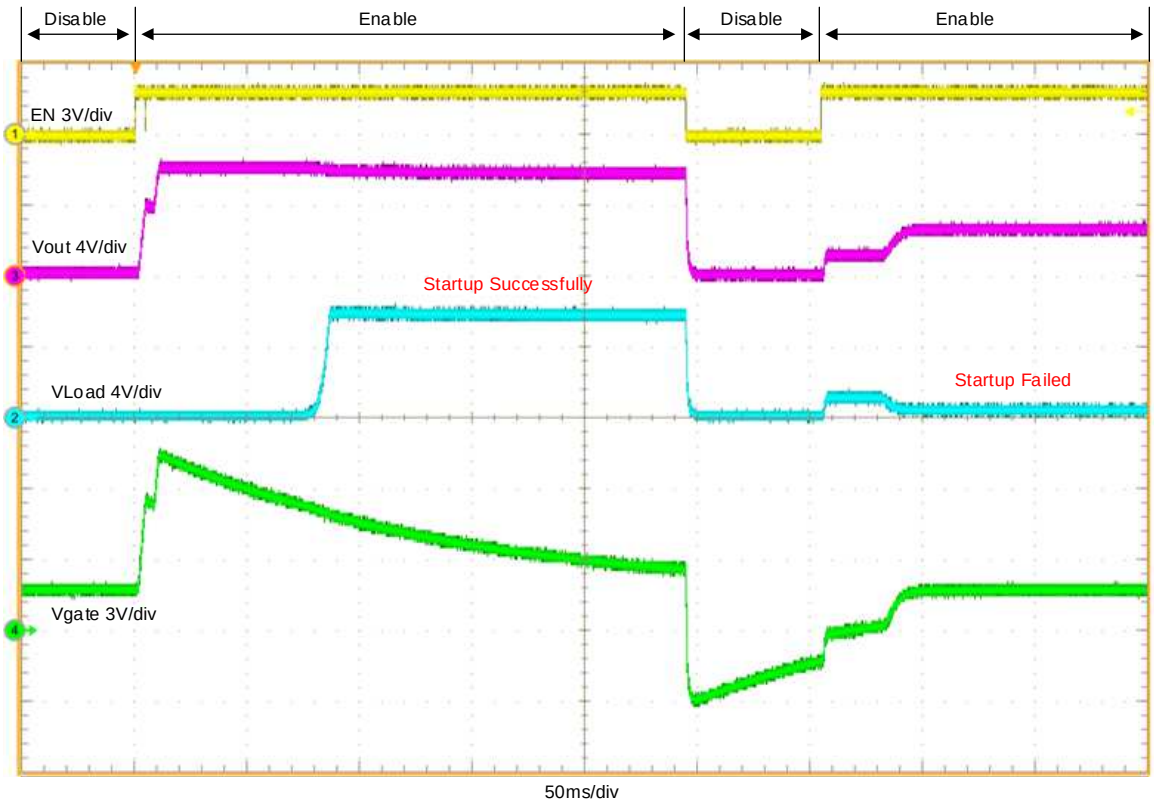

Figure 10. Failed to Restart Quickly

To solve the restart issue, a diode and a resistor can be added to help discharge the Cg quickly. The resistor, Rlim has the potential to control the discharge current. Figure 12 shows the waveform after adding the diode. From the waveform, the gate voltage recovers to VIN at approximately 60 ms, so the circuit is able to start-up with 40 Ω if the disabled period is longer than 60 ms. You can see that the quick restart is successful.

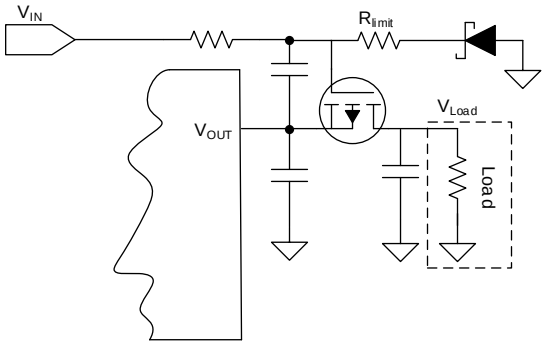

Figure 11. The Circuit With a Diode to Discharge the Cg

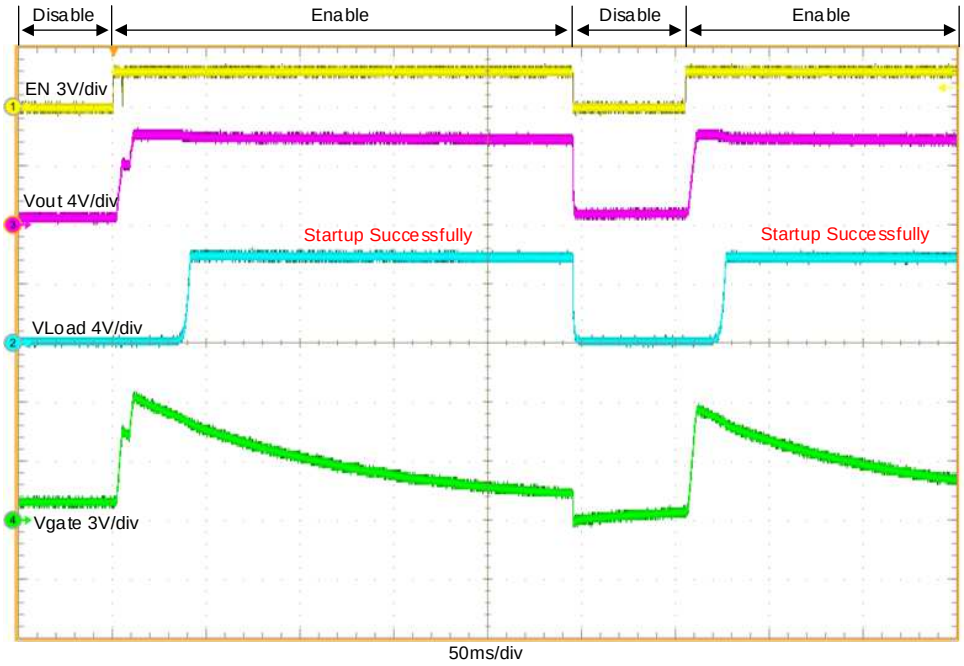

Figure 12. Quickly Restarts After Adding a Diode

4 Summary

This application note describes some solutions to improve the capability of loading start-up. With the proposed circuit, the converter can start-up with a 40 Ω resistive load. These solutions are simple to realize and are helpful to improve the loading capability during start-up. The solution can be chosen depending on the requirements in the real system.

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