Application Report
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Alleviating Short Circuit Thermal Concerns for PoE Powered Devices

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ABSTRACT

In IEEE 802.3bt Power over Ethernet (PoE) applications, an isolated power supply is implemented in most Power Devices (PDs) for safety considerations. In addition, DC-DC output overcurrent protection is an important topic especially end-equipment damage that creates an output short circuit condition. This paper introduces the thermal issues that can exist in a prolonged output short condition and how to alleviate any thermal concerns with discrete hiccup circuit. This circuit could be implemented in all of tps2375x family of PoE PDs.

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1 Introduction

In the traditional Flyback topology shown in Figure 1, the peak current signal is sensed through the current shunt resistor at the primary side of the power transformer. When the overcurrent occurs at output side, the Flyback controller IC will clamp the input current to the point of overcurrent protection (OCP) threshold by monitoring the peak current signal on current shunt resistor in Figure 2. The method of OCP protection is an input current limit, or input power (Pin) limit. That method also does output power (Pout) limit indirectly. During the OCP, based on Pout limit, the output voltage drops while the output peak fault current is increasing until the voltage on auxiliary (AUX) winding drops to hit the point of under voltage lockout (UVLO) of controller's Vc pin. The worst case occurs at lower Vout and higher Pin limit at short circuit condition, producing the pretty high peak fault current and causing the thermal issue on Synchronous FET or Rectifying Diode at secondary side.

The duration of peak fault current depends on the capacitance on Vc pin of controller. The smaller capacitance on Vc pin, the higher hiccup OCP frequency is produced. The higher capacitance on Vc pin, the longer duration of peak fault current exists. Whatever the higher hiccup OCP frequency or the longer duration of peak fault current, the duty cycle of hiccup OCP is similar and the thermal issue could not be reduced. One way to minimize the thermal issue at short circuit condition is to reduce the hiccup OCP frequency and to make the shorter duration of peak fault current.

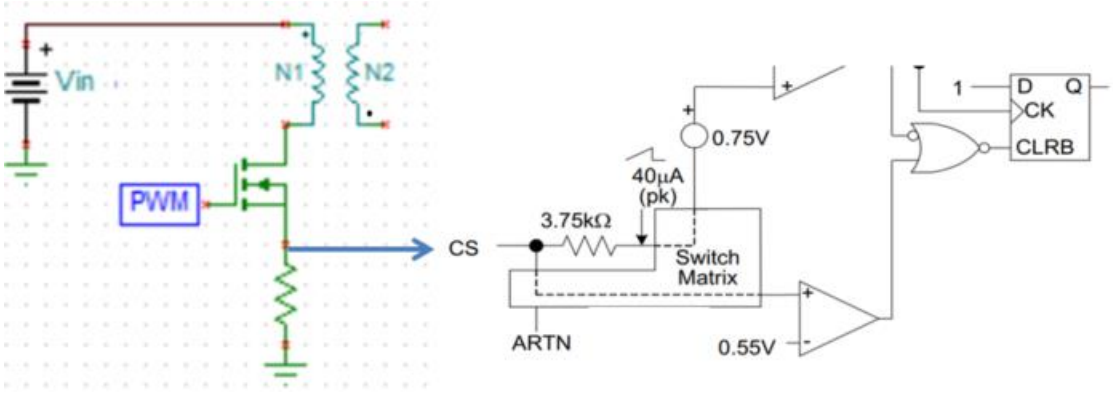

Figure 1. Traditional Flyback Current Limit Scheme

Figure 2. Peak current signal on current shunt resistor

Figure 3 shows that when the standard PoE voltage range feeds VDD bus after PoE handshaking or adapter plug-in, the internal constant current source will be triggered to start charging the external C_{vc} capacitor. The voltage on C_{vc} is a constant rising slope until reaching to 15V,typ. The charging current path to external C_{vc} is (1). Therefore, the controller starts sending PWM pulse to switch the external primary FET M1 while the internal current source of controller is turned off. Before the output voltage (Vout) achieves the target Vout, the external C_{vc} capacitor is providing the energy as discharging to Vc pin as the source of the internal gate driver. The current path is (2). After Vout achieves the target voltage, the AUX winding start providing the energy to the internal gate driver and recharging C_{vc} capacitor. The current path is (3) and the waveform is shown in Figure 4.

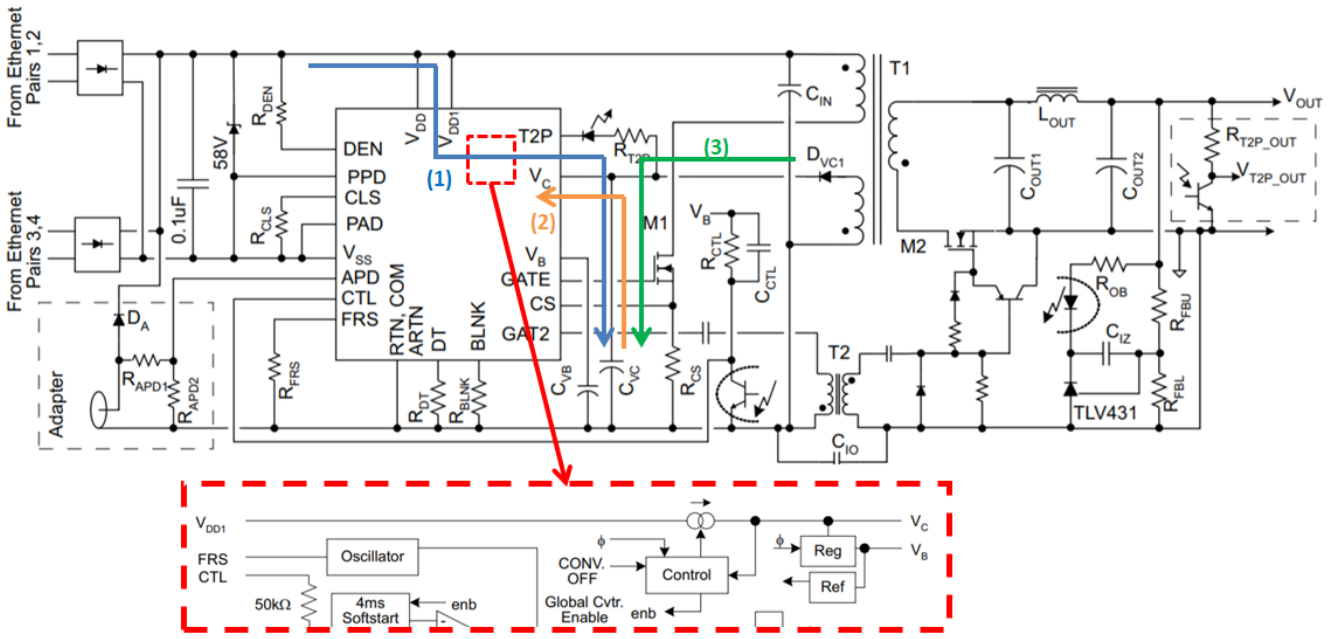

Figure 3. C_{vc} Current Path During the Startup

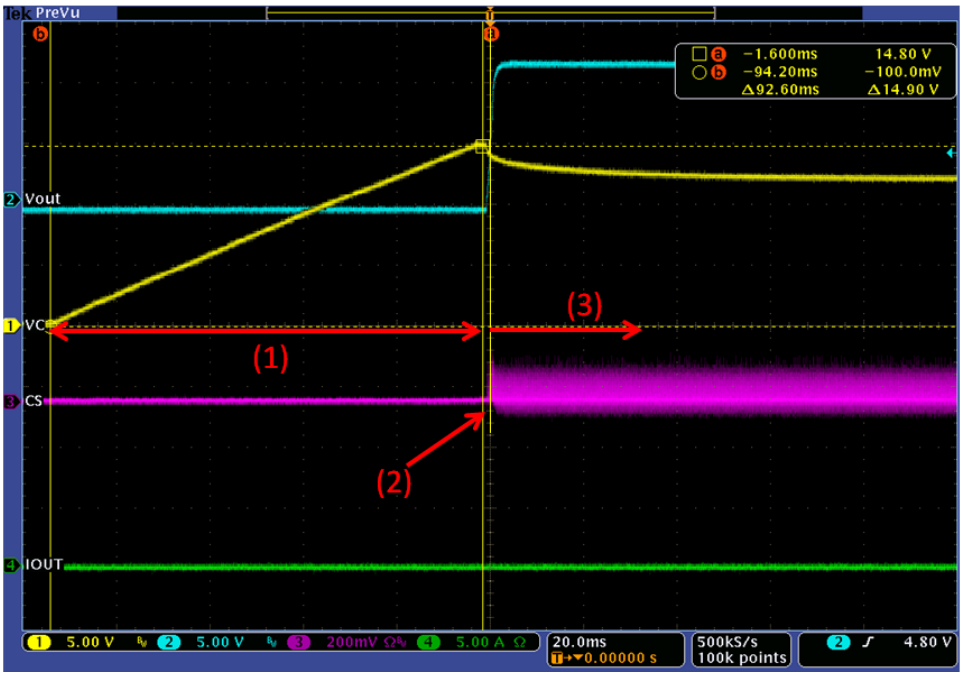

Figure 4. Startup waveform on C_{vc}

2 Thermal Challenge During an Output Short

When the output is short, the PWM controller will clamp input current to do Pin limit. At output side, the output peak fault current is increasing while output voltage is decreasing until the voltage on AUX winding, which is reflected from 2ed output winding, to hit UVLO of VC, causing PWM pulse stop. Therefore, the internal current source will be enabled again to recharge the external C_{vc} until achieving 15V,typ, turning off internal current source and starting new PWM pulse. If the short circuit fault still exists, the power converter will repeat the cycle above until fault goes away. The hiccup OCP behavior could be observed at output short circuit condition.

The challenge is that before PWM stop switching, the output peak fault current will keep rising to a pretty high level. The worst case occurs at lower Vout condition such as 5Vout/5A AT power level. During the period of short circuit condition, the peak fault current will pass through the Synchronous FET or Rectifying Diode on the secondary, causing its temperature to increase. In some conditions, its surface temperature can exceed 130C at 25C ambient condition. The waveform is shown in Figure 5 and the thermal picture is shown in Figure 6.

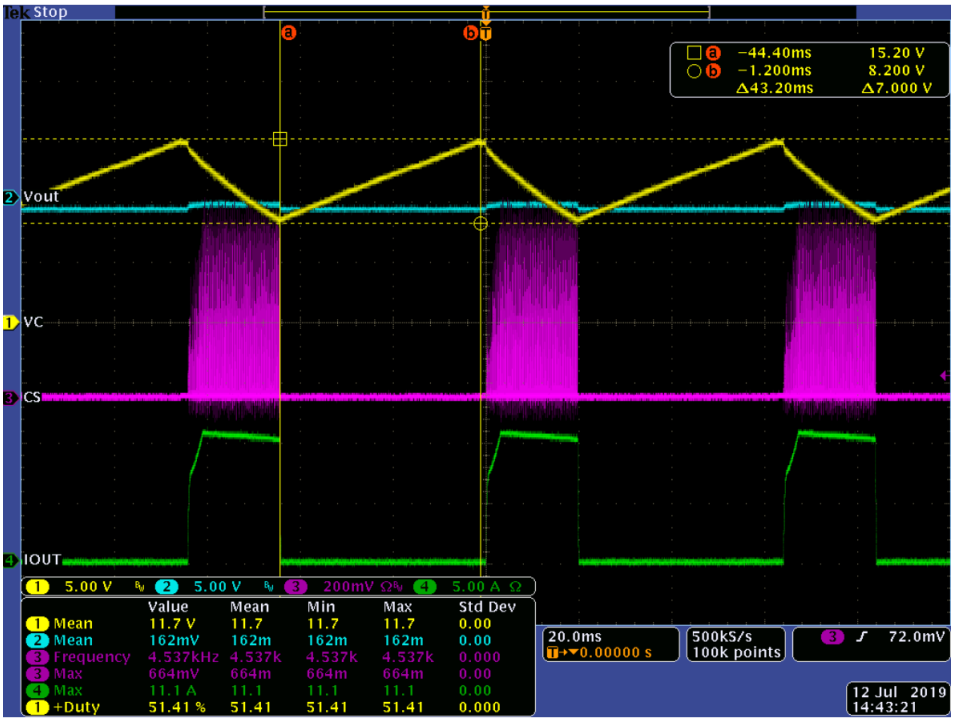

Figure 5. The original hiccup OCP waveform

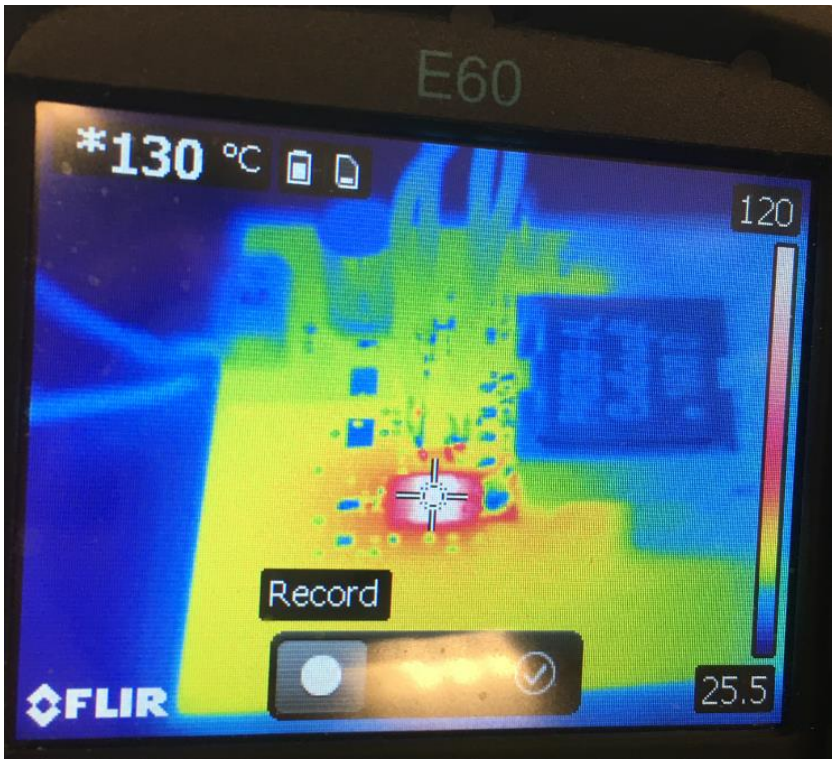

Figure 6. IR thermal photo with original hiccup OCP mode

3 Alleviating the Thermal Concern at Short Circuit Condition

Decreasing C_{vc} will increase the frequency of hiccup OCP. Conversely, the frequency of hiccup OCP will decrease by increasing C_{vc}, but make longer duration of peak fault current. Whatever increasing or decreasing C_{vc}, the duty cycle of the hiccup OCP is almost the same. The heat issue could not be alleviated. This paper introduces the way how to adjust the duty cycle of peak fault current duration.

In Figure 7, use the 2N3906's emitter-base diode in parallel with 5.1k to create a current source as current path (b) as 0.6V/5.1k = 117uA.

The rest of current from internal current source is passed through the current path (a).

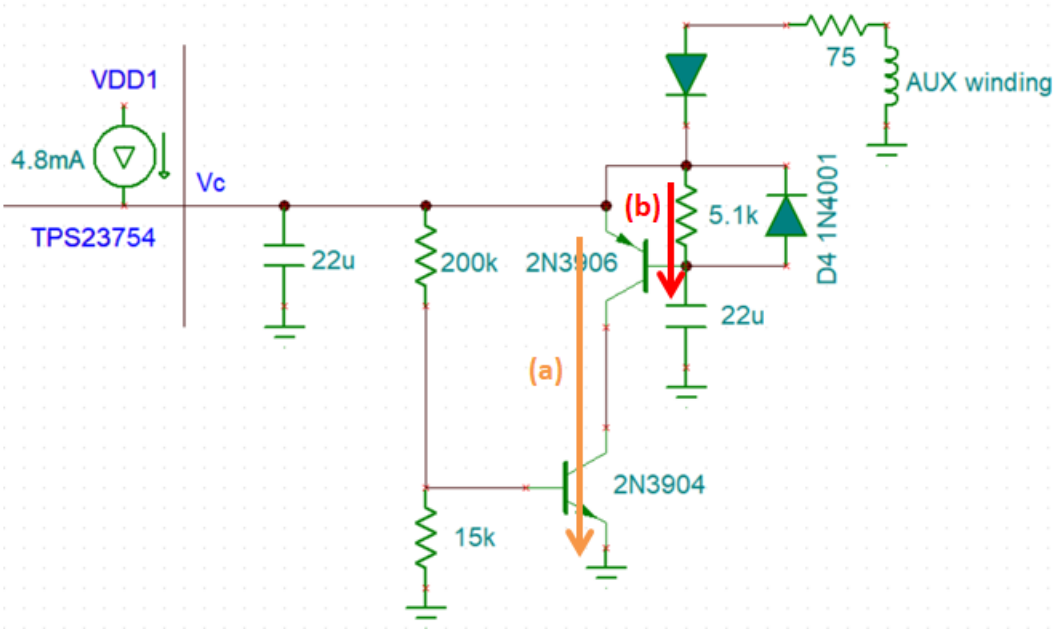

Figure 7. The External Discrete Hiccup Circuit

The new current source is to create the longer recharging time as OFF time of the hiccup OCP, getting a lower average fault current and alleviating the thermal concern on Synchronous FET or Rectifying Diode at secondary. The waveform is shown in Figure 8 and the thermal picture is shown in Figure 9.

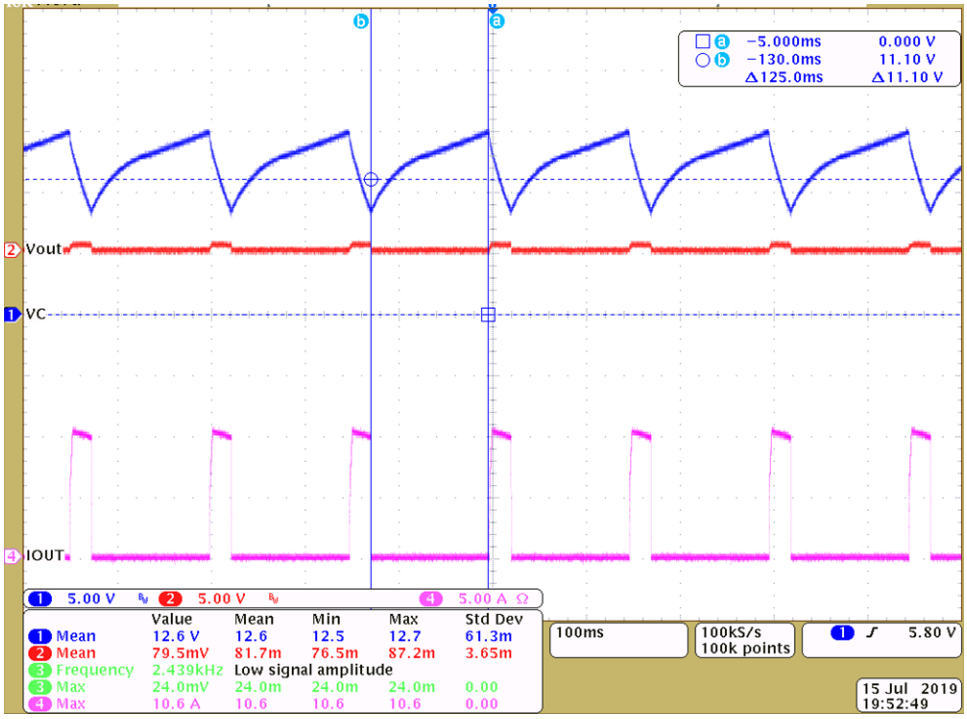

Figure 8. The Hiccup OCP Waveform with External Hiccup Circuit

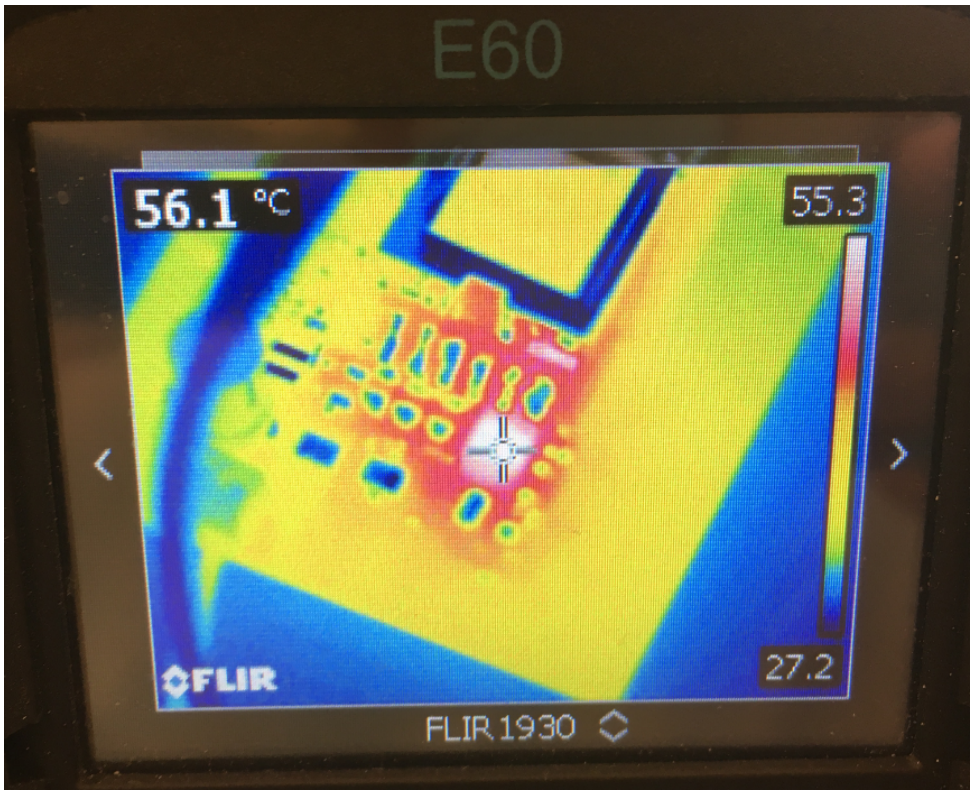

Figure 9. IR Thermal Photo with External Hiccup OCP Circuit

3.1 Maintain Power Signature (MPS)

According to IEEE802.3bt standard in Table 1, a valid Type-2 Maintain Power Signature (MPS) is a 10-mA pulse current for at least 75 ms every 310 ms. The NPN transistor 2N3904 plus divider resistor 200k and 15k act an important role to delay turn ON the new current source and to speed up the ramping time of Vout at beginning in order to meet the timing of MPS 310ms in the IEEE802.3bt standard. After 2N3904 turn ON, the new current source will be enabled to support the longer hiccup OCP OFF time at short circuit condition. The two ramping Vout slope can be observed at startup in Figure 10.

Table 1. PD DC Maintain Power Signature (MPS)

Item	Parameter	Symbol	Units	Min	Max	Conditions
1	Total input current per the assigned Class, for single-signature PDs					
	Class 1 to 4	I_{Port_MPS}	A	0.01	—	See 145.3.9
	Class 5 to 8			0.016		
2	Input current on each powered pairset for dual-signature PDs					
	Class 1 to 5	I_{Port_MPS-2P}	A	0.01	—	—
3	PD Maintain Power Signature Time	T_{ms}	ms	75	—	long_class_event = FALSE
				7	—	long_class_event = TRUE
4	PD Drop Out Period	T_{MPDO_PD}	ms	—	250	long_class_event = FALSE
				—	310	long_class_event = TRUE

Figure 10. Startup Waveform with External Discrete Hiccup Circuit

In the next generation PDs TPS2373x family, the ~25% hiccup duty ratio is integrated into TPS2373x. In the Figure 11, when overload or short circuit occur, VCC voltage goes low to hit its UVLO. Therefore, the startup source is turned back on and soft start cycle is reinitiated. SST is slowly discharged by 4 µA internal current source while PWM is stopped until reaching to a certain low level. There is new soft start cycle and the output voltage is ramped up. SST is charged with 10 µA.

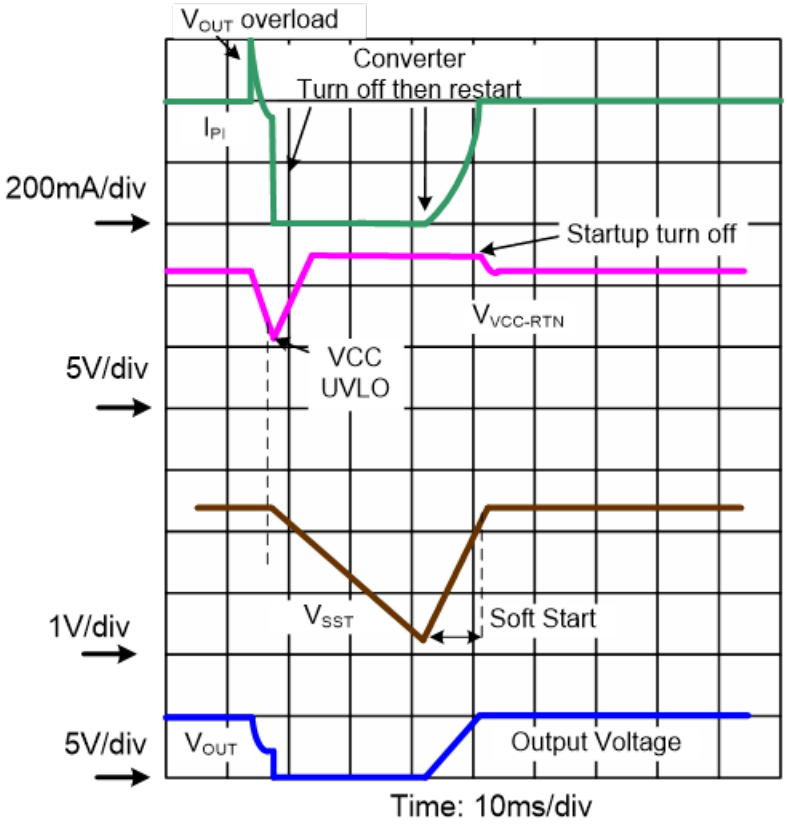

Figure 11. TPS2373x Restart Following Severe Overload at Main Output of PSR Flyback DC-DC Converter

4 References

1. Texas Instruments, *TPS2375x IEEE 802.3at, High Efficiency, PoE Interface and DC-DC Controller*
2. Texas Instruments, *TPS23730 IEEE 802.3bt Type 3 PoE PD with High Efficiency DC-DC Controller*

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