Application Note

Driving PWM Loads with TI High-Side Switches

ABSTRACT

Driving LED and resistive loads are two of the most common applications for High-side switches where the design benefits from PWM driving with High-side switches. This application report investigates design tradeoffs in resistive and LED PWM applications for TI High-side switches.

This report details the PWM's effects on load power, high-side switch output timing, and device thermals through example designs, theory, and real-world testing.

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Trademarks

1 Introduction

Pulse-width modulation (PWM) is an indispensable technique for controlling load power when driving off-board loads with high-side switches (HSS). By adjusting PWM duty cycle, average load power can be controlled with accuracy and much more efficiently than designs which rely on linear regulation of voltage or current to the load. PWM control can be used to increase product functionality — for example, to enable a vehicle owner to choose the heat level in a heated seat or adjust the brightness of footwell lighting. Figure 1-1 compares PWM and linear control schemes which result in the same load power.

PWM duty cycle may be software or hardware defined and can be varied in real-time. Apart from the limitations of the high-side switch or nuances of the load, the average power delivered to the load is virtually independent of PWM frequency. This allows for flexibility in the system design.

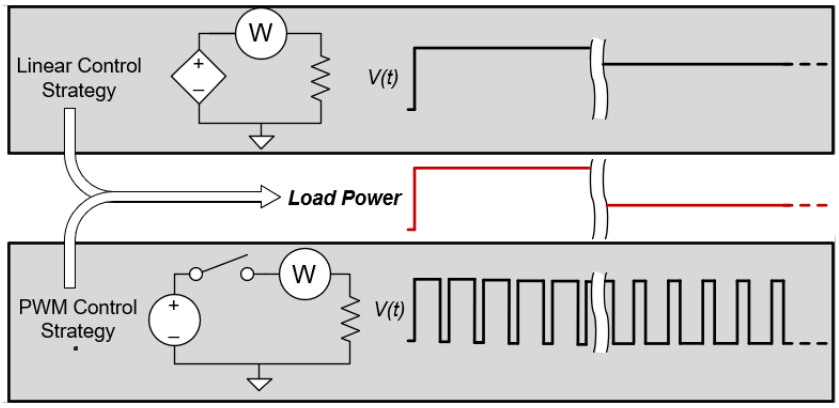


Figure 1-1. PWM and Linear Control of Load Power

2 Device Thermals

Thermal limits of any IC should always be kept in mind, and this is especially true for high-side switches which are often asked to switch large currents to the load.

We can estimate the total power dissipated by the device itself by summing power dissipation due to the FET R_{ON}, switching losses, and quiescent power.

We can calculate power dissipated in the HSS FET as in Equation 1. This power is proportional to the on-resistance (specified in the device datasheet) and the average current through the FET.

$$P_{FET} = R_{ON} \cdot I_{Avg}^2 \tag{1}$$

As PWM operation switches the HSS FET on and off every cycle, we also need to consider how much energy it takes to charge and discharge the gate. We can use Equation 2 to calculate switching loss from switching energy losses E_{ON}, E_{OFF} if defined in the device datasheet. Notably, this scales with frequency and is a large component of total power dissipation in the HSS.

$$P_{SW} = f_{PWM} * (E_{ON} + E_{OFF}) \tag{2}$$

If E_{ON}, E_{OFF} are not available for a device, we can approximate the switching losses from how long it takes the device to slew the output low or high using Equation 3.

$$t_{rise,fall} = \frac{V_{vs}}{SR_{ON,OFF}} \tag{3}$$

We then substitute our results from Equation 3 into Equation 2 to get switching power.

$$P_{SW} \approx I_{load} \cdot V_{vs} \cdot f_{PWM} \cdot \frac{t_{rise} + t_{fall}}{2} \tag{4}$$

$$P_{HSS(TOT)} = P_q + P_{FET} + P_{SW} \tag{5}$$

A safe junction temperature must be maintained whether operating in PWM or DC driving. The maximum limit is specified in the HSS datasheet—generally 150°C. TI HSS datasheets contain the thermal characterization parameters listed in Table 2-1

Table 2-1. Definitions of Thermal Parameters

$R_{\Theta JA}$	Junction-to-ambient thermal resistance
$R_{\Theta JB}$	Junction-to-board thermal resistance
$R_{\Theta JC}$	Junction-to-case thermal resistance.

TI HSSs utilize a thermal pad which is recommended to be soldered directly to the PCB. This benefits devices thermals by utilizing the large surface area of the attached thermal plane as a heatsink, which closely couples with board temperature. Board temperature, however, is difficult to measure accurately and is highly dependent on board construction and solder coverage/quality on the high side switch. Ambient temperature, on the other hand, is easier to measure and straightforward to use in junction temperature estimation.

For a given ambient temperature the operating junction temperature may be estimated as below.

$$T_J = T_A + P_{TOT} \cdot R_{\Theta JA} \tag{6}$$

The PWM frequency is set tightly by the maximum sustainable power dissipation of the HSS, as switching losses are dominant. This power limit can be estimated from Absolute max junction temperature specification and maximum ambient temperature.

$$P_{TOT} < \frac{T_{J(MAX)} + T_{A(MAX)}}{R_{\Theta JA}} \tag{7}$$

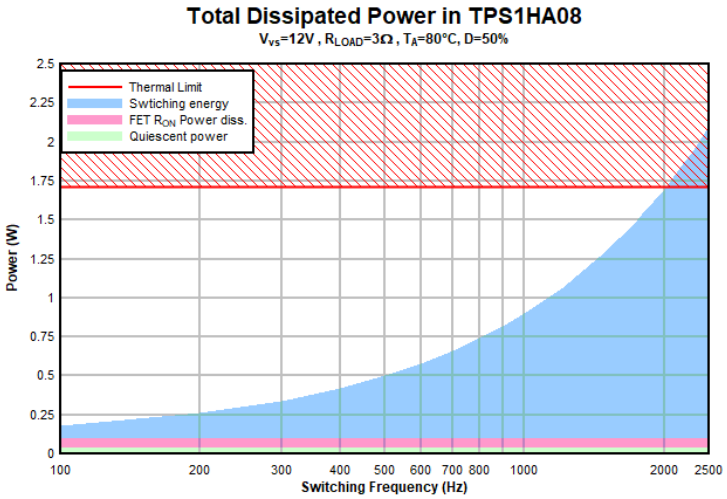


Figure 2-1. Power Dissipation Sources in TPS1HA08

3 Timing Limitations

3.1 Background

In a PWM application, it is important to know the limits of timing that the HSS imposes on the final system design. Timing limitations affect how accurately load power can be controlled over the range of duty cycles. Since resistive and LED loads that convert load power to energy are intended to be detected by humans, some variation from ideal load power can often be tolerated. In cases where load power has to be more precisely controlled, such as in automotive lighting where luminous power is strictly regulated by governmental agencies, a designer may choose to use a lower PWM frequency in order to guarantee compliance with lightning standards regardless of HSS parameter skew.

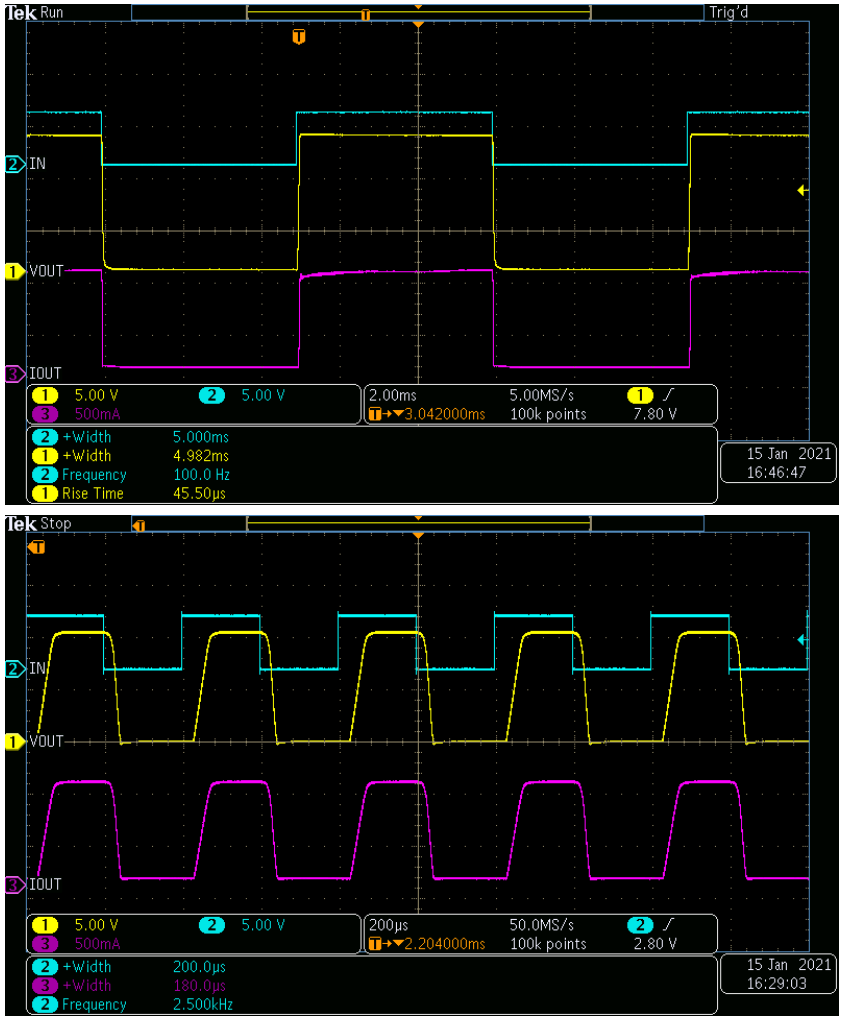


Figure 3-1. Switching Too Fast in a TPS1H000-Q1 Resisitve Load Setup

The principal phenomena that limit the pulse width a HSS can drive accurately are limited output slew-rate and propagation delay mismatch, also known as pulse-width distortion.

3.2 Pulse-Width distortion (PWD)

Pulse-width distortion (PWD) arises from mismatch in the HSS's ON and OFF delay times and low-high/high-low propagation delay. In Figure 3-2, the various timing parameters that need to be considered when implementing a PWM scheme with a TI high-side switch is illustrated. The timing parameters in this diagram are correlated closely to the parameters specified in the "Switching Characteristics" section of the device data sheet. In Figure 3-3, an example excerpt of the switching characterstics can be seen.

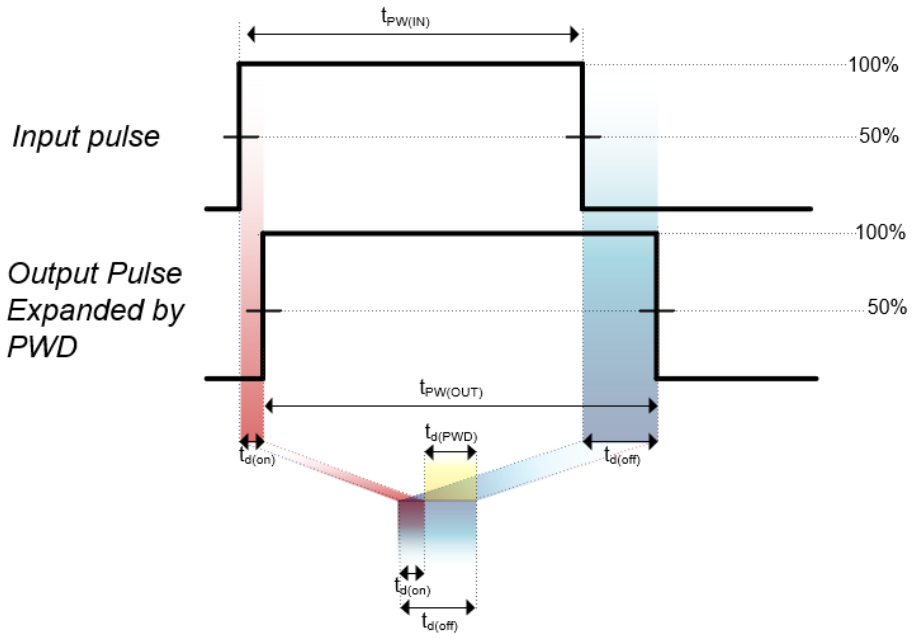


Figure 3-2. Pulse-Width Distortion Timing Definition

7.6 Switching Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(on)}$	Delay time, V_{OUTx} 10% after $V_{INx}\uparrow$ (See Figure 1.)	V_{VS} = 13.5 V, V_{DIAG_EN} = 5 V, I_{OUTx} = 0.1 A, IN rising edge to 10% of V_{OUTx}	10	30	60	µs
$t_{d(off)}$	Delay time, V_{OUTx} 90% after $V_{INx}\downarrow$ (See Figure 1.)	V_{VS} = 13.5 V, V_{DIAG_EN} = 5 V, I_{OUTx} = 0.1 A, IN falling edge to 90% of V_{OUTx}	10	30	60	µs
dV/dt(on)	Turnon slew rate	V_{VS} = 13.5 V, V_{DIAG_EN} = 5 V, I_{OUTx} = 0.1 A, V_{OUTx} from 10% to 90%	0.1	0.25	0.5	V/µs
dV/dt(off)	Turnoff slew rate	V_{VS} = 13.5 V, V_{DIAG_EN} = 5 V, I_{OUTx} = 0.1 A, V_{OUTx} from 90% to 10%	0.3	0.5	0.9	V/µs
$t_{d(match)}$	$t_{d(rise)} - t_{d(fall)}$ (See Figure 1.)	V_{VS} = 13.5 V, I_L = 0.1 A. $t_{d,\ rise}$ is the IN rising edge to V_{OUTx} = 90%. $t_{d(fall)}$ is the IN falling edge to V_{OUTx} = 10%.	–60		60	µs
CURRENT-SENSE CHARACTERISTICS (See Figure 2.)						

Figure 3-3. TPS4H000-Q1 Timing Parameters

The pulse-width distortion due to propagation-delay effects is defined as

$$t_{d(PWD)} = t_{d(on)} - t_{d(off)} \tag{8}$$

If the high-side switch data sheet specifies $t_{d(match)}$, using this parameter is preferable to calculate total distortion as it removes any uncertainty of correlation between slew rate and out. When rise and fall times are much smaller than the pulse width, slew-rate effects can be ignored and total pulse-width distortion may be approximated as:

$$t_{d(PWD)} \approx t_{d(match)} \tag{9}$$

In the case the data sheet does not specify $t_{d(match)}$ we can obtain more precision by using:

$$t_{d(PWD)} = t_{d(match)} - \frac{V_{vs}}{2}\left(\frac{1}{SR_{ON}} - \frac{1}{SR_{OFF}}\right) \tag{10}$$

Where V_{vs} is the high-side supply voltage, and SR_{ON} / SR_{OFF} are the device turn-on/turn-off slew rates. Note that these specifications are worst-case and are specified at a specific supply voltage and load current. The use

of the worst-case parameters will allow us to build a robust design that will work under a wide arrange of ambient conditions.

3.2.1 Timing Impact of Delay Mismatch

If $t_{d(match)} > 0$, this means that the ON delay is larger than OFF delay. This results in truncation of a high PWM pulse by $t_{d(match)}$. Conversely $t_{d(match)} < 0$ results in expansion of the high PWM pulse and truncation of the low pulse by $t_{d(match)}$. Increased delay mismatch mutates the output PWM, which is why delay mismatch is also referred to as pulse-width distortion.

The actual pulse-width observed on the output can be calculated as below, where D_{in} is the input PWM duty cycle and f is the PWM frequency. Using min/max data sheet specifications in these calculations gives the worst case pulse-widths versus frequency as well as the range guaranteed by TI.

$$t_{d(PWD)} = t_{d(match)} - \frac{V_{vs}}{2}\left(\frac{1}{SR_{ON}} - \frac{1}{SR_{OFF}}\right) \tag{11}$$

$$t_{PW(OUT)} = D_{in} \cdot f^{-1} - t_{d(PWD)} \tag{12}$$

$$D_{out} = f \cdot t_{pw(out)} = D_{in} - (f \cdot t_{d(PWD)}) \tag{13}$$

Figure 3-4, Figure 3-5 show the possible variation from ideal pulse width based on data sheet specifications for TPS1H100-Q1. Most devices will be well-matched and fall close to the ideal pulse-width curve, but as pulse-width decreases the output pulse-width may vary significantly for some devices.

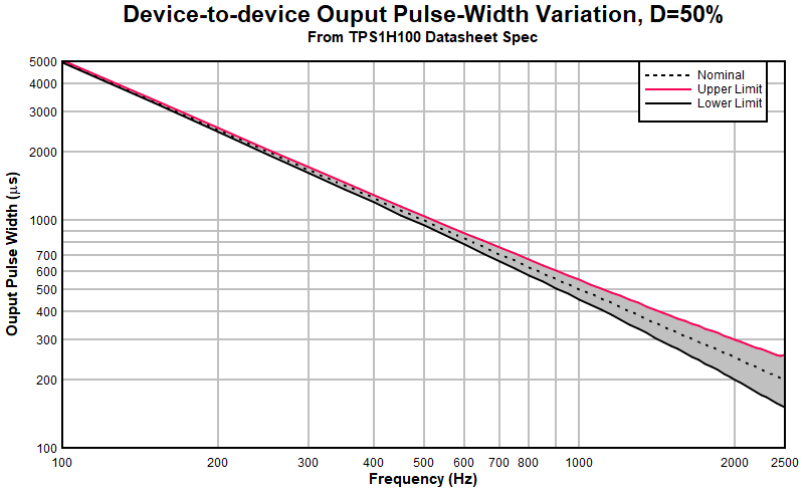


Figure 3-4. Device-to-Device Output Pulse-Width Variation, D = 50%

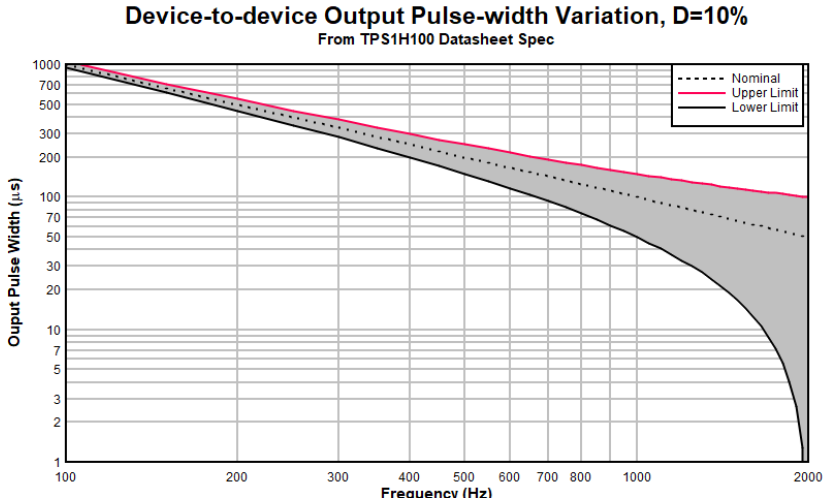


Figure 3-5. Device-to-Device Output Pulse-Width Variation, D = 10%

We can then take the pulse width accuracy compared to the input and correlate this into the formula below:

$$t_{PW(IN)} = D_{in} \cdot f^{-1} \tag{14}$$

$$PW_{acc}\% = \frac{t_{pw(OUT)}}{t_{pw(IN)}} = 1 - |t_{d(PWD)} \cdot f \cdot D_{in}^{-1}| \tag{15}$$

From Equation 16, we know that output PWM accuracy scales proportionally with respect to frequency and inversely with respect to duty cycle. Thus, delay mismatch has the greatest distortion effect at the highest frequencies and lowest duty cycles.

3.2.2 Power Impact of Delay Mismatch on Resistive Loads

The reduction of output pulse-width accuracy has an even greater effect on the accuracy of power delivered to a resistive load since load power is proportional to the square of the current delivered.

LED power analysis taking the example of a resistive load scenario:

$$P_{load} \propto I_{load}^2 \text{ , where } I_{load} = D_{out} \cdot \frac{V_{vs}}{R_{load}} \tag{16}$$

$$P_{load(actual)} = P_{load(ideal)} \cdot \frac{D_{out}}{D_{in}} \tag{17}$$

$$P_{load(actual)} = R_{load} \cdot I_{load}^2 = R_{load} \cdot \left(D_{out} \cdot \frac{V_{vs}}{R_{load}}\right)^2 \tag{18}$$

$$P_{load(actual)} = V_{vs}^2 \cdot D_{out}^2 \cdot R_{load}^{-1} \tag{19}$$

And

$$P_{load(ideal)} = V_{vs}^2 \cdot D_{in}^2 \cdot R_{load}^{-1} \tag{20}$$

Substituting input duty cycle from Equation 11,

$$P_{load(actual)} = V_{vs}^2 \cdot R_{load}^{-1} \cdot \left[D_{in} - \left(f \cdot t_{d(PWD)}\right)\right]^2 \quad (21)$$

We can visualize the worst-case effects of pulse-width distortion on a resistive load scenario with the following conditions:

- HSS supply voltage: V_{vs} = 10 V
- Load resistance: R_{load} = 10 Ω
- PWM Duty Cycle: D_{IN} = 50%
- Pulse-width distortion: $t_{d(PWD)}$ = ±50 µs (TPS4H000-Q1 min/max spec)

We can also quantify the variation of actual power dissipation due to compared to ideal.

$$\frac{P_{load(actual)}}{P_{load(ideal)}} = \frac{D_{out}^2}{D_{in}^2} = \left(\frac{D_{in} - f \cdot t_{d(PWD)}}{D_{in}}\right)^2 \quad (22)$$

Using the example of TPS4H000-Q1,

- PWM Duty Cycle: D_{IN} = 50%
- Pulse-width distortion: $t_{d(PWD)}$ = ±50 µs (TPS1H100 min/max spec)

We can see that if we consider a worst-case PWD scenario of TPS4H000-Q1, switching frequency is virtually limited to below 1 kHz again if relatively accurate load power is desired at 50% duty cycle. This figure is even lower if high accuracy is required at low duty cycles.

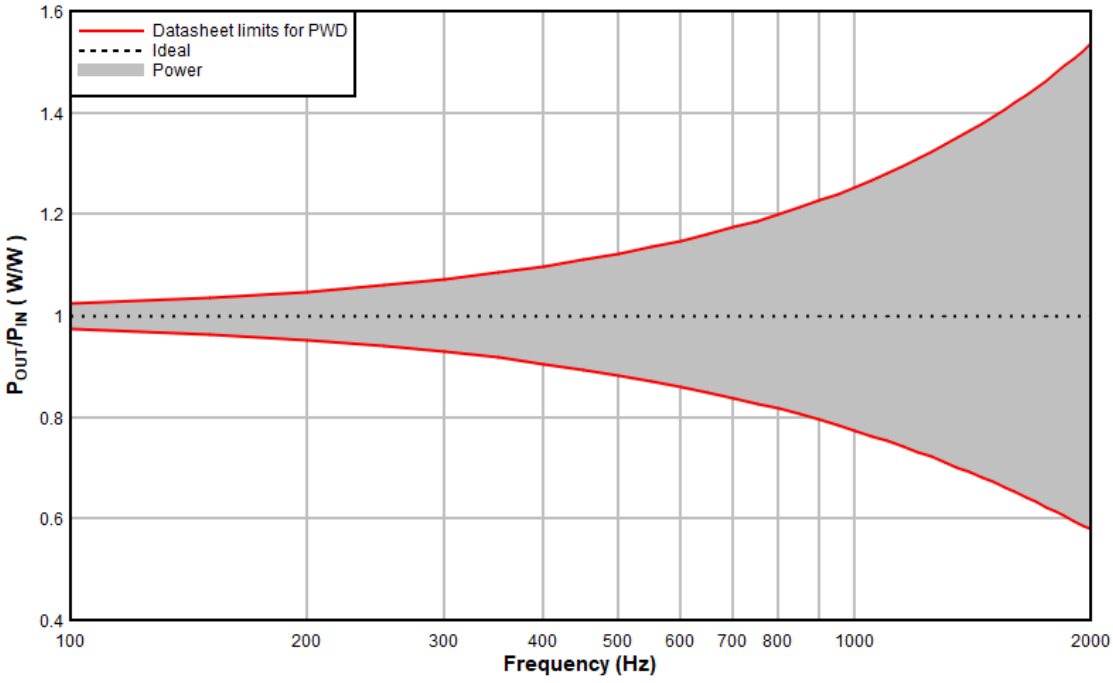


Figure 3-6. Potential Load Power Variation for TPS4H000, Normalized

3.3 Finite Slew Rate

Along with non-zero pulse-width distortion, finite output slew-rate is the other principal timing constraint that limits high side switch operating frequency and minimum input pulse-width. While this appears as a drawback when driving resistive and LED loads, reduced slew-rates are useful in limiting inrush current for large capacitive loads.

Taking the TPS1H100-Q1 HSS as an example, ON and OFF slew rate are nominally SR_{ON} = *0.36 V/µs* and SR_{OFF} = *0.32 V/µs*, and stable over operating conditions. This leads to rise and fall times being heavily dependent on (and directly proportional to) the supply voltage V_{vs}. If we consider the minimum slew rate

specification from the TPS1H100-Q1 data sheet the slew rate will be as low as $SR_{ON,OFF}$ = *0.1 V/µs*. This range can drastically reduce the power delivered at higher operating frequencies and supply voltages if ignored.

We can estimate the rise and fall times from the ON/OFF slew rates as follows,

$$t_{rise(OUT)} = V_{vs} \cdot (SR_{ON})^{-1}, \text{ and } \quad t_{fall(OUT)} = V_{vs} \cdot (SR_{OFF})^{-1} \tag{23}$$

In extreme cases, unreasonably small input pulses can cause the HSS output to be unable to reach before dropping if the sum of output rise and fall times is less than the input pulse width. In LED applications where the output needs to exceed the forward voltage(s) of the LED string, such distorted output pulses will result in lower than expected light intensity or possibly no visible output.

Ensuring the output rise/fall times are at least an order of magnitude less the ON pulse duration means we can safely ignore the effects of slew rate on both power and output accuracy. This same general rule can also applied to propagation-delay mismatch effects. If this cannot be guaranteed, designers wishing to operate their systems at the highest PWM frequency possible must make deliberate effort to understand the effect of slow and mismatched rise times. In the remainder of this section, the impact of slew rate on the operation of the PWM will be analyzed in more detail, both from the perspective of timing and load power.

3.3.1 Timing Impact of Finite Slew Rate and Slew Rate Mismatch

If slew rate on/off matching is provided in the data sheet, as it is for TPS1H100-Q1, we can consider the worst-case impact on pulse width from both propagation delay mismatch and slew-rate mismatch. If we consider pulse-width as the duration from the rising and falling edges taken at 50% of max value we get:

$$t_{d(SRD)} = \frac{\left(t_{rise(OUT)} - t_{fall(OUT)}\right)}{2} = \frac{V_{vs}}{2}\left(\frac{1}{SR_{ON}} - \frac{1}{SR_{OFF}}\right) \tag{24}$$

$$SR_{OFF} = SR_{ON} + SR_{match} \tag{25}$$

$$t_{d(SRD)} = \frac{\left(t_{rise(OUT)} - t_{fall(OUT)}\right)}{2} = \frac{V_{vs}}{2}\left(\frac{SR_{match}}{SR_{ON}^2 + SR_{ON} \cdot SR_{match}}\right) \tag{26}$$

where SR_{match} could be positive or negative. If we consider both slew-rate and propagation-delay mismatch, the output pulse-width expression follows:

$$t_{pw(OUT)} = t_{pw(IN)} \pm \left(t_{d(SRD)} + t_{d(PWD)}\right) \tag{27}$$

To illustrate the effect, we use specification of TPS1H100-Q1 and Equation 24 to understand the slew-rate mismatch relationship with PWM accuracy.

- HSS supply voltage: V_{vs} =*10 V and 40 V*
- Pulse-width distortion: $t_{d(PWD)}$ = *±50 µs* (TPS1H100 min/max spec)
- ON Slew rate: SR_{ON} = *0.36 V/*µs
- Slew rate matching: SR_{match} = *0.15 V/*µs
- Duty cycle: D_{IN} = *50%*

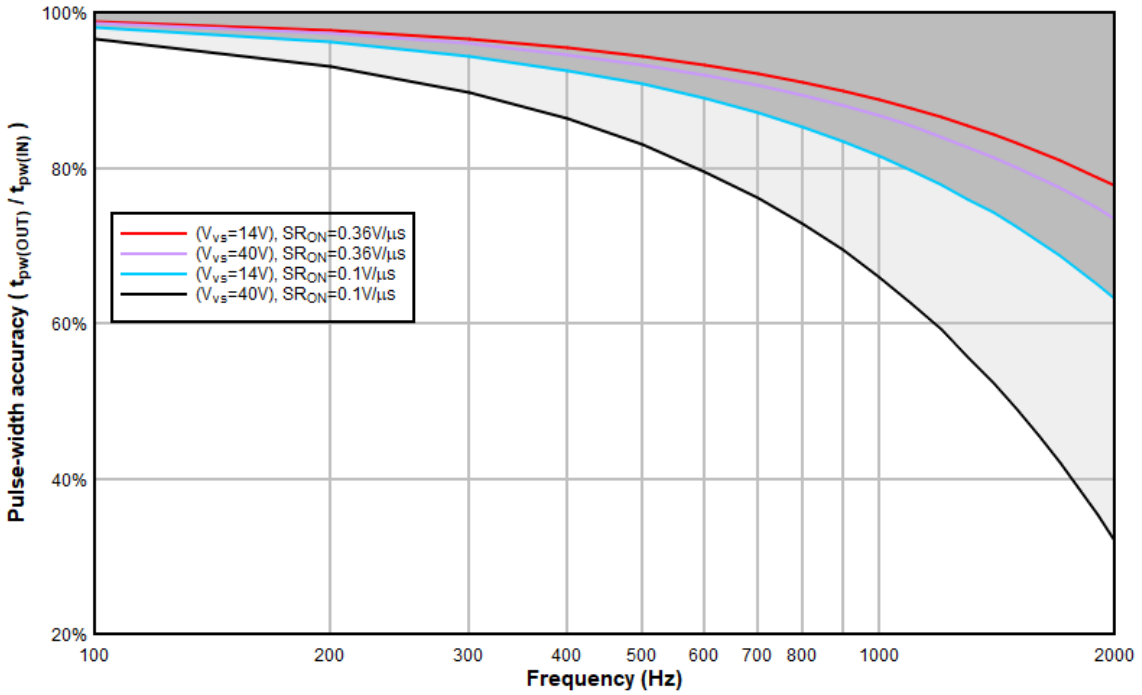


Figure 3-7. Input-to-Output PW Accuracy Over Supply Voltage, Considering Slew Rate and Delay Mismatch

Clearly, if we consider both PWD and slew rate mismatch this places additional limits on feasible PWM frequency especially at higher supply voltages. It is important to note that each high side switch can have varying switching characteristics. Refer to the device parameters and calculation methods above to determine if a specific set of PWM loading conditions is feasible for a selected high side switch.

3.3.2 Impact of Finite Slew Rate on Resistive Load Power

In earlier sections of this report, it was shown that as PWM frequency increases the effects of PWD on load power increases causing significant divergence from the calculated ideal power.

A high side switch's finite slew rate introduces additional challenges that deviates true load power from an ideal case. Unlike PWD, which can either increase or decrease delivered load power, finite slew-rate *always* results in reduced load power compared to an ideal high side switch as the rise times reduce the time when the full input voltage is present across the load. As frequency increases, the rise and fall times account for more and more of the output ON pulse.

Figure 3-8 defines timing parameters used for analysis.

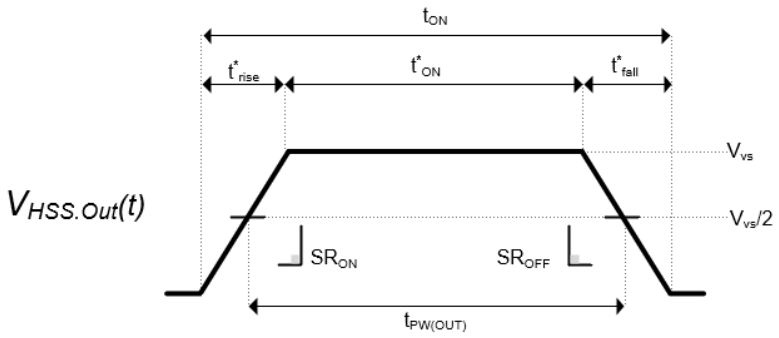


Figure 3-8. Timing Definition for Resistor Power Analysis

t_{ON} is the total duration of the ON cycle pulse.

- t'_{ON} is the total duration where output is at final voltage

- $t_{pw(OUT)}$ is the output pulse width
- $t_{rise,fall}$ are rise and fall times calculated from device slew rate, such that

$$t_{ON} = t'_{ON} + t_{rise} + t_{fall} \tag{28}$$

$$t_{ON} = t_{pw(out)} + \frac{(t_{rise} + t_{fall})}{2} \tag{29}$$

The average dissipated power in a resistor is $R \cdot I_{AVG}{}^2$. When considering the slew rate, voltage becomes a linear function of time during rise and fall times. By decomposing the resistor power into the rising, falling, and steady periods of output voltage, we can calculate average load power for an arbitrary resistor with a severely distorted output pulse.

$$P_{avg} = D \cdot \frac{1}{t_{ON}} \int_0^{t_{ON}} dP \cdot dt \tag{30}$$

$$P_{avg} = D \cdot \frac{2}{R_{load} \cdot t_{ON}} \int_0^{t_{ON}} V(t) \cdot dt \tag{31}$$

Splitting up the ON cycle waveform yields

$$P_{avg} = D_{out} \cdot \frac{2}{R_{load} \cdot t_{ON}} \left(\int_{t_0}^{t_1} V(t) \cdot dt + \int_{t_1}^{t_2} V(t) \cdot dt + \int_{t_2}^{t_3} V(t) \cdot dt \right) \tag{32}$$

Even if rise and fall waveforms were complex, it would not be a good use of time to start integrating at this point. As we are assuming the rise and fall periods are linear (constant slew rates), our output waveform is trapezoidal and the power calculation simplifies.

$$P_{avg} = D_{out} \cdot \frac{2}{R_{load} \cdot t_{ON}} \left(\frac{V_{vs}^2}{4} (t_{rise} + t_{fall}) + V_{vs}^2 \cdot t'_{ON} \right)$$

, where V_{vs} is the supply voltage. This can be further simplified to: (33)

$$P_{avg} = \frac{D_{out} \cdot V_{vs}^2}{R_{load} \cdot t_{ON}} \left(t_{ON} - \frac{t_{rise} + t_{fall}}{4} \right) \tag{34}$$

As slew rates increase, power dissipated in the resistive load is reduced. At the point where the output only reaches V_{vs} output power is halved. If frequency is increased further than this point, slew rates will further reduce power as the output will never reach V_{vs}.

3.3.3 Impact of Slew Rate on LED Power

Similarly, we can perform this power analysis for LED applications. For a prototypical LED array, we relate the supply voltage to the forward current at the corresponding voltage as follows, where *N* is the number of series LEDs per string and *M* is the parallel strings.

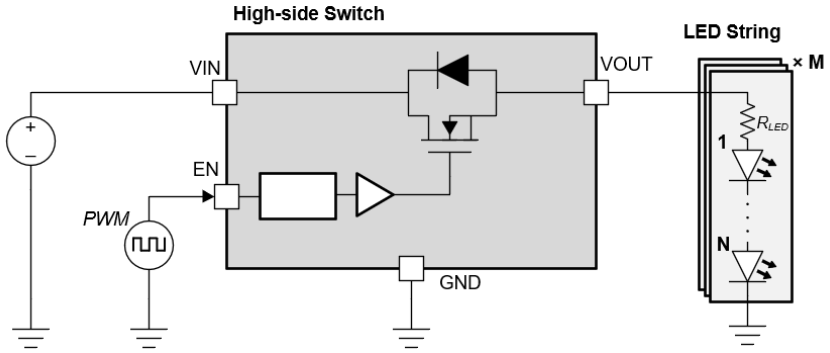


Figure 3-9. High-Side Switch Driving LED Load

$$V_{vs} \approx M(N \cdot V_F + I_F \cdot R_{LED}) \quad (35)$$

A CREE JB2835B 3-V, 0.5-W class LED I-V characteristic is shown below. Because diode voltage and current change with time due to the slewed waveform of *Vvs*, the LED power dissipation is better to be analyzed with via modeling than by calculating by hand. We can simplify the V-I curve by 1st order least-squares regression which gives a turn-on voltage of ~2.6 V and which matches the true performance of the device with little variance.

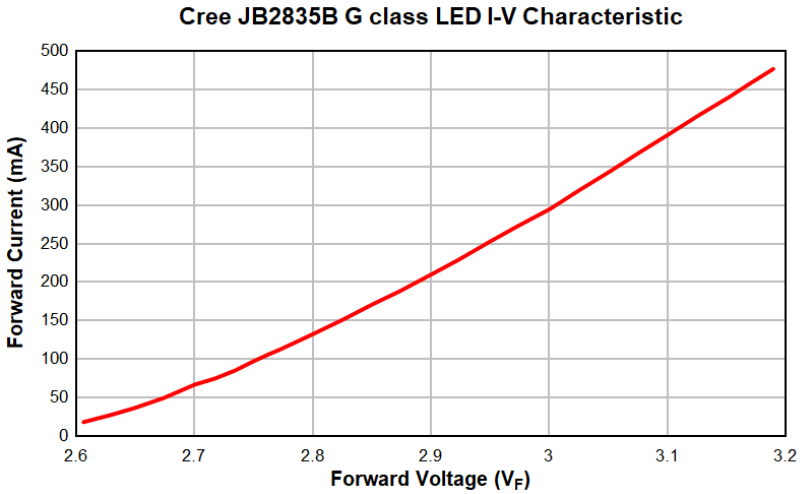


Figure 3-10. Cree JB82835 0.5-W LED I-V Characteristic

For most purposes, assuming the current is already at its peak as soon as the diodes become forward biased is fairly accurate and enables quick estimation.

$$I_F \approx 0.8 \cdot V_F - 2.11 \quad (36)$$

$$I_F \approx I_{F(OP)} @ V_{F(op} \quad (37)$$

The main difference from the restive load case is that no current and thus no power is delivered before the supply potential can forward bias the LED string. The LED string(s) begin conducting once the output voltage exceeds the sum of the LED forward voltages $N \cdot V_F$.

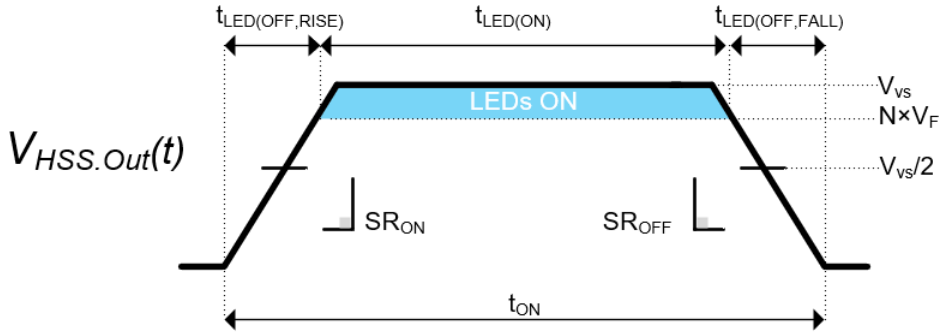


Figure 3-11. Timing Definitions for LED Power Analysis

Average power for one cycle is based on the number of parallel LED strings as well, the time-dependent LED forward current, and the HSS output voltage which is distorted by slew rate and PWD, where *M* is the number of parallel LED strings and N the number of series LEDs.

$$P_{LED(AVG)} = V_{F(AVG)}.N \cdot M \cdot I_{F(AVG)} \quad (38)$$

$$V_{VS}(t) = N \cdot V_F(t) + I_F(t) \cdot R_{LED} \quad (39)$$

$$I_F(t) = f\left(V_F(t)\right) \quad (40)$$

$$P_{LED(AVG)} = \frac{D}{t_{ON}} \int_0^{t_{ON}} dV_F(t) \cdot I_F(t) \cdot dt + \int_0^{t_{ON}} V_F(t) \cdot dI_F(t) \cdot dt + \quad (41)$$

LED current of Cree JB2835D G-class LED string was modeled in a computational tool, according to the design target below

- Supply voltage: V_{vs} = 12 V
- # of Series LED: N =4
- # of Parallel Strings: M = 1
- LED operating point: $V_{F(OP)}$ = 2.75 V , $I_{F(OP)}$ = 95 mA
- Current limiting resistor: R_{LED} = 3 Ω
- HHS Slew rate: SR_{ON} = 0.36 V/ µs

LED current in the string is shown in Figure 3-12 to Figure 3-14. As pulse-width decreases, either by increasing the PWM frequency or decreasing duty cycle, the LEDs spend less and less time of the output pulse above their

forward voltage. In Figure 3-13, the diodes can no longer become forward biased during the ON pulse and stay off.

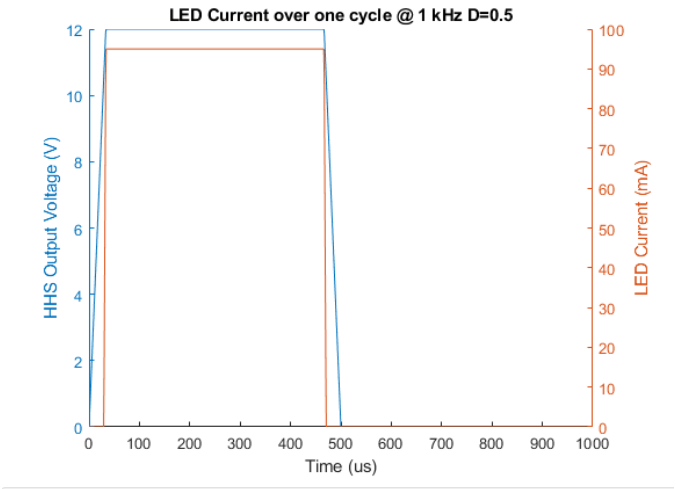


Figure 3-12. TPS1HA08-Q1 Driving LED String Sample Design, *f* = 1 kHz , D = 50%

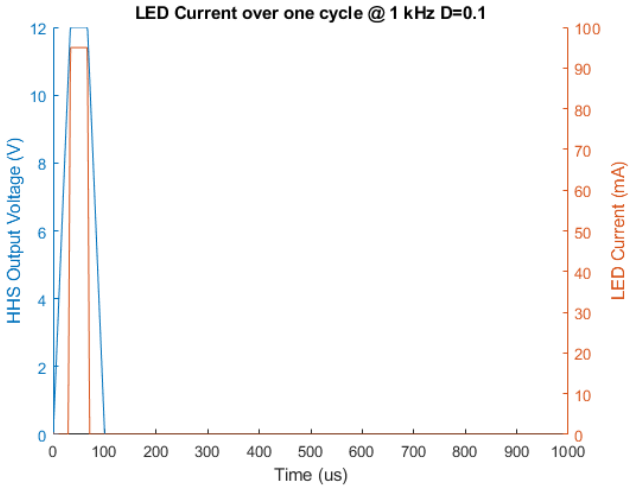


Figure 3-13. TPS1HA08-Q1 Driving LED String Sample Design, *f* = 1 kHz , D = 10%

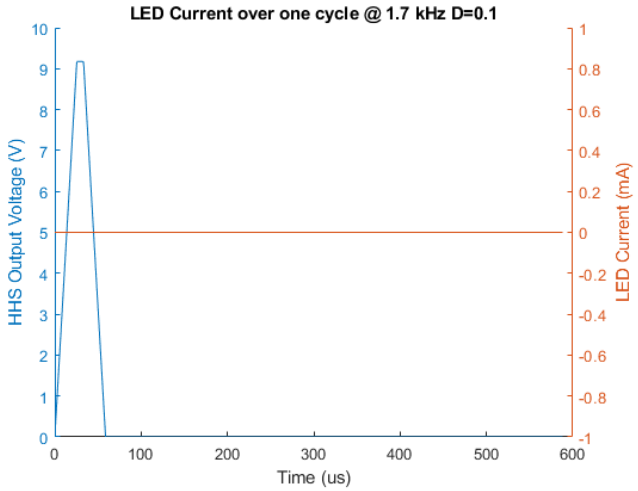
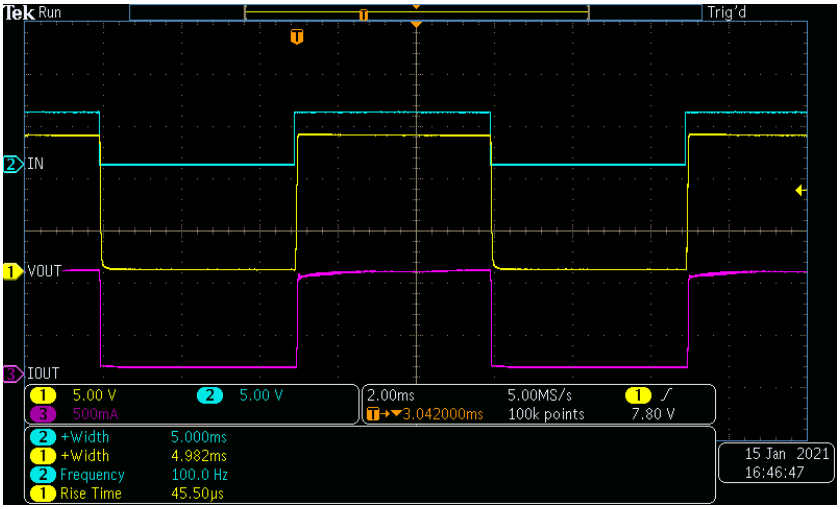
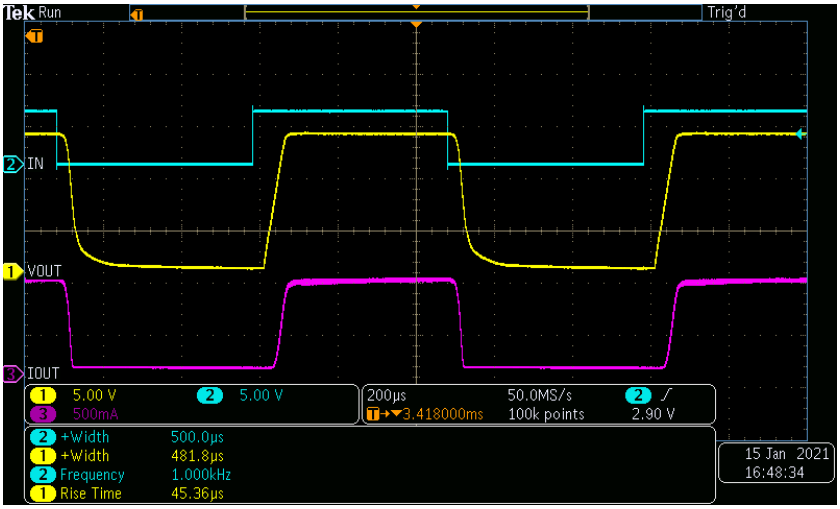


Figure 3-14. TPS1HA08-Q1 Driving LED, Insufficient Pulse-Width, *f* = 1.7 kHz , D = 10%

This design was recreated on the bench with a > 500-mA LED forward current and run for several PWM frequencies across several duty cycles.

These results match the Cree model at input pulse widths of 50 µs. At 1 kHz and up, PWD was noticeably worse and would no longer conduct.





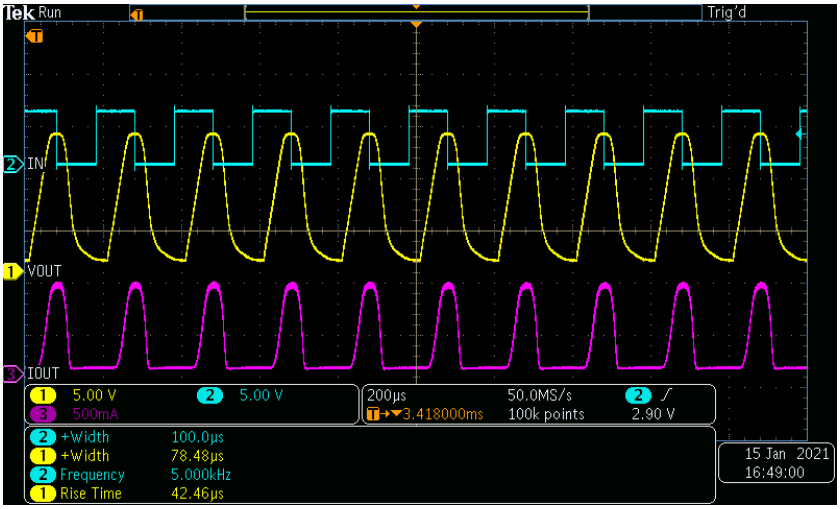


Figure 3-15. Bench Results of 12-V, 500-mA PWM Diode Load Over Frequency

4 System-Level Considerations

4.1 Diagnostics and Protection

TI's portfolio of smart high side switches offer integrated diagnostics and protection features which protect, monitor, and feedback device performance during operation. This section will explore these features with implications on PWM operation.

4.1.1 Analog Current Sense

Integrated analog current sense functionality allows the device to measure and feedback operating parameters including load current. High accuracy and fast response of the analog sense circuit enables closed-loop control of the high side switch. TPS1AH08-Q1 is one HSS that offers analog sense output that can measure supply voltage, output current, and IC temperature, and will be used as an example in this section.

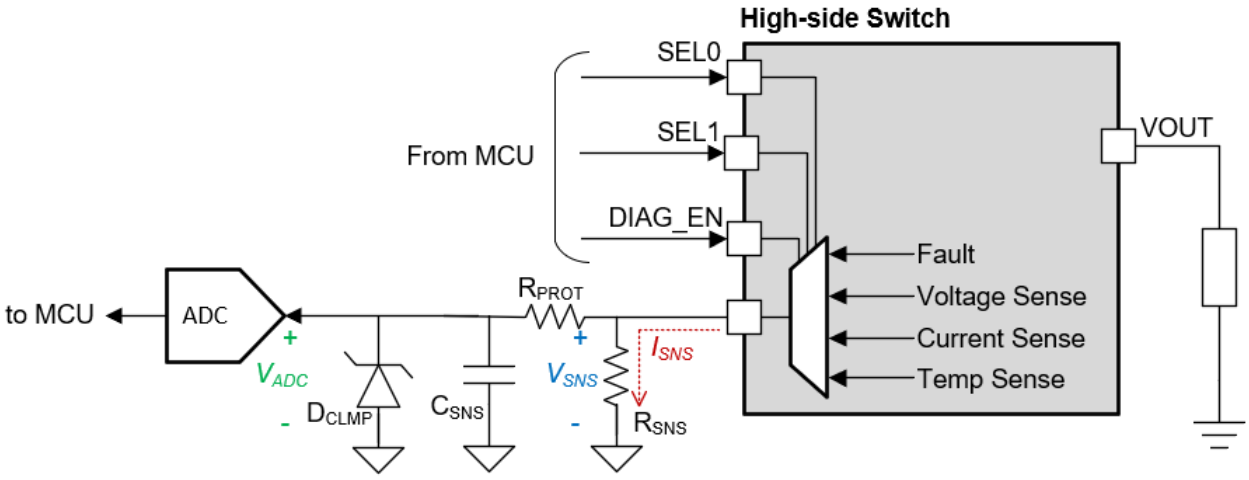
The analog sense circuit converts its measured parameter into a current according to the specified transfer function. The transfer function of TPS1HA08 is shown in Table 4-1.

Table 4-1. TPS1HA08 analog Sense Transfer Functions

PARAMETER	TRANSFER FUNCTION
Load current	$I_{SNSI} = I_{OUT} / 4600$
Supply voltage(1)	$I_{SNSV} = (V_{BB}) \times dI_{SNSV} / dV$
Device temperature	$I_{SNST} = (T_J – 25°C) \times dI_{SNST} / dT + 0.85$

The sense current I_{sns} is converted to an analog voltage by the external R_{sns} resistor and then passed on to an ADC, either discrete or internal to a microcontroller. Designers should select the value of R_{sns}based on the input range and resolution of the ADC, as well as the possible range of the particular parameter or parameters (if multiplexed) the HSS will see. The tolerance of R_{sns} should also be considered as it has a direct impact on total analog sense accuracy.

For TPS1HA08-Q1, the analog sense outputs a current I_{SNSFH} ~7 mA when there is a fault detected. Device specifications for TPS1HA08-Q1 set the maximum steady-state output current at 10 A, though the analog sense is capable of measuring current higher than this. SNS output value should be clamped (e.g. by Zener diode) to avoid exceeding the input range of the ADC if output current of the high side switch jumps unexpectedly.



Adapted from TPS1HA08 data sheet

Figure 4-1. HSS Multipurpose Analog Sense System

In a example application, the designer needs the ability to collect current, voltage, and temperature measurements. This fictitious engineer targets 50-mA output current resolution. The supply voltage for logic

is 3.3 V, so AVDD 3.3-V supply is assumed for the converter as well. The system limits along with the corresponding sense currents are listed.

- Peak output current: I_{OUT} = 5 A, I_{SNS} = 1.10 mA
- Peak Temp: Tj=150°C, I_{SNS} = 2.25 mA
- Peak Supply Voltage: V_{vs} = 15 V, I_{SNS} = 1.29 mA
- SNS Fault current: I_{SNSFH} = 6.9 mA

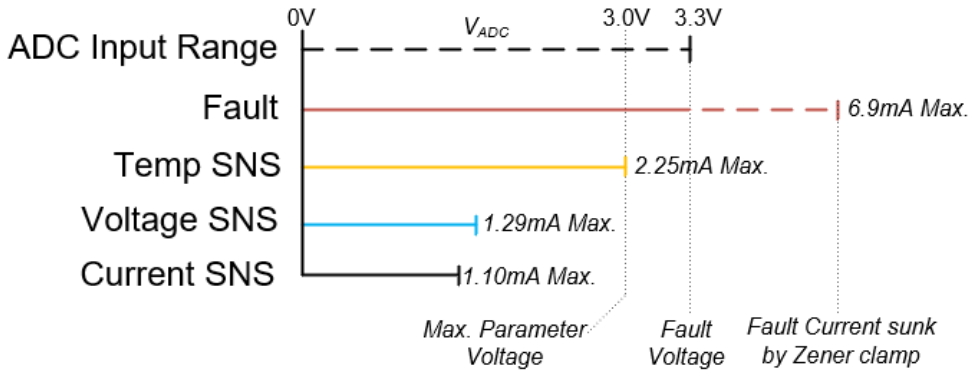


Figure 4-2. ADC Range Allocation

We can determine the maximum feasible value of R_{sns} possible based on the input range of the ADC and the SNS fault current, which is the absolute maximum. In order to minimize the resolution, the max SNS voltage range is set 10% under the input range of the single-ended ADC and a Zener clamps the fault current I_{SNSFH} to 3.3 V. Without the Zener, the ADC could be damaged as the input voltage would far exceed the device limits. The 300-mV difference allows plenty of headroom to prevent false fault detection.

$$R_{SNS(MAX)} = \frac{V_{AVDD(ADC)}}{\max(I_{SNS})} \tag{42}$$

The analog sense output is gated by both EN and DIAG_EN. The requirement of DIAG_EN allows a controller to multiplex analog sense outputs from several HSS onto a single ADC. After a rising edge of EN, the sense output current, I_{SNS} , settles after a certain time. For TPS1HA08, the maximum settling time of I_{SNS} is 180 µs. Since PWM operation implies that EN is constantly driven high or low, the sense settling time affects every switching cycle ON period where diagnostics are enabled.

A low pass is recommend to filter transients or interference on the analog sense output voltage. In TPS1AH08-Q1, a 10 - 15-kΩ resistor $R_{PROT}$is suggested to protect the HSS pins. Together with filter capacitor, C_{SNS}, the RC filter is formed. If there is a long lead or trace from the HSS sense pin to the ADC input, the sense resistor and RC filter should be placed close to the ADC prevent interference.

The transfer function of the sense current to the voltage at the ADC input is

$$H(j\omega) = \frac{V_{ADC}(j\omega)}{I_{SNS}(jw)} = \frac{R_{SNS}}{(R_{PROT}+1)C_{sns}j\omega + 1} \tag{43}$$

The sense LPF 3dB cutoff frequency is then

$$f_c = \frac{1}{2\pi(R_{PROT}+1)C_{sns}} \tag{44}$$

R_{PROT} and C_{SNS} should be selected such that the $f_{pwm} \ll f_c$. By a rule of thumb, setting the cutoff frequency at least one decade above the PWM frequency ensures good input/output matching and no attenuation.

For example, if operating at 1-kHz PWM frequency, we can find a suitable C_{SNS} value for a fixed R_{PROT} of 10 kΩ. By using a rule of thumb we set our target cutoff frequency for the LPF at $f_c \geq 10 \cdot f_{PWM}$. From there,

$$C_{SNS} \leq \frac{1}{2\pi \cdot R_{PROT} \cdot 10 \cdot f_{PWM}} \tag{45}$$

$$C_{SNS} \leq 1.59\text{nF} \tag{46}$$

From there we found an acceptable value of C_{SNS} that ensures sufficient bandwidth of the LPF as not to attenuate the SNS signal which is at PWM frequency. The RC filter values can of course be tuned if the designer wishes to filter certain frequencies by the discrete RC filter rather than in the software domain. If a designer wishes to do all filtering digitally within the ADC/controller, a sense LPF does not need to be used.

4.2 Dimming Ratio

One key advantage of PWM is the ability to change the average output of the energy dissipated by the load by varying only the duty cycle. Systems may need a wide range luminous or thermal outputs which helps define the duty cycle range.

This is commonly referred to as the dimming ratio or contrast ratio in lightning applications. Dimming ratio, *DR*, is proportional to the power dissipated in a resistive element and the luminous flux of an LED.

$$DR = \frac{D_{MAX}}{D_{MIN}} = \frac{t_{PW(max)}}{t_{PW(min)}} \tag{47}$$

$$\text{For a resistive load,} \quad \frac{P_{AVG(HOT)}}{P_{AVG(COLD)}} = \frac{D_{MAX}}{D_{MIN}} \tag{48}$$

$$\text{For an LED load,} \quad \frac{\Phi_{AVG(BRIGHT)}}{\Phi_{AVG(DIM)}} \approx \frac{D_{MAX}}{D_{MIN}} \tag{49}$$

For *DIM* and *COLD* extremes of operation, the pulse widths will be the smallest. High side switch timing limitations on minimum pulse width are used to set D_{MIN} and PWM frequency.

4.3 Side-Stepping Frequency Limitations

In some applications, systems may need to operate at PWM frequencies beyond the 1-2 kHz which most HSS are limited to, but still maintain the robust diagnostics and protection features of a high side switch.

This can be accomplished by reassigning the PWM switching duties from the HSS to a separate low-side switch, such as ULN2003A, which is capable of much higher-frequency operation. For higher-current applications, N-ch FET based low-side driver such as DRV103 may be used. This topology is shown in Figure 4-3. With this dual-IC strategy, a designer still must consider frequency dependent power dissipation and thermals in the HSS, but not HSS switching losses.

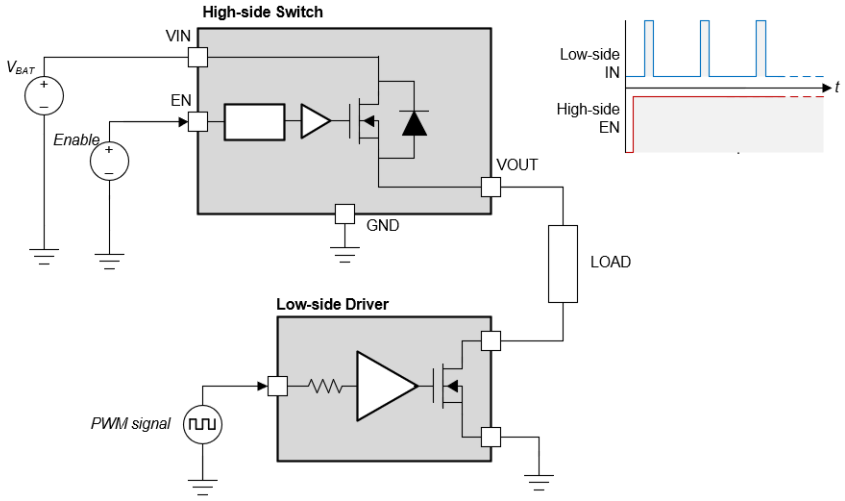


Figure 4-3. Dual-Driver Strategy for High Frequency PWM

5 References

- Texas Instruments, TPS1HA08-Q1 data sheet
- Texas Instruments, TP4H000-Q1 data sheet
- Texas Instruments, TPS1H100-Q1 data sheet
- Cree, Inc., Cree J-Series 2835 3-V LEDs data sheet

Additional Resources

For more information on using TI smart high side switches, please see the following:

- 11 Ways to Protect Your Power Path
- How to Drive Resistive, Inductive, Capacitive, and Lighting Loads

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