Application Report

Stability Analysis and Design of D-CAP2 and D-CAP3 Converter – Part 1: How to Select Output Capacitor

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ABSTRACT

D-CAP series control schemes are widely used in TI buck controllers/converters due to the advantages of good dynamic performance and less external components. In D-CAP2 and D-CAP3 schemes, the limitation on the use of small ESR capacitor is broken through with the internal *ripple injection* circuit. The frequency loop models of D-CAP and D-CAP2 control schemes have been studied in some previous application reports. However, the application design and component choose methods from loop stability view are still obscure for customers. In this application report, the principle of loop design for D-CAP2/D-CAP3 converters are introduced. Combined with the loop model of D-CAP control, the method to choose components for application are proposed. A phase margin estimation method is further researched to evaluate the stability with chosen components. Finally, a comprehensive application design example is given as design guide.

To be noted, the method proposed in this application report can be only used as a reference material. Due to the simplification in deduction and non-ideal factors in reality, the calculated results will have difference with bench test. Also, the application design method for converter with feed forward capacitor isn't included in this application report.

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Trademarks

1 Introduction

D-CAP series control schemes are widely used in notebook, server, EP power and many other areas due to the advantages of good dynamic performance and less external components [1 and 2]. Different from the compensation with error amplifier in voltage mode and current mode, the zero formed by output capacitor ESR is used for loop compensation in the original D-CAP control [3 and 4]. With ESR zero after LC double poles, the slope of loop gain magnitude becomes -20dB/decade at crossover frequency, which ensures the system phase margin. For the application with MLCC or other small ESR capacitor, external or internal *ripple injection* circuit can be used to generate a zero instead of the ESR zero in D-CAP/D-CAP2/D-CAP3 control [5 and 6]. But if the inductor and output capacitor are not chosen properly and crossover frequency is lower than the frequency of *ripple injection* zero, a -40dB/decade slope at crossover frequency will happen and cause insufficient phase margin. An application design method is proposed for D-CAP2/D-CAP3 buck converter in this application report to ensure enough phase margin and system stability.

2 Open Loop Frequency Response of D-CAP2 and D-CAP3 Converter

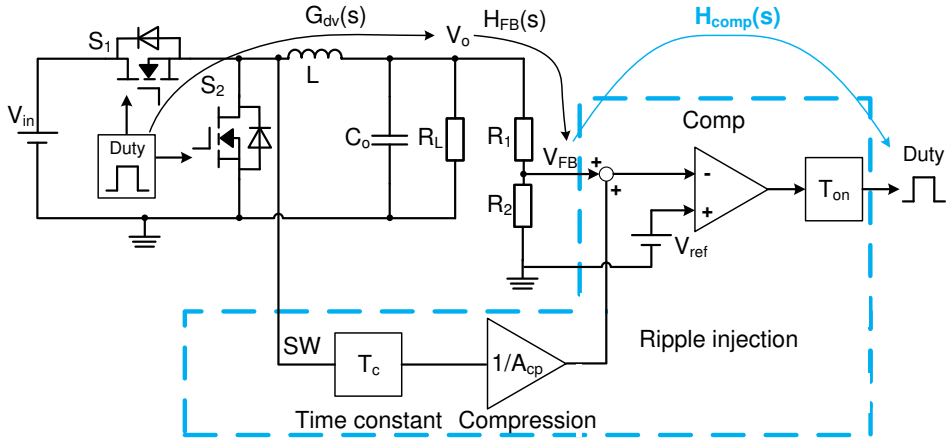

Figure 2-1. Control Diagram of D-CAP2 Converter

Diagram of buck converter with D-CAP2 control scheme is shown as Figure 2-1 . The open loop transfer function was derived in application report [2], as shown in Equation 1.

$$G_{open\text{-}DCAP2}(s)=G_{dv}(s)H_d(s)\underbrace{(1+sT_c)\frac{A_{cp}}{V_{in}}H_{FB}(s)}_{H_{comp}(s)} \quad (1)$$

where $G_{dv}(s)$ is the transfer function from Duty to V_o, well known using *state-space averaging model*.

$H_d(s) = e^{-sTon/2}$: Delay factor of fixed on time

T_c: Time constant block of ripple injection circuit in D-CAP2

A_{cp}: Voltage compression block of ripple injection circuit in D-CAP2

$H_{FB}(s)$: Transfer function of feedback divider network

The expression of $G_{dv}(s)$ is shown as Equation 2.

$$G_{dv}(s)=\frac{V_{in}\left(1+\frac{s}{\omega_{esr}}\right)}{1+2\sigma\frac{s}{\omega_0}+\left(\frac{s}{\omega_0}\right)^2} \quad (2)$$

where

$$\sigma = \frac{\sqrt{L/C_o} + R_L(r_L + r_c)\sqrt{C_o/L}}{2R_L\sqrt{1 + r_L/R_L}} \quad (3)$$

R_L is the load resistance, r_L is DC resistance of the inductor, r_c is ESR of output capacitor.

A pair of double poles (conjugate poles) and a zero formed by ESR of output capacitor are included in the transfer function $G_{dv}(s)$. The angular frequency of the double poles and the zero formed by ESR are shown as Equation 4 and Equation 5.

$$\omega_0 = \sqrt{\frac{1 + r_L/R_L}{LC_o}} \approx \sqrt{\frac{1}{LC_o}} \quad (4)$$

$$\omega_{esr} = \frac{1}{C_o r_c} \quad (5)$$

A zero is formed by the time constant block of ripple injection in D-CAP2 control mode, the angular frequency of the zero is:

$$\omega_{RI} = \frac{1}{T_c} \quad (6)$$

ω_{esr} is at high frequency range in most cases. ω_0 and ω_{RI} are the dominant poles and zero to determine bandwidth and phase margin. The bode plot of open loop transfer function for D-CAP2 converter is shown as Figure 2-2.

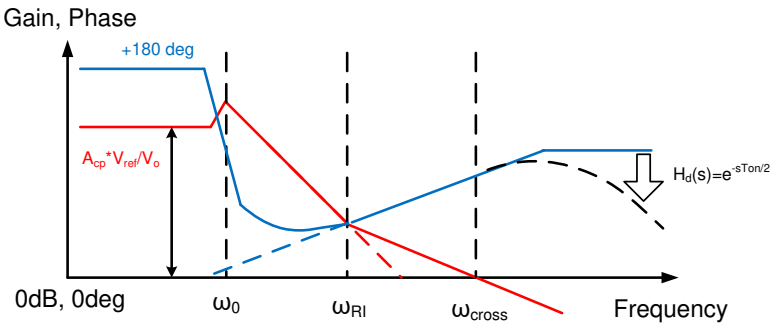

Figure 2-2. Bode plot of D-CAP2 Converter

To enhance DC accuracy of output voltage, D-CAP3 is proposed and widely used in TI's current products. Compared with D-CAP2, the DC error correction performance is further improved in D-CAP3. By adding additional poles and zeros at low frequency range, the gain at low frequency range is increased to achieve better ability for DC error correction. But the characteristics of gain and phase at middle frequency and high frequency are almost same as D-CAP2 converter. The bode plot of open loop transfer function is shown as Figure 2-3.

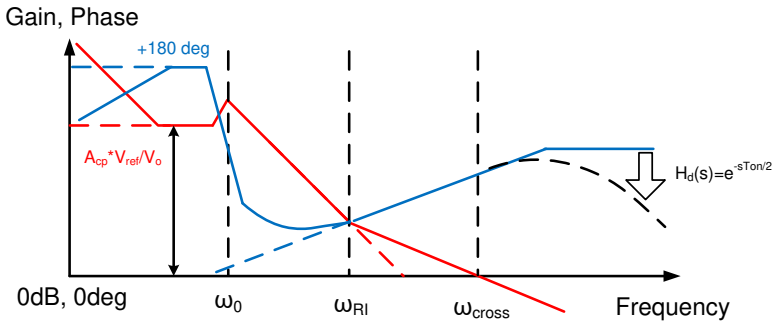

Figure 2-3. Bode plot of D-CAP3 Converter

Phase margin is the phase at crossover frequency and it is one of the most important value for system stability evaluation. Since the crossover frequency is at middle frequency or high frequency, the impacts of additional zeros and poles at low frequency in D-CAP3 control mode on stability analysis can be ignored. Thus the application design method for D-CAP3 stability is same as that of D-CAP2. The analysis and design method in this application report can be applied on converters using either D-CAP2 or D-CAP3 control.

3 Method to Choose LC Value for Loop Stability

For system loop stability, a -20dB/decade slope near crossover frequency is ideal for loop gain, since that can bring sufficient phase margin [7].

3.1 Limits of Output Capacitance

In buck converters, the slope of open loop gain can be seen as -40dB/decade after double poles frequency ω_0. When the ripple injection zero frequency ω_{RI} is smaller than bandwidth, the loop gain will cross 0dB with -20dB/decade slope, as shown in Figure 3-1. Otherwise, it will cross 0dB with -40dB/decade slope, as shown in Figure 3-2.

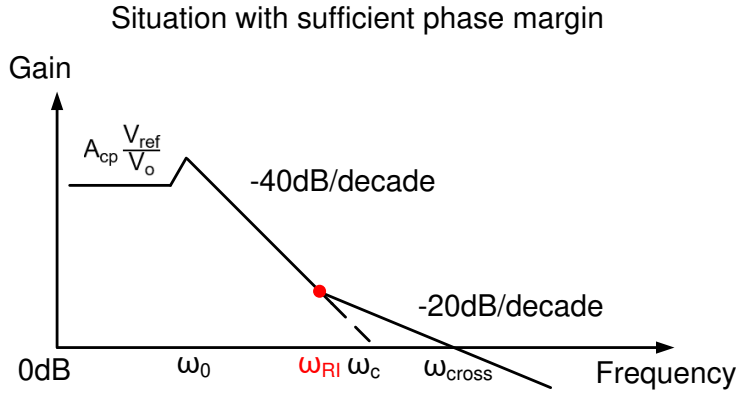

Figure 3-1. Loop Gain of D-CAP2 Converter with -20dB/Decade at 0dB

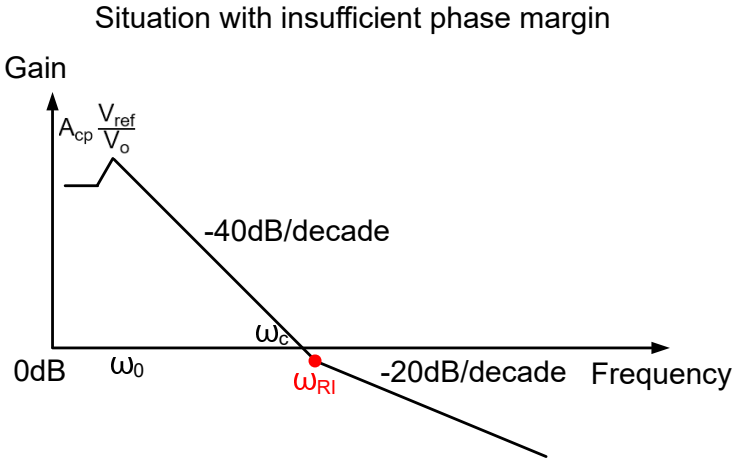

Figure 3-2. Loop Gain of D-CAP2 Converter with -40dB/Decade Slope at 0dB

Assuming the loop gain drops with -40dB/decade slope after ω_0, the cross frequency at 0dB is denoted as ω_c. From Figure 3-1 and Figure 3-2, it's known that Equation 7 is needed for a -20dB/decade cross.

$$\omega_c > \omega_{RI} \tag{7}$$

To calculate the frequency ω_c, we can first get Equation 8 with ω_c

$$\frac{20\lg\left(A_{cp}\frac{V_{ref}}{V_o}\right)-0dB}{\lg(\omega_0)-\lg(\omega_c)} = -40dB/decade \tag{8}$$

Then ω_c can be derived as:

$$\omega_c = \sqrt{A_{cp}\frac{V_{ref}}{V_o}} \times \omega_0 \tag{9}$$

Substituting Equation 4 and Equation 9 into Equation 7, Equation 10 can be derived to ensure -20dB/decade cross.

$$C_o < \frac{A_{cp}V_{ref}}{LV_o\omega_{RI}^2} \tag{10}$$

If further considering the DCR of inductor r_L, Equation 10 will become:

$$C_o < \frac{A_{cp}V_{ref}}{LV_o\omega_{RI}^2}\left(1+\frac{r_L I_{out}}{V_o}\right) \tag{11}$$

Since the inductance L is normally designed with the target to let inductor current ripple be about 20%-40% of max load current rating. With Equation 10 or Equation 11, the upper limit of capacitance value can be got for loop stability.

In D-CAP2/D-CAP3 control, A_{cp} and ω_{RI} are the parameters determined by the internal circuit inside converters. Table 3-1 shows the A_{cp} and ω_{RI} of some devices with D-CAP2 or D-CAP3 control.

Table 3-1. A_{cp} and ω_{RI} of Several Devices

Device	A_{cp}	ω_{RI} (f_{sw}=600kHz)
TPS568230	29.3	270krad/s (43kHz)
TPS566235	29.36	198krad/s (31.5kHz)
TPS566231	36	247krad/s (39.3kHz)

Note: ω_{RI} is already given in some data sheets (sometimes named as time constant, it's the reciprocal of ω_{RI}). A_{cp} of a device can be estimated by checking the gain before double poles, which equals to $20\lg(A_{cp}*V_{ref}/V_o)$dB in bode plot.

From Equation 11, it can be found that smaller output capacitor tends to bring a -20dB/decade cross. But too small output capacitance will make the double poles frequency too high and increase the bandwidth a lot. That may also cause insufficient phase margin, since the phase will drop apparently at high frequency range due to the effects of delay factor. For D-CAP2/D-CAP3 mode converter, normally the bandwidth needs to be limited below $1/3*f_{sw}$. That corresponds to a lower limit for output capacitance.

To get the limit, first we can get the loop gain at ripple injection zero in Figure 3-1 as:

$$A_{RI}=\frac{A_{cp}V_{ref}\omega_0^{\,2}}{V_o\omega_{RI}^{\,2}} \tag{12}$$

Loop gain will drop with -20dB/decade slope from A_{RI} and cross 0dB at ω_{cross}:

$$\omega_{cross}=\frac{A_{cp}V_{ref}\omega_0^{\,2}}{V_o\omega_{RI}} \tag{13}$$

Limit the crossover frequency below $1/3*f_{sw}$ and the lower limit of output capacitance can be derived as Equation 15.

$$\omega_{cross}<\frac{2\pi f_{sw}}{3} \tag{14}$$

$$C_o>\frac{3A_{cp}V_{ref}}{2\pi f_{sw}LV_o\omega_{RI}} \tag{15}$$

Above all, the Equation 11 and Equation 15 are the upper limit and lower limit of output capacitance for loop stability.

3.2 Phase Margin Estimation Method

A phase margin estimation method is proposed in this section to help evaluating the components chosen with the method in previous section.

Based on the phase characteristics of poles and zeros, it can be derived that the phase of double poles, ripple injection zero, ESR zero and delay factor are as Equation 16 through Equation 19 at crossover frequency.

$$\text{Phase}_{DP}(\omega_{cross})=-\tan^{-1}\left(\frac{2\sigma\omega_0\omega_{cross}}{\omega_0^{\,2}-\omega_{cross}^{\,2}}\right) \tag{16}$$

$$\text{Phase}_{RI}(\omega_{cross})=\arctan\left(\frac{\omega_{cross}}{\omega_{RI}}\right) \tag{17}$$

$$Phase_{ESR}(\omega_{cross})=\arctan\left(\frac{\omega_{cross}}{\omega_{ESR}}\right) \quad (18)$$

$$Phase_{Delay}(\omega_{cross})=-\frac{T_{on}\omega_{cross}}{2}\frac{180}{\pi} \quad (19)$$

For D-CAP control schemes, the initial phase before double poles frequency is about 180 degree. Then we can calculate the phase margin:

$$PM(\omega_{cross})=180+Phase_{DP}(\omega_{cross})+Phase_{RI}(\omega_{cross}) +Phase_{ESR}(\omega_{cross})+Phase_{Delav}(\omega_{cross}) \quad (20)$$

If the components chosen can't ensure enough phase margin with Equation 20, it's recommended to recheck the calculated limits and reselect the capacitance. Basically, if the estimated crossover frequency is closer to 1/3 of crossover frequency, select larger capacitance. Otherwise select smaller capacitance.

The application design method and evaluation method above are only the reference for output capacitance choose. It needs to be verified with bench test due to the effects of parasitic parameters and some non-ideal situation.

4 Example of LC Design Method for D-CAP3 Converter

TPS568230 is used as the example. V_{in}=12V, V_o=1.5V, f_{sw}=600kHz, I_{outmax}=8A.

First, choose inductance to let the inductor current ripple equal to 20%-40% of max loading current. The inductance value can be derived as Equation 21.

$$L=\frac{(V_{in}-V_o)V_o}{V_{in}}\frac{1}{NI_{outmax}f_{sw}} \quad (21)$$

Substituting the parameters into Equation 21, it can be calculated that 0.68uH< L<1.36uH. Choose L=1uH. Choose inductor 744311100 and its DCR is 4.6mOhm. Substituting inductance and DCR into Equation 11 and Equation 15, we can get the range of output capacitance as 35uF< C_o<163uF.

Choose output capacitance C_o=110uF. Here 5 parallel 22uF MLCC with 10V rated voltage are used and ESR of each one is about 3mohm. The total ESR is 0.6mohm.

For the estimation of phase margin and crossover frequency, the degrading of inductor and capacitor needs to be considered. With only 1.5 V DC bias, the degrading of output capacitor can be ignored. Degrading curve of inductance with increasing current is shown in Figure 4-1. The inductance is about 0.86uH at 8A loading.

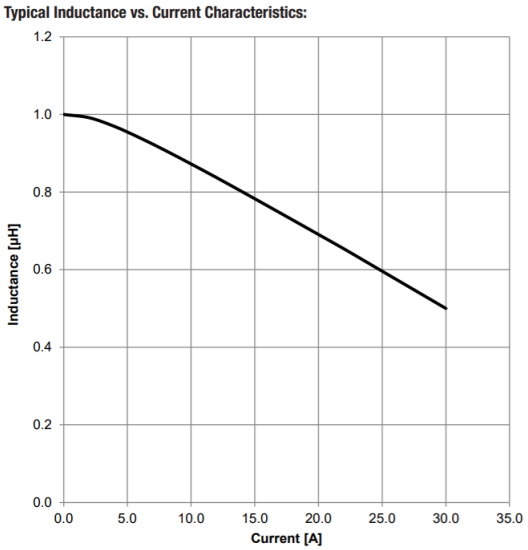

Figure 4-1. Degrading Curve of Inductance with Increasing Current

It can be calculated that the crossover frequency is 77kHz according to Equation 14 and phase margin is 57.7 degree according to Equation 19.

The application design method can be concluded as the flow chart in Figure 4-2.

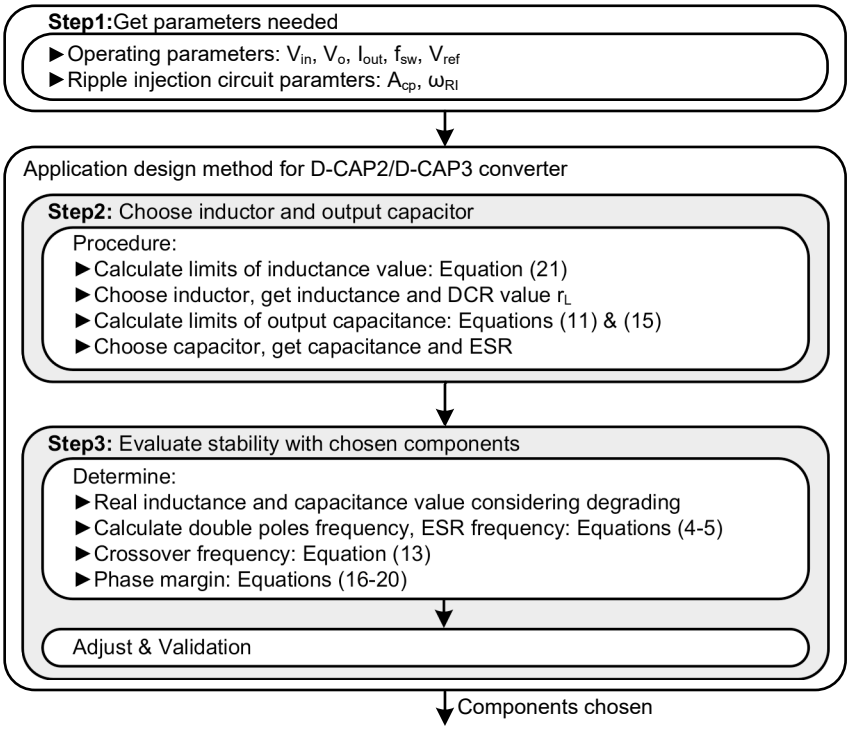

Figure 4-2. Flow Chart for Application Design of D-CAP2/D-CAP3 Converter

5 Simulation and Experimental Verification

The example in Section 4 is verified by Simplis simulation first. As shown from Figure 5-1 that the crossover frequency is 75.9kHz and the phase margin is 55 degree with chosen components. That accords with the theoretical estimated results 77kHz and 57.7 degree and it's proven that phase margin is enough with the proposed application design method.

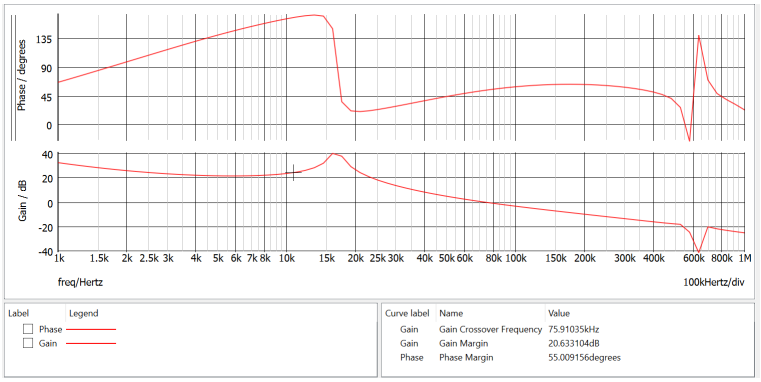

Figure 5-1. Bode Plot from Simplis Simulation

The experiment result is shown in Figure 5-2. The crossover frequency and phase margin are 82.99kHz and 52.2 degree respectively, which are close to the theoretical analysis and also prove the effectiveness of proposed application design method for stability.

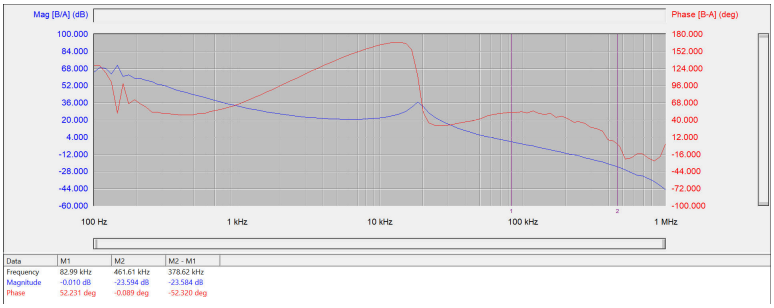

Figure 5-2. Bode Plot from Experimental Verification

6 Summary

An application design method is proposed in this application report for D-CAP2/D-CAP3 converters based on loop stability analysis. The method is based on two principles to achieve enough phase margin: First, ensure -20dB/decade slope at crossover frequency. Second, limit bandwidth below 1/3*f_{sw}. Combined with the loop characteristics of D-CAP2/D-CAP3 converter, the limits for output capacitance are derived. For evaluation of the chosen components value, a phase margin estimation method is further proposed. Finally, a detailed flow chart is given to help designing application of D-CAP2/D-CAP3 converter. The proposed methods are verified by both simulation and experiment.

Note

The internal ramp inside some D-CAP converters for jitter performance improvement will decrease phase margin a little. For those types of converters, please leave more margin from limits when choosing output capacitor. Meanwhile, the calculated phase margin needs to subtract about 5-10 degree for the stability evaluation.

7 References

1. M. Lin, T. Zaitsu, T. Sato, and T. Nabeshima, *Frequency Domain Analysis of Fixed On-Time with Bottom Detection Control for Buck Converter*, IEEE IECON2010, pp.475-479
2. Texas Instruments, *D-CAP2™ Frequency Response Model based on frequency domain analysis of Fixed On-Time with Bottom Detection having Ripple Injection* application report.
3. Texas Instruments, *Loop Stability Analysis of Voltage Mode Buck Regulator with Different Output Capacitor Types – Continuous and Discontinuous Modes* application report.
4. Robert Sheehan, *Understanding and Applying Current-Mode Control Theory*, Power Electronics Technology Exhibition and Conference, Nov. 2007
5. Texas Instruments, *Adaptive Constant On-Time (D-CAP™) Control Study in Notebook Applications* application report.
6. Texas Instruments, *D-CAP Mode with all-Ceramic Output Capacitor Application* application report.
7. Gene F. Franklin, J. David Powell, Abbas Emami-Naeini, *Feedback Control of Dynamic Systems*.

8 Appendix A

For TPS568230 I_{outmax}=8A, V_{ref}=0.6V. PM is the phase margin of converter. All the capacitors used in the validation are MLCC. With POSCAP or electrolytic capacitors, the phase margin can be boosted with ESR zero and that could bring larger range of output capacitance values.

Table 8-1. Validation Results for the Proposed Methods

V_{in} (V)	V_o (V)	f_{sw} (kHz)	L_{limits} (uH)	L_{choose}(uH)	C_{limits} (uF)	C_{choose}(uF)	$PM_{estimated}$	$PM_{experiment}$
6	0.9	600	0.4-0.8	0.68	85-393	376	47.1°	52.9°
6	1.2	600	0.5-1	0.68	64-297	282	45.8°	51.9°
6	1.5	600	0.59-1.17	1	34-158	132	48.5°	46.9°
6	1.8	600	0.66-1.31	1	28-129	110	46.7°	47.1°
18	0.9	600	0.45-0.89	0.68	85-393	376	49.3°	53.9°
18	1.2	600	0.58-1.17	1	43-200	188	52.6°	54.4°
18	1.8	600	0.84-1.69	1.5	19-89	88	54.2°	48.1°

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