User's Guide

PoE Powered Devices Debug Guidelines

ABSTRACT

This document provides the debug process for TI Power over Ethernet (PoE) Powered Device (PD) designs. *Most* problems occur in the DC/DC design. PoE uses the IEEE802.3 standard that includes IC vendors and end-equipment designs, resulting in strict requirements for PoE operation. However, there are no such requirements on DC/DC design. Unfortunately, the complex nature of DC/DC design leaves less margin of error than one might expect, yet many degrees of freedom in design choices. This combination allows errors to slip in undetected that can result in designs that do not work or cause damage.

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1 Introduction

This guide has three main parts. The first part is the preparation work before debugging. Sometimes the preparation work can take an hour or more, but good preparation decreases overall debugging time. The second part of the guide covers the first part of the debug process: narrowing down what is causing the issue. PoE plus DC/DC designs can be broken up into sections, and this application report guides you through how to check if one or more of these sections are suspect in the problem. The third part of this guide covers common issues and common resolutions. For example, if the design has the parallel MOSFET in an active clamp forward that breaks during shutdown, what are the issues that usually cause that? This list is not exhaustive because there are many components in PoE designs and they can break in different ways and for different reasons. However, this guide should aid in the first steps of the debug process for most PoE designs.

Note

This document only covers flybacks and active clamp forward topologies. These are the main two topologies used in PoE applications because they provide good comprises of size, cost, and performance for a nominal PoE input voltage range (37 V–57 V) to a typical output voltage range (3.3 V–24 V) while providing isolation.

2 Preparation and Measurement Techniques

Part of the current TI strategy is to provide working reference designs that can be copied. The first recommendation is to find the closest reference design possible to the design being worked on. Look for the same IC, the same topology (for example, synchronous flyback), and the same output voltage and power level. If there is not a close design, contact the PoE applications engineer through E2E for an internal search. Next, evaluate any parts that are different, whether it be a transformer, a MOSFET, a resistor size, and so forth. Question why the part is different. List all the reasons how these parts are different (for example, different gate capacitance, different reverse recovery time, different voltage rating, different package size). These may be the first clues to why the design is experiencing problems, but the TI reference design is not. Review the *PoE PD Schematic Review Guidelines* application report for component variations.

2.1 Important PoE Signals

This section explains some of the important signals in a TI PoE PD design. First are VDD and VSS. These signals are the input power of the system, after it has been rectified off the input twisted pairs. Next is RTN (Return), which is the *ground* of the IC. RTN is also referred to as the *primary* ground because it is the ground on the primary side of the transformer. RTN is connected to VSS by an internal pass MOSFET after a successful PoE handshake is done. So VSS and RTN are not the same thing, VSS is not primary ground, and RTN is not negative input power. VC (also known as VCC and VC_in) is the input power to the IC. It is commonly believed that VDD is IC power, but VDD is input power for the whole design. In respect to the power path, VDD is the positive input power from the power sourcing equipment (PSE), and that power is what is sent through the transformer to the load. VC is taken from VDD and powers the IC.

Another important signal is VB (Bias Voltage). This is the 5-V regulator output. If the IC has an integrated DC/DC controller, it has a VB pin. Again following the power, VDD is input power, of which a portion is transformed down to VC through the auxiliary winding to power the IC, and that voltage gets bucked down to VB to produce a 5-V rail to power other functions within the IC. There is an important distinction to note here. TI has two device types for PDs: standalone PDs and PDs with integrated PWM controllers. An example of the first is the TPS2373-4 device. An example of the second is the TPS23730 device. Note that the PD does the *PoE* portion of operation – the detection, classification, MPS signal (if the device has Auto-MPS), and so on. Many of these functions are not dependent on VC or VB because their function comes before power is negotiated (like detection). Then there is the PWM controller (also known as the DC/DC controller), which is powered by VC and has functions like the GATE, the dead time, the switching frequency, and so forth. These functions are normally referenced to RTN for that reason.

So, problems within these designs can occur on either side: PoE or DC/DC. As previously stated, generally it is the DC/DC, but not always. Another important signal is the secondary side ground. This is also the output ground. V_{OUT} is the output voltage of the DC/DC converter.

2.2 Lab Equipment

The following list is not exhaustive, but these items are all useful. Not all equipment is required for every debug:

- DC power supplies
- Electronic load
- Oscilloscope with four channels and probes
- Current probe
- Differential probe
- Resistive load
- Digital multimeters (as many as your bench holds)
- Ethernet cable – standard Cat 5
- Ethernet cable – split open, banana female connectors soldered to twisted pair sets such that a DC power supply can power through these twisted pairs
- Grabber to banana wires
- IEEE802.3 certified Power Sourcing Equipment (PSE) – TPS23881 EVM recommended
- Bode box or equivalent for gain or phase measurement loop response
- Sifos® PDA-602 analyzer

2.3 Measurement Techniques

This section provides basic measurement techniques that make a big difference in debugging. First, it is valuable to use oscilloscope probe labels, if possible. Label each waveform in the picture, so that when it is captured it is clear what is being measured. If there are particular test points used by the oscilloscope probe, put that in parentheses. Second, use the graph marks for offsets. As Figure 2-1 shows, C1 (yellow) is 5 V/div and is offset by +5 V, C2 is 50 V/div and is offset by –150 V. Because of these results, it is apparent that C2 never goes above 100 V. If C2 was offset by –67.5 V, it would be difficult to determine the peak-to-peak voltage at a glance. It is obvious that C2 is the drain-to-source voltage of Q10 because of the oscilloscope probe label.

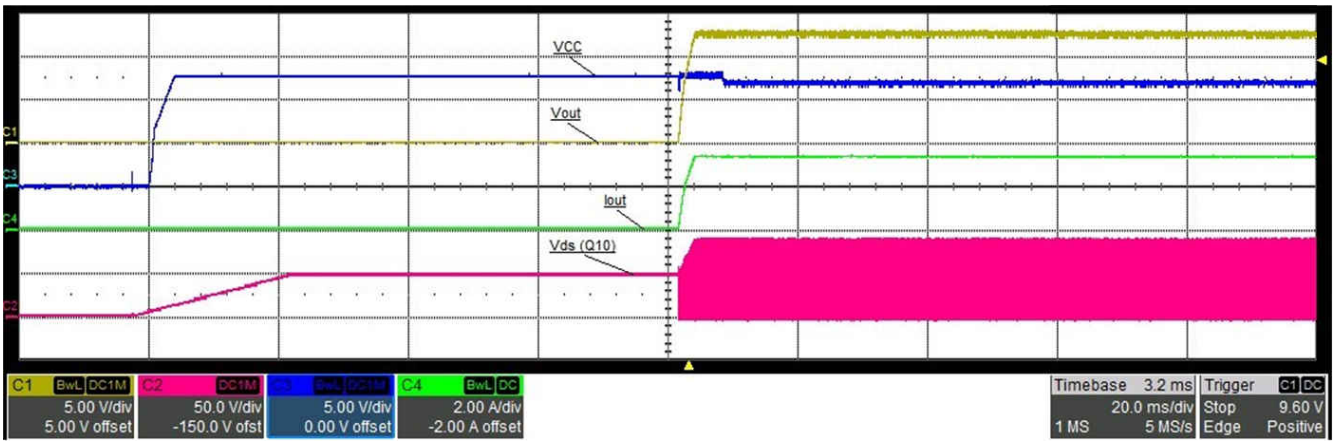

Figure 2-1. PoE Start-up

Another important tip is to use oscilloscope internal measurement functions when applicable. For example, most oscilloscopes can measure the Vpkpk of a particular channel. Oscilloscopes can make both vertical (y-axis) and horizontal (x-axis, which is usually time related) measurements. When setting the volts/div, try to use the largest V/div that will show the full waveform. If there are multiple signals in the same measurement, a smaller V/div can be used but use caution not to make it too small. For the time/div, there are two situations:

1. Figure 2-1 shows a successful start-up sequence. First VCC rises (blue), and then Vout, Iout and Vds begin to switch. This picture shows a successful start-up and a few time stamps of successful normal operation. Ensure scope shots show the entire sequence, but the individual parts can still be seen.
2. Figure 2-2 shows a switching waveform. The best practice is to show at least one full switching period. Optimal pictures show at least one but not more than three switching periods. The less switching periods shown the more detail can be seen in a single period.

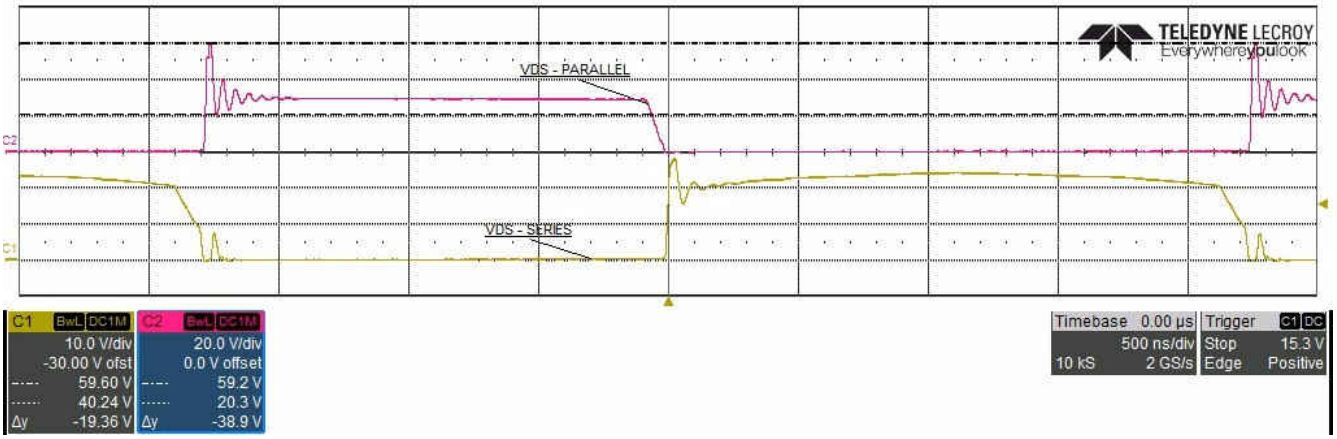

Figure 2-2. Switching Waveform

Oscilloscopes also offer filtering of the probes. Figure 2-2 shows that both C1 and C2 have a *BWL* icon. This indicates that bandwidth limiting is turned on. Many scopes offer filtering for 20 MHz, 200 MHz, and no filtering at all. These filers act as low-pass filters at these set frequencies. Noise from around the lab can be introduced into the scope, so sometimes it is useful to filter that noise inside the oscilloscope itself (if checking if a MOSFET is switching, checking a start-up or shutdown, and so forth). However, when checking a maximum voltage on a MOSFET, or investigating a voltage spike, remove bandwidth limiting. Noise or real, it is critical to find the maximum voltage, so remove bandwidth limiting. If you are unsure, capture both. It is a simple setting change.

Another important measurement technique is called *tip and barrel*. This is best shown in a picture, please see below for reference. For oscilloscopes, tip and barrel commonly have a ground clip that attaches to the probe with a short wire. This short wire can pick up noise and add parasitic inductance, which can alter the waveform. So, when measuring critical voltage signals, whether that be a maximum voltage on a FET, output ripple, switching voltages on a gate, the current sense voltage for the feedback loop, use the tip and barrel method. The tip and barrel method is to remove the ground clip, and replace it with a smaller ground connection wire. The ground connection wire will be a small attachment of wire that is curly on one side and then a small straight portion with one corner. The curly portion is what holds the attachment to the probe, and the wire with the corner is the new ground connection. Many scope probes come with a cover that has a hook, which can be used to hook onto test points or wires. If this is removed, it exposes the probe tip and a small exposed ring of metal. This is the ground connection and the curly side connects to the ground of the probe. This method creates the smallest ground loop between the probe signal and ground, and therefore reduces noise.

2.4 Board Preparation

When prepping a board for debugging, install a wire for RTN, primary ground, so that many oscilloscope probe ground clips can connect to it easily. Do this for both primary ground and secondary ground. Potentially all four probes of an oscilloscope could be connected to primary ground, so make the wire long enough for all four to connect. However, a wire is essentially an antenna, so do not make it excessively long. It should not exceed the length of 5 milimeters, as a general rule. Other signals to put wires on are VDD, VC, and Vout. A wire can connect to these signals because these voltages should be steady and are relatively high voltage (as in connecting a wire to them for the scope probe should not introduce a significant amount of noise to the measurement versus directly connecting the probe to the board). Trying to hold more than two oscilloscope probes and operate the power supplies and take good measurements can be difficult, so it is good to have wire connections with wires, when able. Taking these measures provide a sufficient start for debugging.

3 Narrowing Down the Problem Area

This section helps narrow down the potential problem area. Problem areas are identified by finding the area or component that is the most likely cause of the issue in the design.

First, define what those areas are and highlight them on a schematic.

3.1 Schematic Areas

The first area is the PoE Input, see Figure 3-1. This includes the RJ45, the Ethernet PHY (which separates the data and power), the Bob Smith terminations, the rectifier, the EMI filtering components, and the TVS diode. The rectifier can be discrete components or integrated solutions.

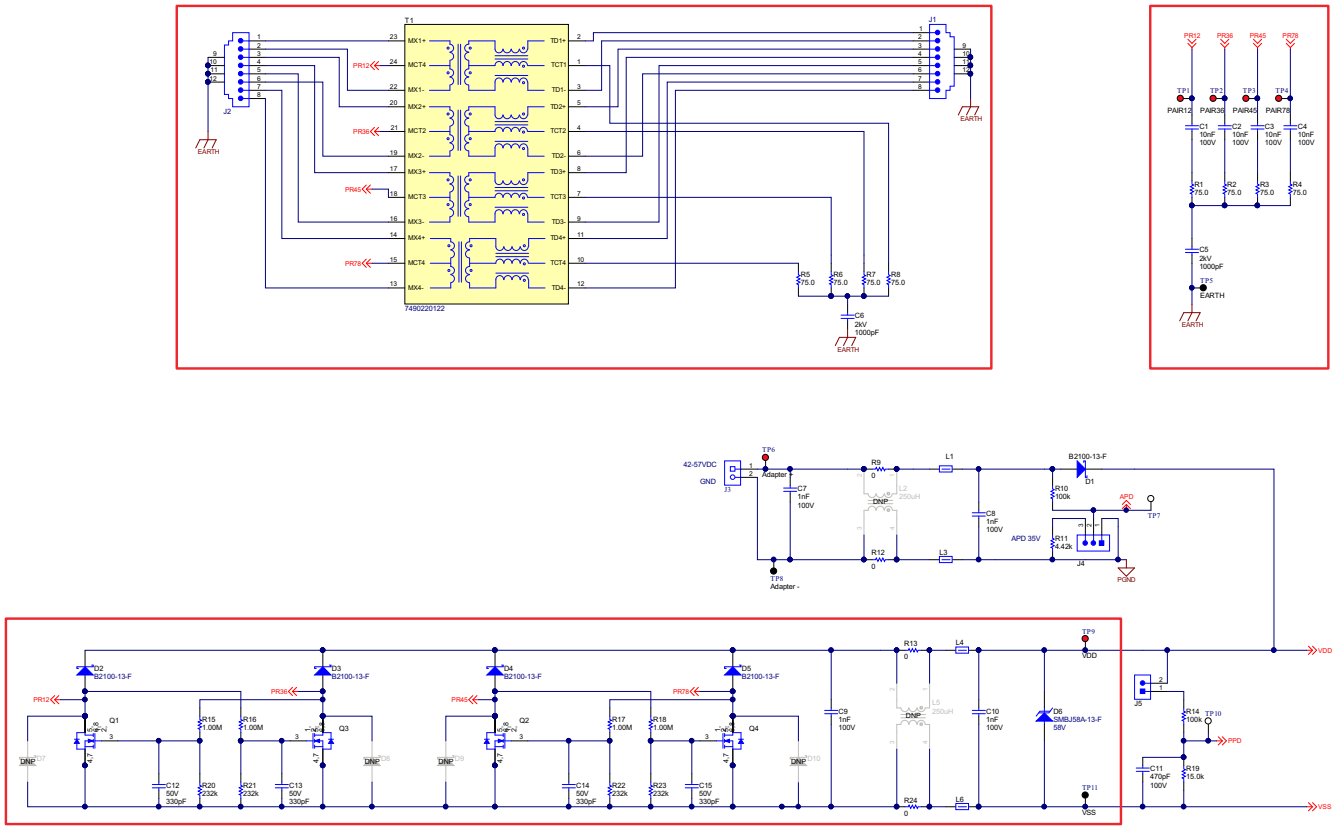

Figure 3-1. PoE Input Section

Figure 3-2 shows the second area, the PoE Settings. These are the components that set or enable different PoE functions. For example, the detection resistor, enabling Auto-MPS, the detection capacitance, and so on. Note that many of these components reference VSS instead of RTN.

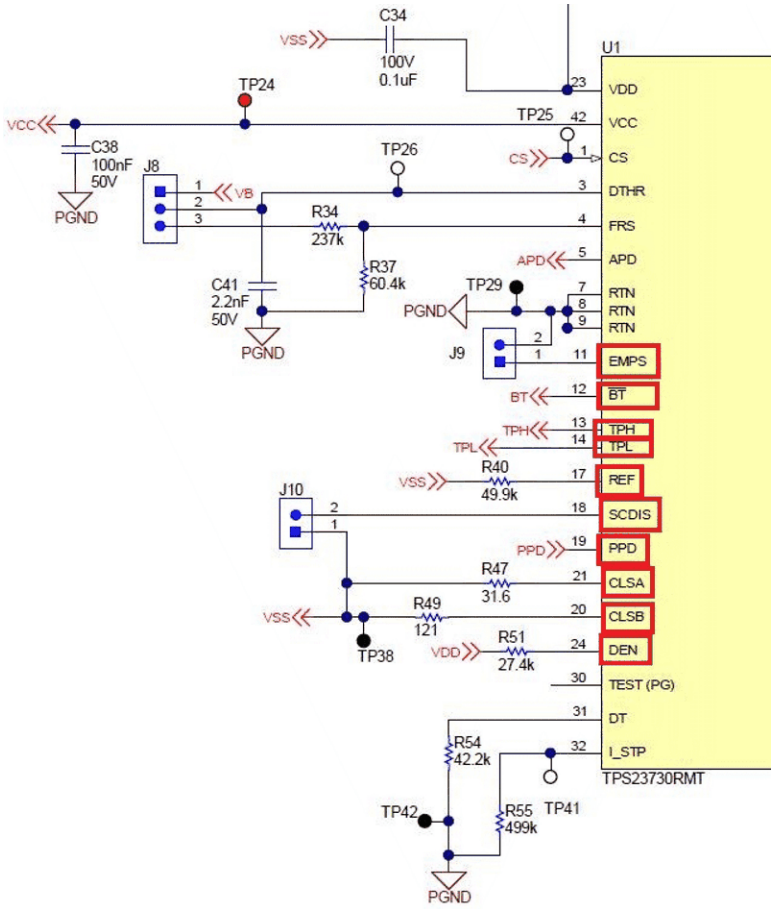

Figure 3-2. PoE IC Settings

In a standalone PD, like the TPS2373, these are the pins and components that are not being sent downstream to a PWM controller.

The next section is the primary side of the DC/DC. This section includes a few subsections: input filter, IC settings, VCC input, primary side feedback components, the primary MOSFETs (and accompanying components), and the primary side of the transformer.

The input filter, illustrated in Figure 3-3, includes the input bulk capacitor, an inductor, and some smaller capacitors. The bulk capacitor must have some ESR to operate, so they are typically electrolytic or aluminum capacitors. These are a good reference point on the board since they are typically easier to see with the naked eye, and they give access to VDD and RTN with large solder pads. The other components of the input filter help reduce input ripple (and thus output ripple).

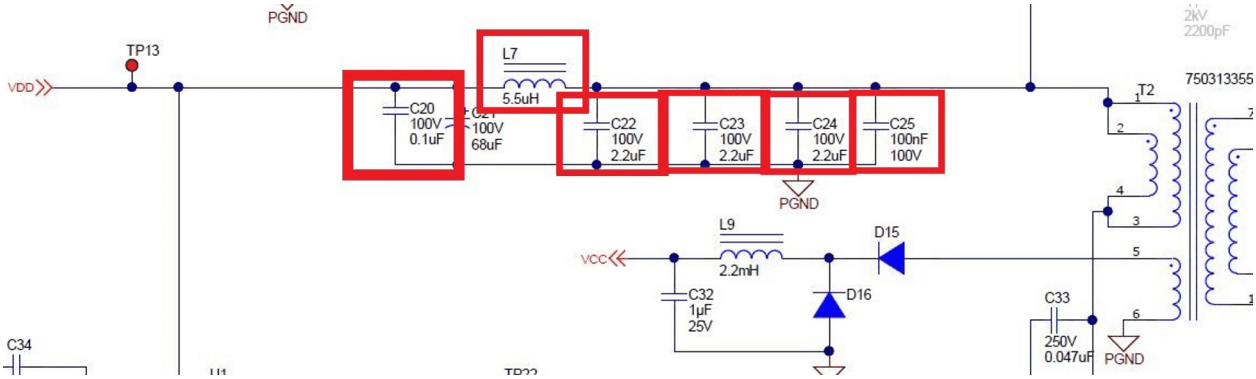

Figure 3-3. Input Filter

The PWM IC settings are the rest of the resistors and capacitors on the IC. They set characteristics of the PWM controller. For example, the FRS resistor sets the switching frequency, DT sets the dead time between the two gates (if applicable), and so on. Not shown here is the LINUV input. The LINUV input sets the turn-on and turn-off DC/DC input voltage of the IC.

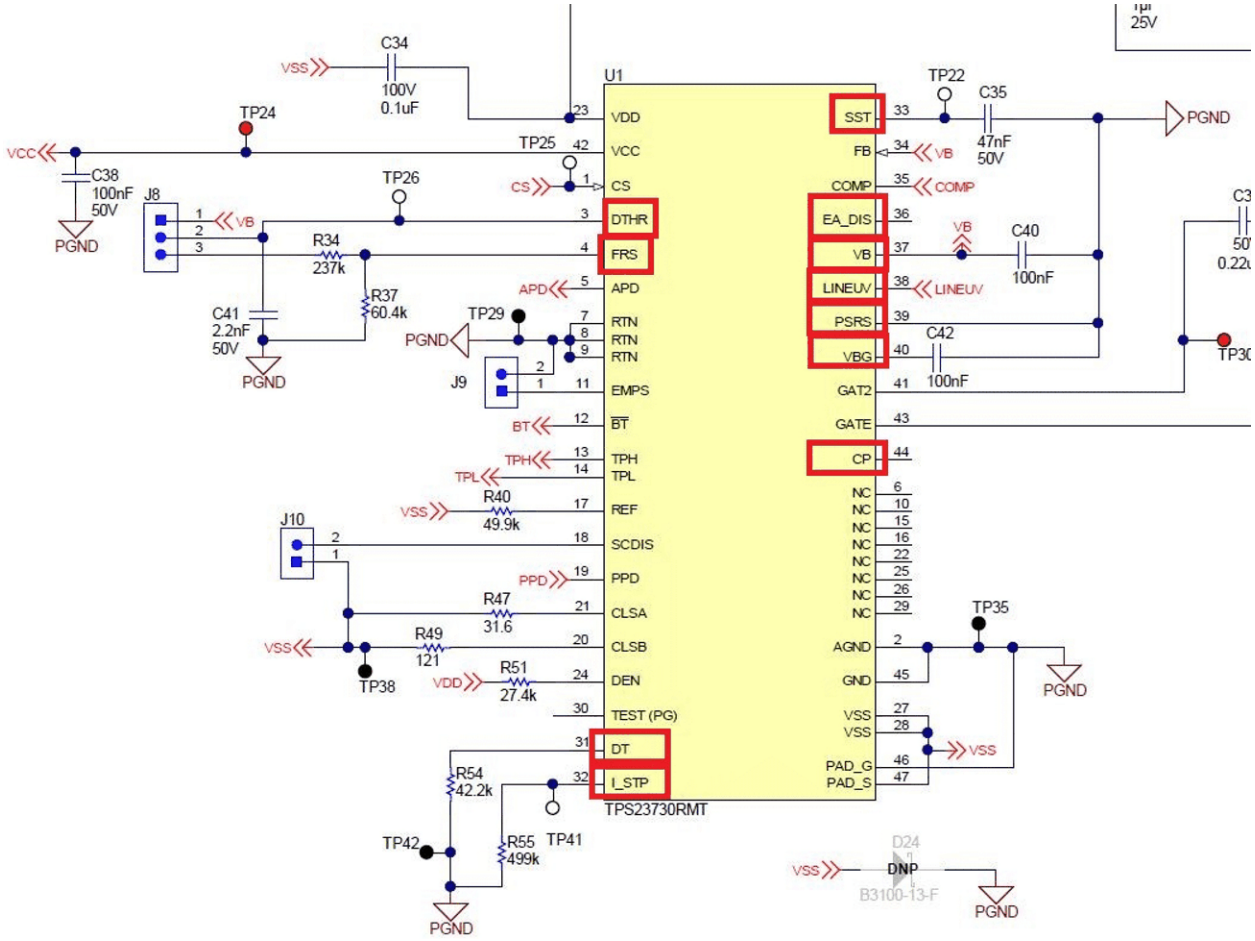

Figure 3-4. DC/DC Pin Settings

The VCC input looks different for different topologies. As previously discussed, VCC is the input power for the IC. In an active clamp forward, the VCC line is taken off the auxiliary winding of the transformer, rectified by two diodes and the ripple is filtered with an inductor. VCC requires a capacitor to store energy for the IC. VCC also requires a smaller bypass capacitor, as does VB and VDD.

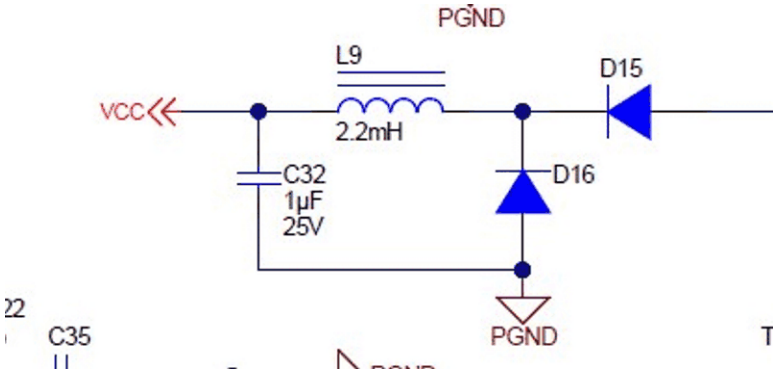

Figure 3-5. VCC Input Circuit for Active Clamp Forward

The VCC input in a flyback appears similar because it is taken off the auxiliary winding of the transformer. Note that flybacks typically only need a single diode to limit the VCC input current from the auxiliary winding and the resistor to help filter. The VCC capacitor is also required. For primary-side regulation flybacks, additional components appear on the winding that is discussed later.

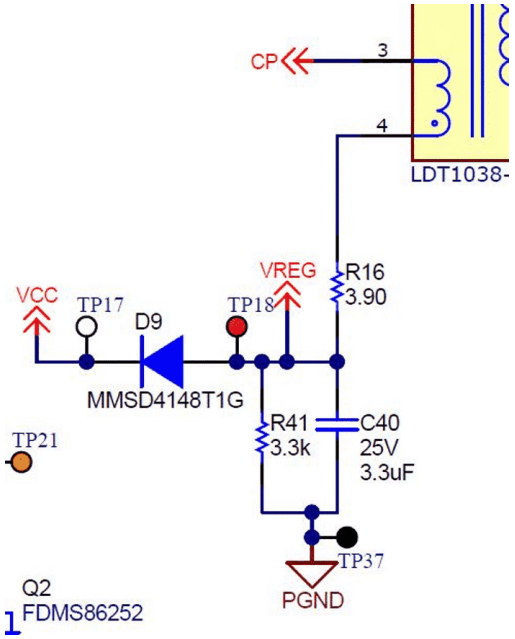

Figure 3-6. VCC Input Circuit for Primary-Side Regulation Flyback

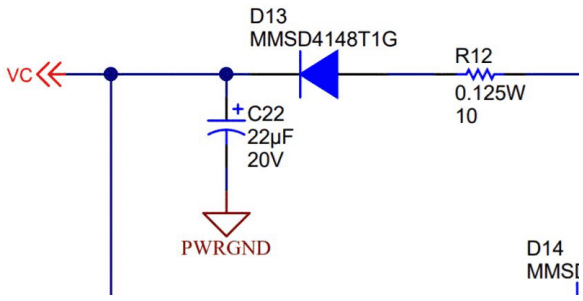

Figure 3-7. VCC Input Circuit for Optocoupler Flyback

Both PSR and optocoupler feedback designs have components that contribute to the feedback loop on the primary side. PSR designs have the entire feedback network on the primary side.

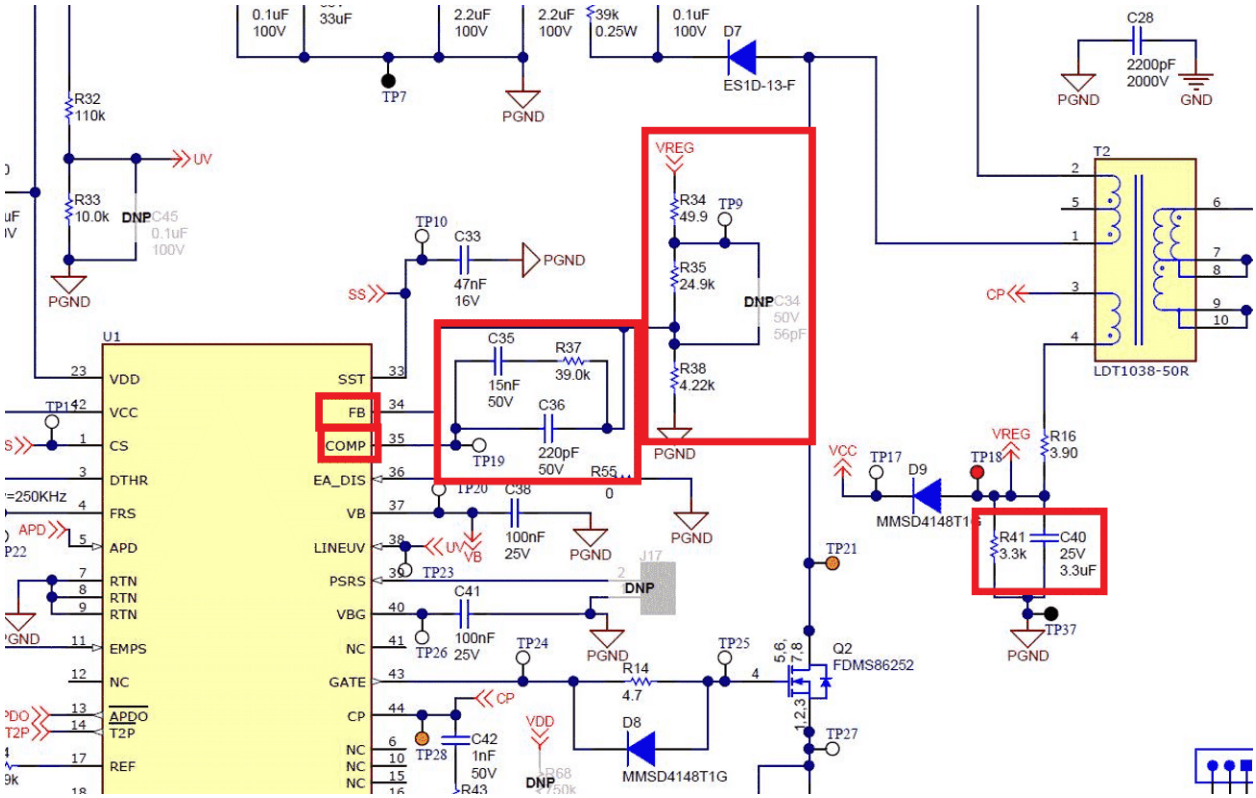

Figure 3-8. Primary Side Feedback PSR Flyback

Optocoupler feedback components have their primary side loop components at the optocoupler. Note this is true for both ACF and flyback designs.

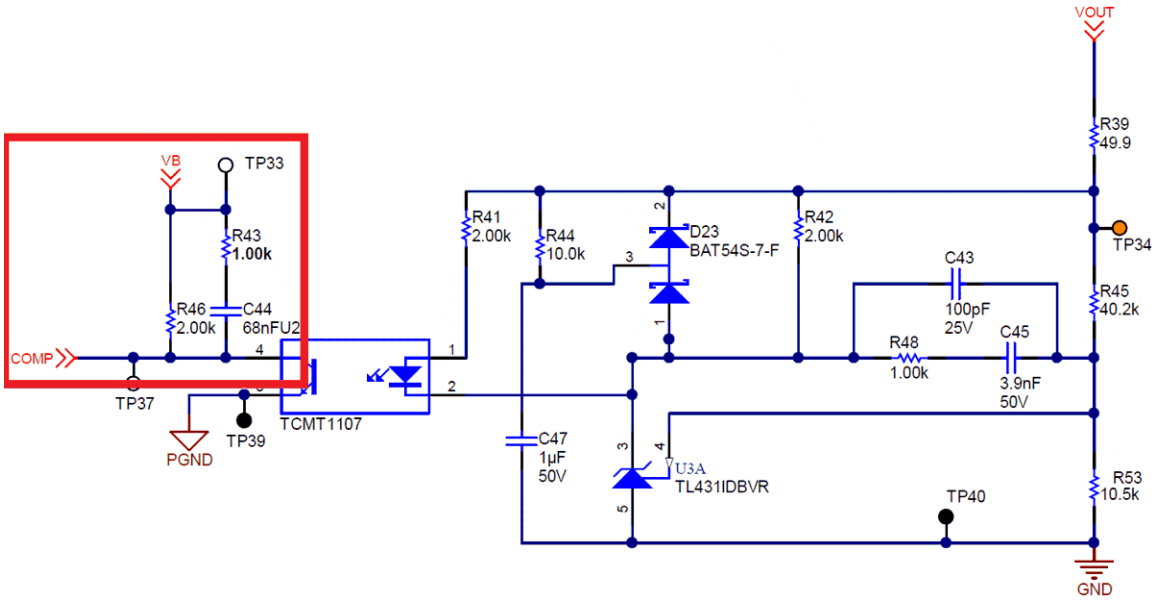

Figure 3-9. Primary Side Feedback Optocoupler Flyback

The next portion of the primary side of the DC/DC is the primary side MOSFETs and accompanying components. For a flyback, there is only one primary MOSFET. This MOSFET requires a gate drive. Sometimes a more robust gate drive, which includes a BJT, is required to turn the MOSFET off faster. All MOSFETs require a DRC clamp.

This limits the overshoot voltage so that the MOSFET is not damaged. There is always overshoot because of the primary inductor of the transformer. The current sense or CS resistor, helps set the output current limit.

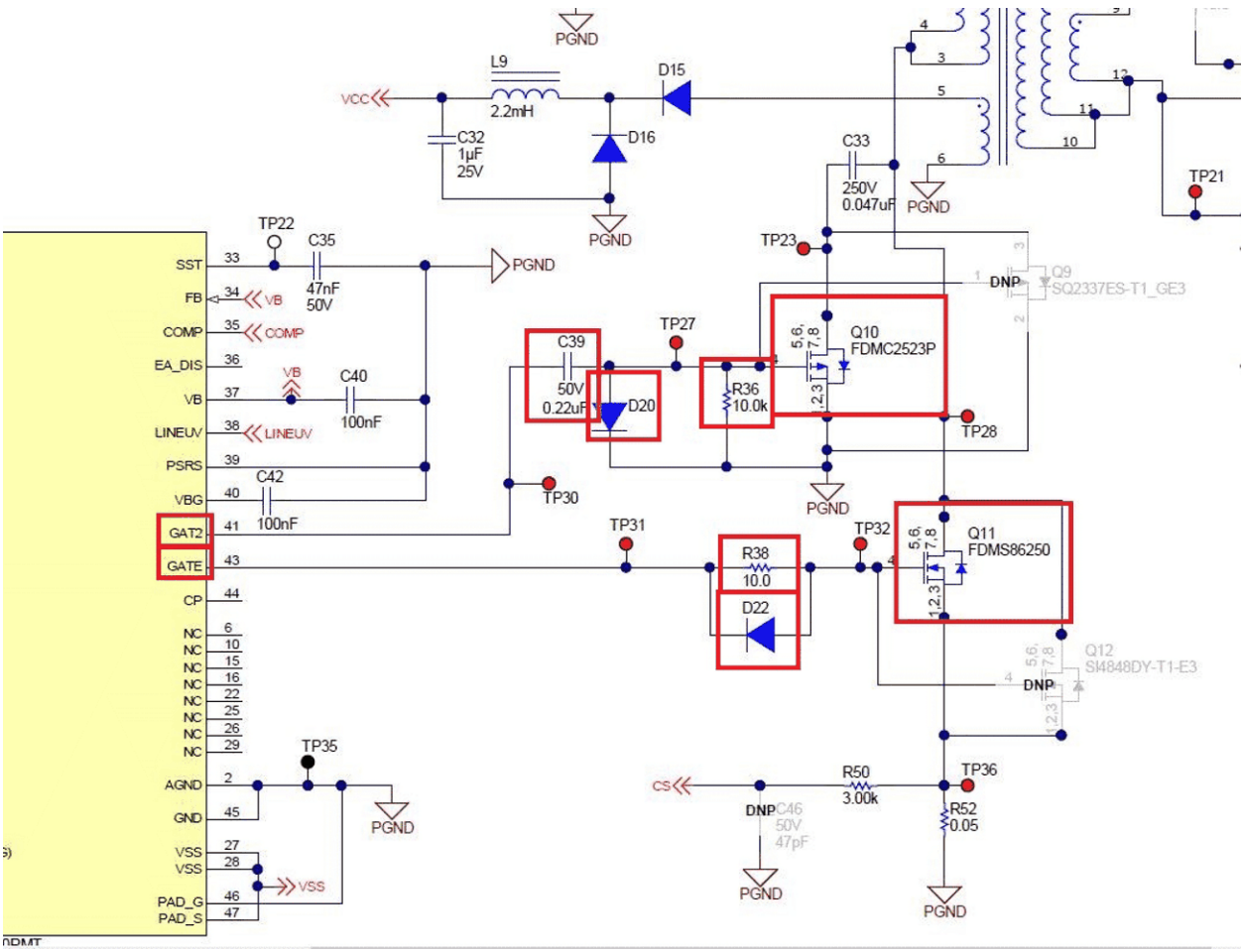

Figure 3-10. Primary Side MOSFETs and Accompanying Components (Flyback)

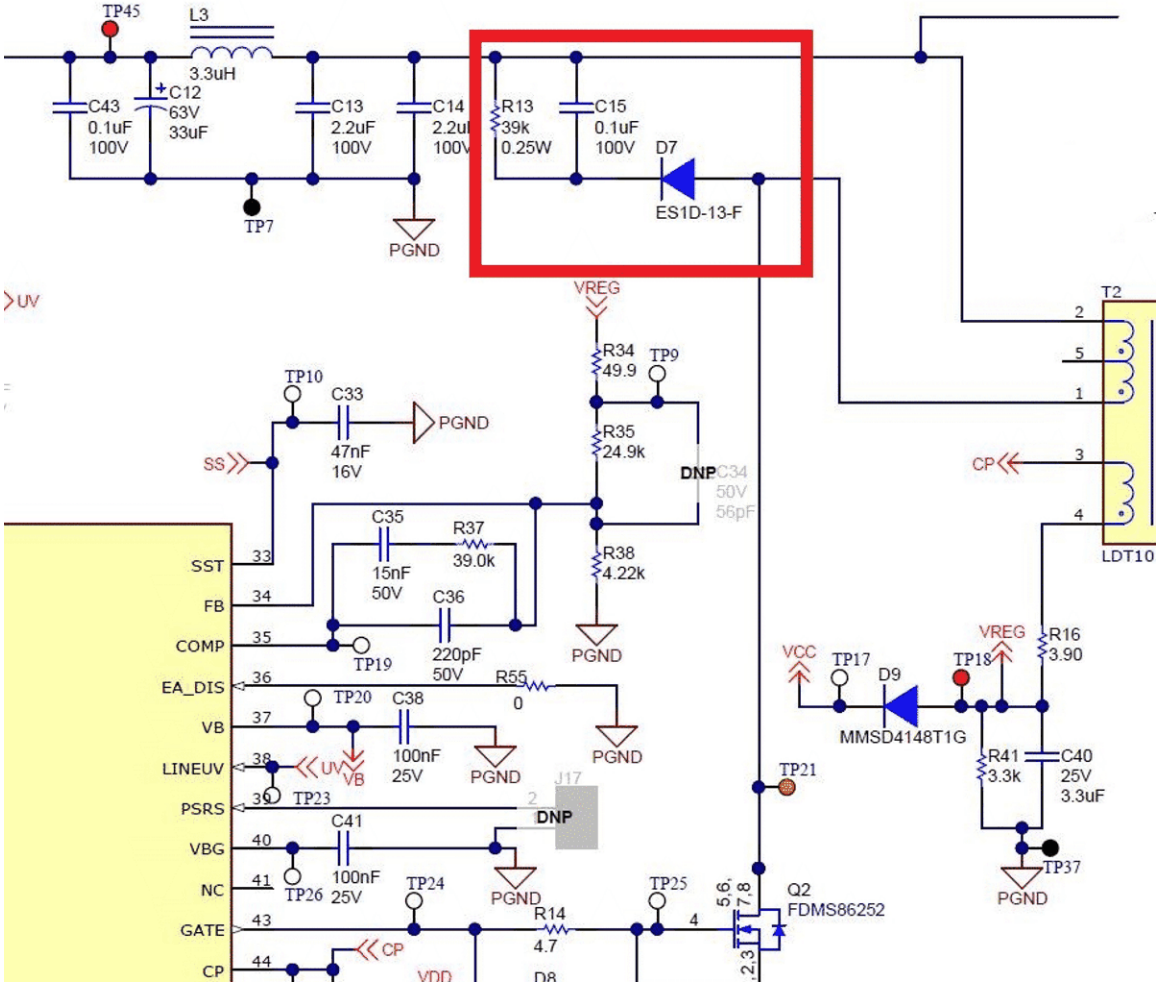

Figure 3-11. Primary Side MOSFET RCD Snubber

An ACF has two MOSFETs on the primary side. The P-FET provides the active clamp. Both MOSFETs need their respective gate drives. Additionally, the high voltage clamp capacitor is required, but note there is no DRC clamp

Note that MOSFETs in any topology can also have an RC snubber. RC snubbers are placed across the drain to source, and can help reduce the overshoot across the FET. These are not pictured here, but sometimes are useful for overshoot or EMI issues.

Lastly, the primary side has the primary side of the transformer, which includes the primary inductor and the auxiliary winding.

The next section examines the secondary side. This is where the topologies differentiate from one another the most. Diode flybacks are considered the easiest because they have the fewest parts.

Diode flybacks consist of the output diode and accompanying snubber (typically RC).

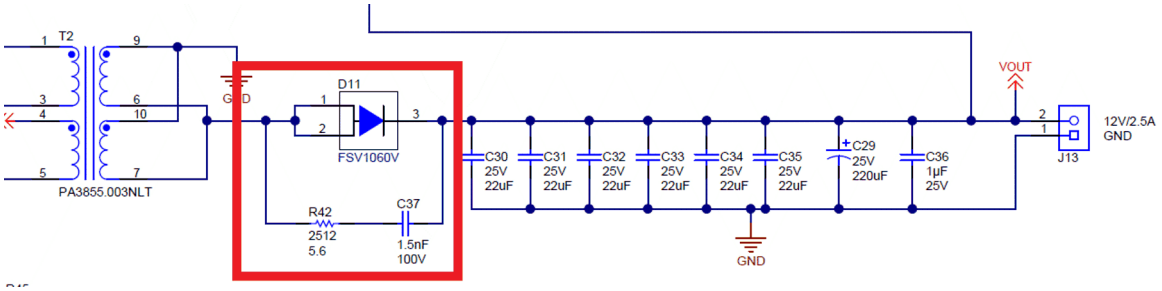

Figure 3-12. Secondary Side Diode Rectified Flyback

A synchronous flyback is similar, except that it has a MOSFET instead of a diode. That MOSFET requires a gate drive. The gate drive can be self-driven, as in the transformer drives it, or it can be driven with a pulse transformer or a synchronous rectifier IC. Figure 3-13 through Figure 3-15 provide samples of gate drives and MOSFETs:

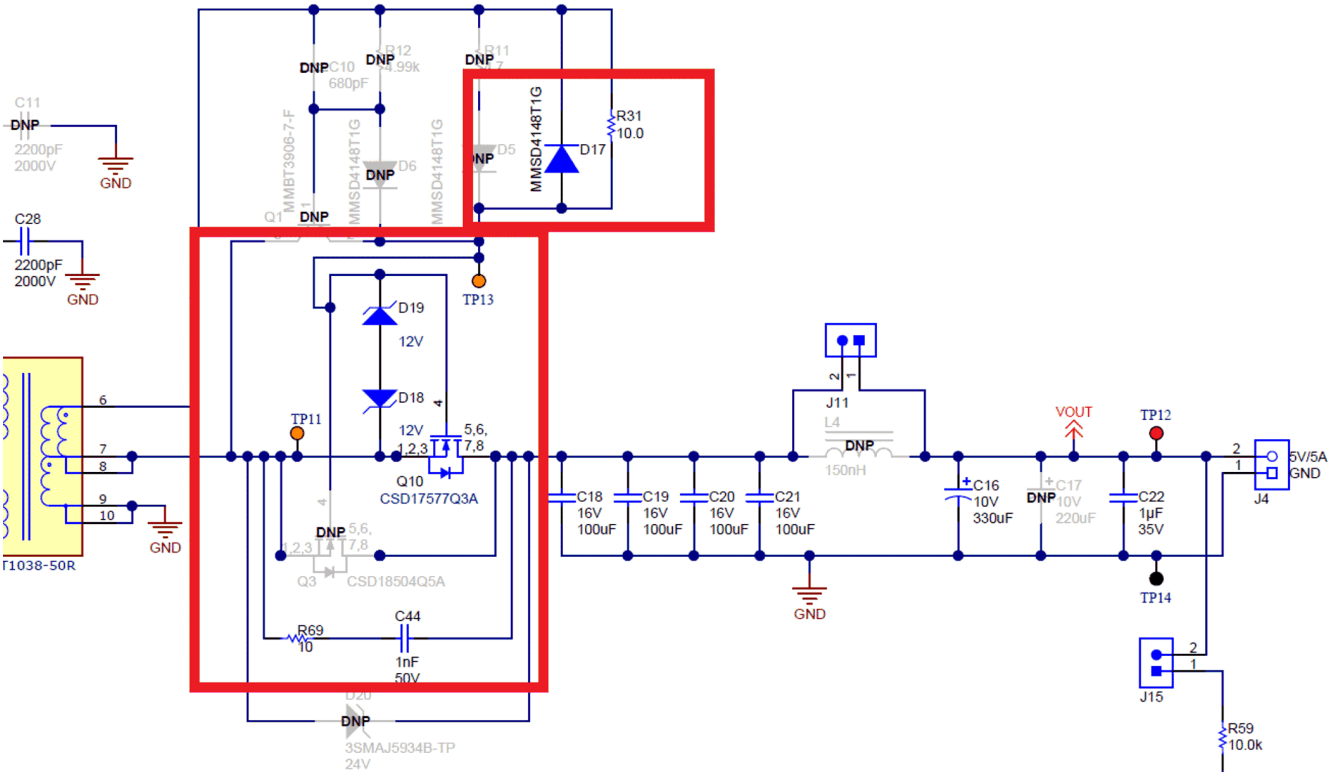

Figure 3-13. Secondary Side Self Driven Synchronous Flyback A

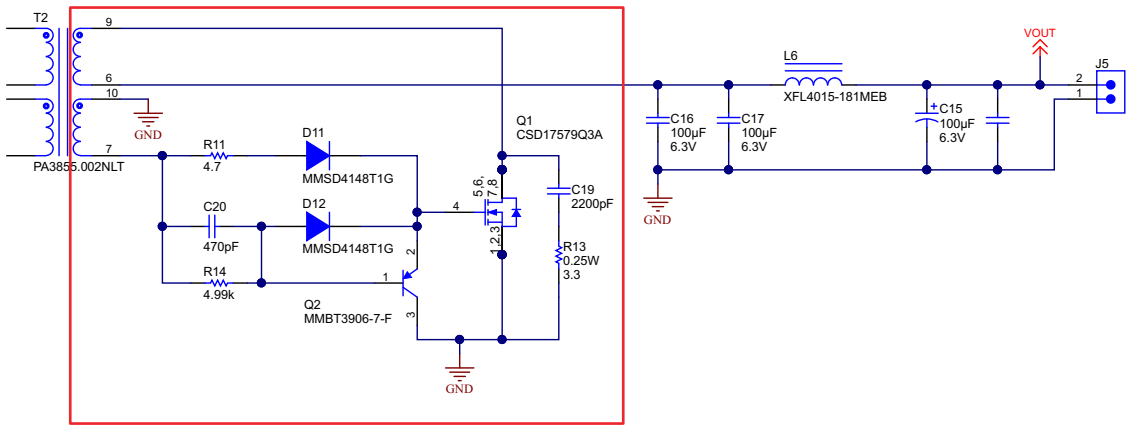

Figure 3-14. Secondary Side Self Driven Synchronous Flyback B

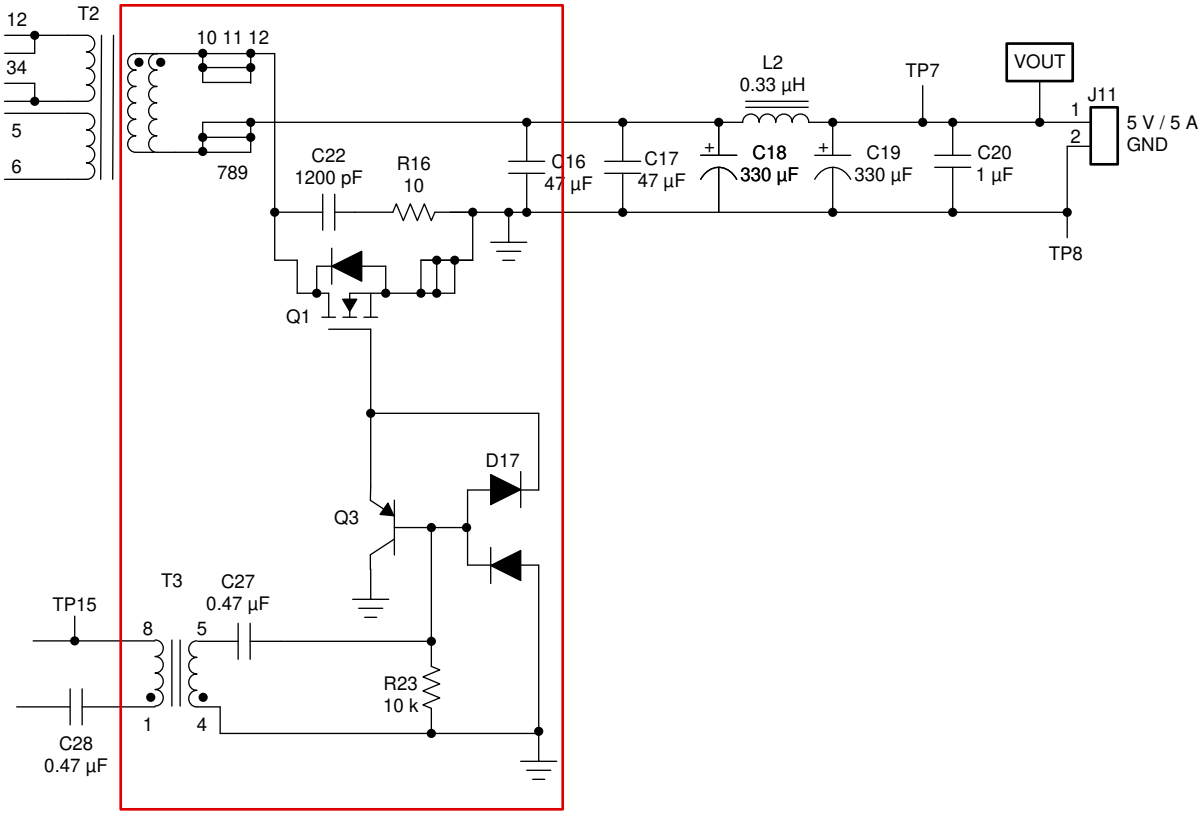

Figure 3-15. Secondary Side Driven Synchronous Flyback

Active clamp forwards are the most complex topology since they have the most parts and most considerations. Active clamp forwards consist of two MOSFETs, their accompanying gate drives, snubbers (both RC and RCD), and an inductor. Using Figure 3-16, the switching MOSFETs and gate drives are in the dotted-line boxes, and the accompanying RC snubber and RCD clamp are in the solid-line boxes. The green line is considered the parallel MOSFET because the VDS is in parallel with Vout. The red box is considered the series MOSFET because the VDS is in series with the power path. Note, the inductor is optional in flybacks but is required in ACFs.

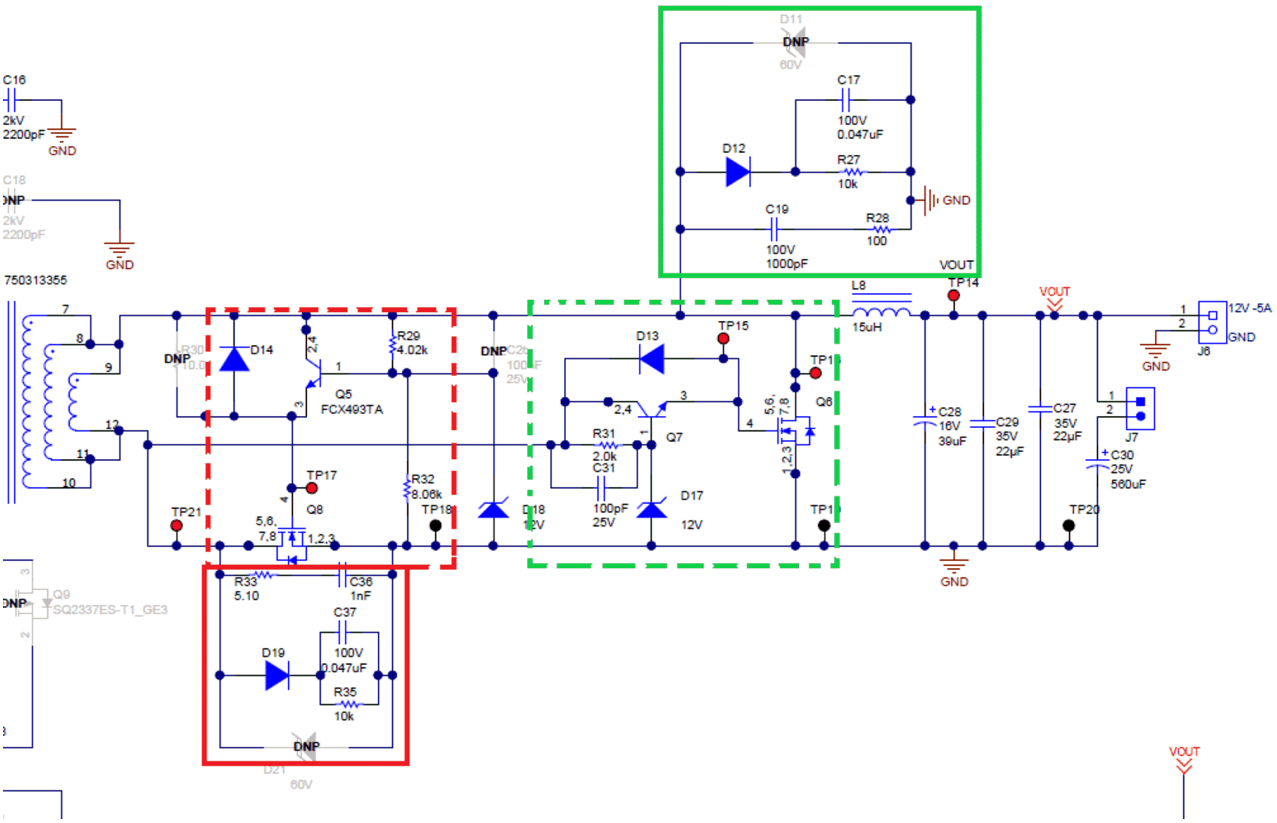

Figure 3-16. Secondary Side Active Clamp Forward

All topologies will have output capacitance. This is usually a mix of electrolytic, aluminum, tantalum polymer and ceramics. Additionally, there may be an inductor to create a PI filter.

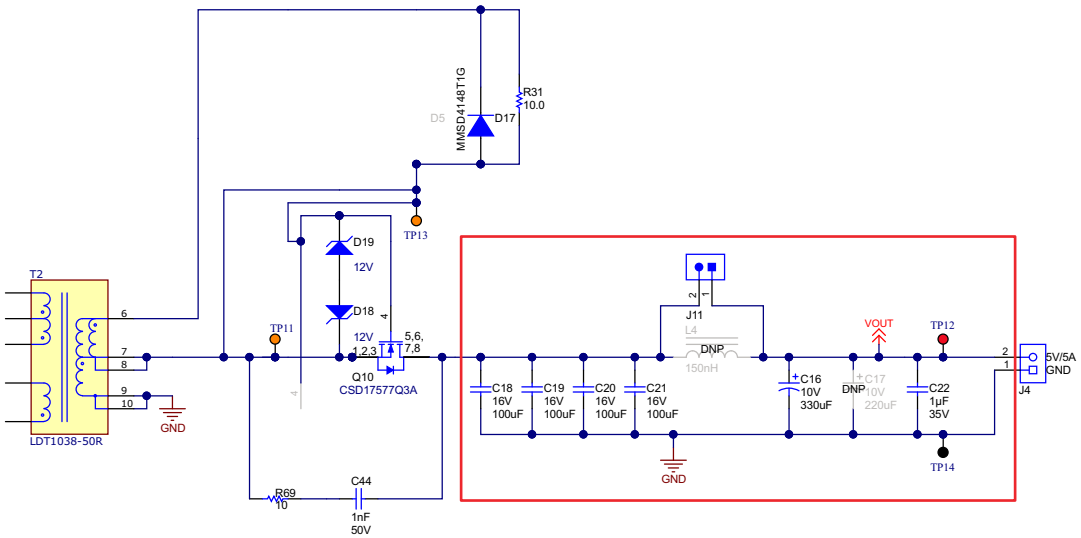

Figure 3-17. Output Capacitance

Finally, the last section is the feedback section, particularly with an optocoupler feedback network, see Figure 3-18. Taken off the output voltage, a TVL, group of resistors and capacitors, and a diode feed into the diode of the optocoupler. These form the poles and zeroes in the loop response, as well as a secondary soft start circuit.

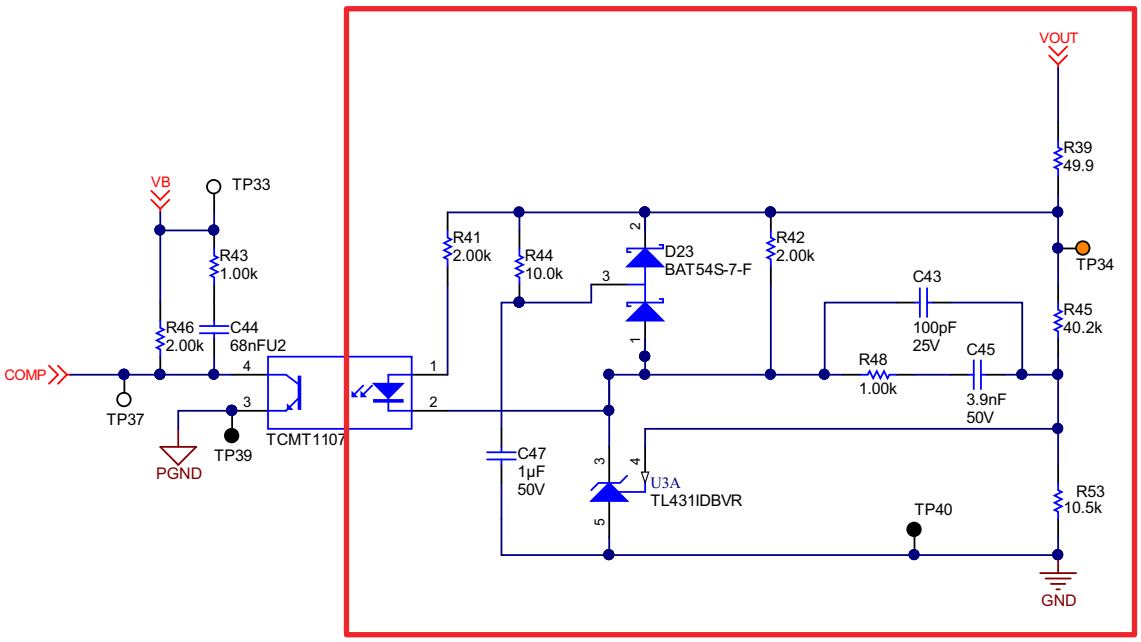

Figure 3-18. Secondary Side Optocoupler Feedback Network

3.2 Narrowing Down the Area On Board

This section discusses how to narrow down in which area the problem might exist.

PoE start-up is tested first. This can have two oscilloscope shots to get everything needed. The waveforms needed are:

- VDD_RTN
- VSS_RTN *
- VC
- GATE (or Vds)
- Vout
- Iout (sometimes)

Note

* Do not connect ground probes to both VSS and RTN at the same time.

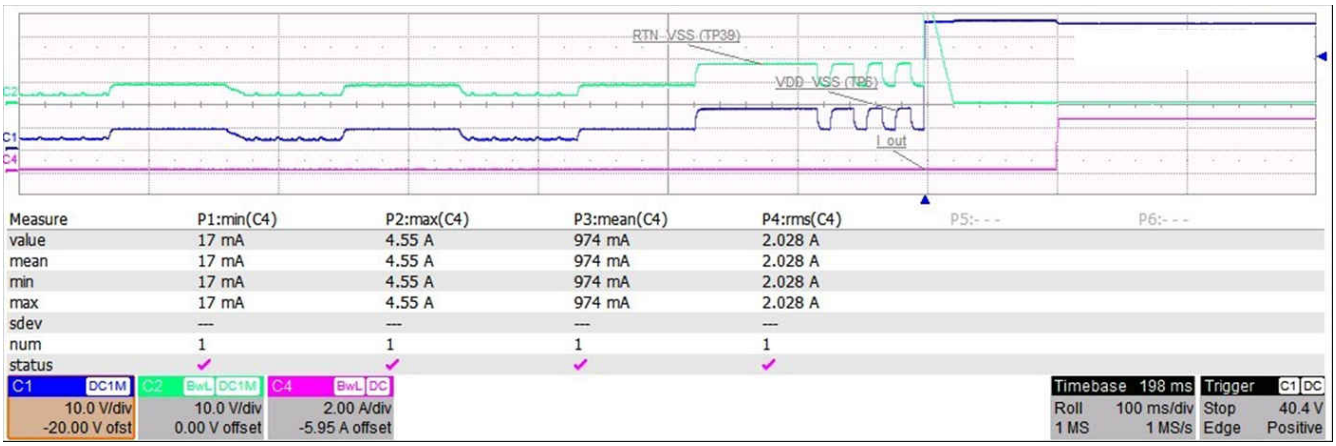

Figure 3-19. PoE Handshake

The waveforms in Figure 3-19 and Figure 3-20 show a successful PoE handshake (or not), and a successful DC/DC start-up. It is important to establish if the PD is negotiating power with a PSE. First, the waveforms confirm if detection is functioning as it should and that the PSE reads a proper detection. Next, the waveforms illustrate that VSS and RTN goes to 0 V, which means the internal pass MOSFET is working. This MOSFET can be damaged from ESD and surge events so it is important to confirm that the MOSFET is turning on after a detection and class signal.

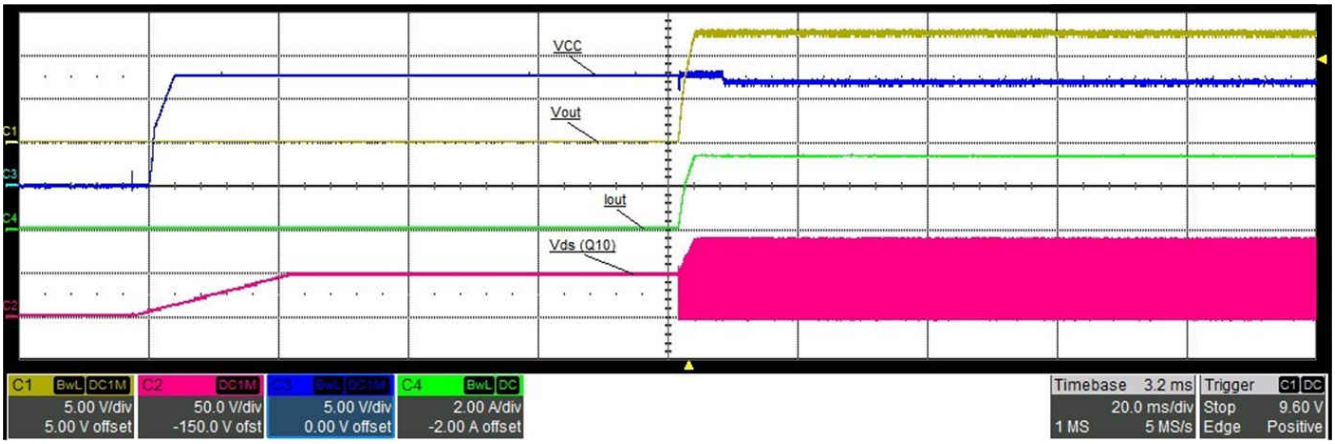

Figure 3-20. PoE DC/DC Start-up

The VCC waveform confirms that the IC is receiving power. Remember that VCC is input power for the IC. If the VCC line is a triangle wave, then usually there is not enough effective capacitance on the VCC input. The next important piece of information to note is the GATE waveform. If VCC is above the threshold, but there is no switching, then the IC is broken internally. However, if there is switching, then it is confirmed that the IC is receiving power, that power is being internally regulated and is powering the gate to be switching. Thus far it is confirmed that the PD can successfully negotiate power, which means the PoE IC settings are probably correct. It is also confirmed that the IC is receiving power and the internal functions are being powered.

If the DC/DC converter is not starting up, then check the PoE settings, the DC/DC settings, the input bulk capacitor, the transformer, and the VC input.

The next thing to check is the switching components. First and foremost, check all MOSFETs in the system. Check the drain-to-ground and gate-to-ground of each MOSFET. Ensure they are all switching properly and the VDS and VGS is not exceeding the limits. Vary the input voltage and load to test the MOSFETs for maximum voltage and current. For example, do 57 Vin at no load and full load. Next, try 37 Vin at no load and full load.

Now, check the Vout signal. Vary the load of the system across the full range, and note any changes in the output behavior. The potential causes here can be an error in the feedback, too little output capacitance, or an error in the switching timing. Check for oscillations on the output as well.

After Vout, check the CS pin. This should be measured across the sense resistor – usually it is less than 1Ω, and placed directly next to the primary MOSFET. The waveform should look like a triangle wave. Ensure that the CS pin does not exceed the CS threshold before full load is applied to the output. Check the transformer primary inductance, the CS resistor size, and the primary FET. See Figure 3-21 for a reference of the CS waveform.

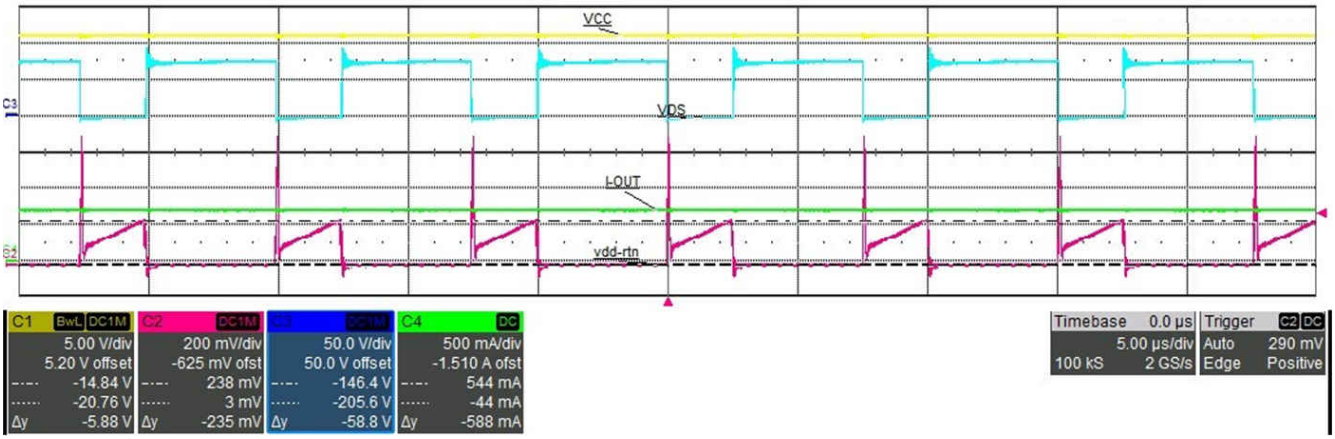

Figure 3-21. Current Sense Switching Waveform

Check the adapter input power (if applicable). Ensure that it properly powers the output and interacts with the PoE power as expected. Meaning, insure the adapter has the proper priority with PoE. For example, if the adapter is prioritized, then the PSE should remove power from the PD.

Finally, check the overall efficiency of the design. This is a good measure to tell the overall health of the design. If a component is too small, something is broken, something is too hot, something is too slow, and a number of other conditions can cause a drop in efficiency.

4 Common Issues

This section lists some common issues that happen often, and includes a quick discussion about the potential causes. Sometimes unique issues present themselves as a common problem, so the causes discussed here are not necessarily an exhaustive list.

- When power is applied, the VCC waveform looks like a triangle wave. If the gate is probed, it is switching momentarily, but then shuts off.
  - The usual cause for this is that there is not enough effective capacitance on the board on VCC. ACF designs that use the TPS2375x family might require more capacitance. Small capacitors, such as 0603 size, have a smaller effective capacitance than a 0805 or 1206. Additionally, the voltage rating is important to check. If there is anything connected to VCC (or VB), then the amount of capacitance might need to be increased. Therefore, it is recommended to increase the capacitance on the VCC line.
  - Check that there is a small bypass capacitor on VCC.
  - The VCC cap has to power the design until the output is ramped up, so if the output takes too long to settle then the VCC cap can be drained. If there is too much output capacitance it can take too long to charge. Additionally, the secondary soft-start circuit could be taking too long. The solutions here is to reduce the output capacitance or reduce the capacitor in the secondary soft-start circuit.
- If the gate is not switching at the expected duty cycle when VCC is past its threshold, then the IC could be damaged or it could be something in the feedback. If the optocoupler is damaged, it could be pulling the feedback low. The feed-forward resistor could be putting too much bias on CS – the solution is to increase the resistance. The CS resistor or slope compensation could be incorrect. Sometimes adding a 47-pF capacitor in series with the slope compensation resistor can help filter this signal and make the difference.
- If a successful PoE negotiation is observed, but VSS and RTN do not go to 0 V, then the internal pass MOSFET could be damaged. This is often caused by ESD and surge events. Both of these events are system-level considerations, so there are a number of components and system parameters to be considered. TI recommends adding a TVS between VSS and RTN. This helps protect the IC during surge and ESD events. Additionally, reducing the common-mode capacitance helps with surge events. Besides MOSFET damage, the rise time of VDD_VSS needs to be checked. Ensure the PSE ramp-up time is compliant with the IEEE802.3 standard.
- If the output voltage changes with load, there are a few things that could be causing it:
  - The CS threshold is met before it should be
  - The feedback system either does not have enough gain margin, phase margin, or something is installed improperly (broken or incorrect part)

  - The shunt voltage regulator has the incorrect reference voltage. Check the part number for this.
  - The optocoupler could have the wrong CTR: look for 80%–160% or 100%–200%, or the optocoupler biasing current could be incorrect.
  - The timing of the circuit (especially ACFs) is off
- If a MOSFET is breaking, then it could be for the following reasons:
  - The switching voltage is too high. Example, the overshoot on Vds is 60 V and the MOSFET is rated for 40 V. This could be because there is no snubber, the snubber is the incorrect value, or the physical placement is too far away. The overshoot voltage can happen exclusively during start-up, shutdown, or during normal operation. Check all of these conditions.
  - Too high of peak currents. Check the transformer inductance and turns ratios as compared to a validated design (EVM or reference design). Also check the polarity (dots) of the transformer and ensure the polarity is correct.
  - Shoot-through, which is defined as when both the primary and secondary MOSFETs are ON at the same time. This is not possible in a diode flyback, but can happen in synchronous flybacks or ACFs. Shoot-through can cause a higher Vds, and more importantly it heats up the FET. Many times the issue is that the GATE of the synchronous (secondary) MOSFET is not turning off fast enough. The MOSFET could also need a faster diode across Vds. Sometimes no diode is present, which means the circuit is running off the body diode of the MOSFET. This body diode may not be fast enough for the switching frequency, so adding a faster diode can correct this. Another common cause here is that the gate charge of the MOSFET is too high. Please compare the current design to a known working design, such as an EVM or TI reference design. Compare the MOSFET gate charge and ensure the gate charge is not excessively larger. To check for shoot-through, capture both GATEs and DRAINS of the MOSFETs on the same oscilloscope shot.

Note

Snubbers and diodes are not effective if they are placed too far away from what they are protecting. The distance creates a parasitic inductance that renders the diodes ineffective at their clamping voltage. This is also true of TVS diodes. Therefore, place the snubbers closer to the MOSFETs.

- If there is no successful PoE negotiation, the following are common causes:
  - The DEN is incorrect and must be adjusted properly for the input bridge type. A discrete diode bridge typically works with 24.9 kΩ. However, hybrid bridges, full MOSFET bridges or an integrated solution can have a lower resistance and therefore the resistor needs to increase. The resistor is typically in the 25 kΩ to 27 kΩ range.
  - The terminations of the input transformer, the Ethernet PHY, is incorrect.
  - The input capacitance between VDD_VSS is too high. The IEEE802.3 standard permits only 120 nF. Considering most ICs require a 0.1-µF bypass capacitor for VDD_VSS, the input filtering capacitors become limited.
  - If there is any added circuitry (like sensing) this can corrupt the detection current. Try removing this circuitry.
  - A component in the input rectification bridge is broken
  - Potentially the IC could be damaged and not producing the detection or class currents.
- If the PSE cuts off power after 500 ms or so, this is due to the MPS signal not being met. The IEEE802.3 standard has a minimal *Maintain Power Signature* (MPS) signal that needs to be sent to the PSE at about 10 mA. Many times, during the first power up of the board, there is no load attached to the output. Some designs do not draw this much current when there is no load attached. This is more common in diode flybacks since they can more easily slip into discontinuous conduction mode (DCM), which significantly drops the overall input current. Try adding some load to the output of the design to get the input current beyond the MPS signal minimum. This behavior is characterized by a successful PoE handshake and power-up, but after 500 ms or so the input power is cut off and the output drops as well. This behavior is usually the MPS signal.
- There are a few reasons for VCC damage. The first thing to check is VCC during shutdown. If there is an overvoltage, it can be caused by a number of factors. Read the *Soft-Stop: TPS2373X Feature Explanation* application note that discusses this situation at length. Common fixes include:
  - Increasing the amount of capacitance on VCC

  - Changing the amount of input bulk capacitance
  - Changing the amount of output bulk capacitance
  - Overvoltage on the MOSFETs in the design
  - The transformer can be the cause of this, so switching transformers to one used in an EVM or reference design
  - If the inductor on VCC is not big enough it can cause peak charging in ACF topologies, so increase the inductor
  - In a flyback, if the series resistor on VCC is not large enough, it can cause peak charging
  - If there is an error in the feedback, the output voltage can fly up which can cause VCC to also fly up and damage. Check the feedback components and compare them to a reference design
- The following are common causes for a break after a design works for a long time (hours, days, weeks):
  - Thermal issues are the *most* common cause for a break here. Electrical issues typically reveal themselves very quickly. Thermal issues can take a long time to show. Often the thermal issue is not *every* deployed device, but is a number of devices.
  - The next most common cause for breaking is a surge or ESD event. Again, electrical issues typically break the design early, but a design could operate without an ESD or surge event for a long time. Additionally, properly testing these parameters takes careful test procedures, so designs can slip through testing without showing signs of issues.
  - Finally, start-up or shutdown events are the next most likely cause for breaks. Sometimes there is overshoot during start-up, or the energy in the system is not properly dissipated during shutdown. A design can operate a long time without a start-up or shutdown, so they sometimes can slip through testing. Another fact about start-up and shutdown issues is that they can be dependent on multiple factors, such as input bulk capacitance, load, input voltage, and thermals. For example, if a ceramic or aluminum capacitor changes effective capacitance due to temperature, and a BJT current rating is also affected by temperature, then a particular case of load and input capacitance and BJT current could occur in deployment that was not observed in the lab.
- EMI Failure - there are two main tests for EMI: conducted emissions and radiated emissions. Conducted emissions are typically lower frequency (in EMI terms, around the switching frequency), and radiated emissions are higher frequency (example, 30 MHz).
  - Conducted emissions have a few fixes:
    - EMI choke
    - Increasing the common-mode capacitance
    - Decreasing the amount of copper a MOSFET has on a layout -- or shielding it with a ground plane
  - Radiated emissions have a few fixes:
    - Shielded cable
    - Shielded transformer
    - Ferrite beads *
    - Increasing the resistor on the gate of a MOSFET
    - Adjusting the snubber or RCD clamp on a MOSFET or switching diode – if the rise time period matches a frequency of concern, then that switching component is likely causing that EMI issue. Therefore, adjusting the clamp or snubber should help slow down the rise time which should help the EMI.
    - Metal casing of the entire design
    - Good ground planes with many vias connecting them across the layers
    - Putting ground planes next to critical switching traces
    - The overall PCB layout can contribute to EMI

Note

* Make sure they are in series with the EMI choke; not in parallel.

- Common factors that lead to low efficiency:
  - Transformer selection: The transformer sets the foundation of the DC/DC since it has the primary inductance and turns ratios. Additionally, increased resistance here can lead to efficiency loss. Changing the size of the transformer can also affect the performance.
  - MOSFET or Diode selection:
    - Too slow
    - Too low of a Vds

    - Too small of a package
    - Too much charge or internal capacitance
    - Higher $R_{DS(ON)}$
    - Parts that have a wide tolerance for any/all of these parameters
  - Altering with resistors on snubbers or gate drives. These are tuned to the correct value, and changing them will result in more power being dissipated across them.
  - The switching frequency: changing the switching frequency will alter the DC/DC performance. First, the transformer primary inductance is specified for the specific switching frequency. The entire feedback network is also based on the switching frequency. The Current Sense output current threshold is based on the switching frequency. Additionally, the switching MOSFETs and diodes may not be fast enough for the new switching frequency. Their snubbers and RCD clamps will also need to be adjusted.
  - ACF Delay timing could be incorrect

5 Conclusion

To summarize, DC/DC design and PoE design are not simple tasks. This guide discusses some first steps to debug a PoE PD design. Following this guide helps find where the issue is occurring, if not discovering the issue itself. Narrowing down the problem area expedites the debug process for an experienced PoE PD debug engineer.

Review each component in the schematic, using the *PoE PD Schematic Review Guidelines* application report, which discusses every component in the design. Many PoE PD issues are found in the schematic, which is a great place to start the debug process.

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