Application Note

AM62L Power Supply Implementation

ABSTRACT

This application note describes the AM62L power supply implementation for different use cases and low power modes. The power delivery network (PDN) in this document can be used as a guide for integrating PMIC or discrete power designs into applications using the Texas Instruments AM62L Sitara™ Processor. Example supply and digital diagrams are provided to assist the design process. For any questions or technical support needed to assist the design process, use the TI E2E™ design support forum.

Table of Contents

List of Figures

List of Tables

Trademarks

Sitara™ and TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

1 Introduction

The AM62L Arm-based processor is a low-cost, power-efficient system-on-chip (SoC) designed for a wide range of industrial and general-purpose applications. With two ARM Cortex-A53 cores, the AM62L processor provides robust computing with necessary security features such as secure boot. The device enables fast & efficient development with the scalable software development kits (SDK), open-source hardware and design tools. This SoC is designed for smart metering, EV charging, IOT gateways, industrial HMI, patient monitoring among others.

AM62L was developed with a power management architecture that enables lower power dissipation, lower BOM cost and flexible power design. This power architecture requires 4-5 external regulators to supply the main CORE (VDD_CORE), RAM (VDDR_CORE), DDR PHY IO (VDDS_DDR), VDDA analog supply (can be combined with 1.8V IO with proper filtering) and 1.8V/3.3V IO supplies. Table 1-1 highlights some of the benefits of the SoC power architecture.

Note

In the event of any inconsistency between user's guide, application report, or other referenced material, the data sheet specification is the definitive sources.

Table 1-1. AM62L Power Architecture Features

Power Architecture Features	Benefits
✓ Low Power Modes	4 low power modes (RTC Only, RTC + IO + DDR, DeepSleep and Standby) significantly reduce power consumption and allows higher power efficiency and longer battery lifetime.
✓ Active Power	Low active power and OS Idle allows to reduce power during lower activity use cases.
✓ CORE voltage	Differentiated low power capability with 0.75V fixed core voltage supply supports up to 1.25GHz dual A53.
✓ Voltage domain	Single CORE voltage domain enables low cost power design and simpler software control for power management.
✓ Internal dual voltage LDO	Integrates a 3.3V LDO (SDIO) that can be switched to 1.8V to supply SD card interface and support UHS-I speed. This internal LDO allows designers to reduce BOM size and cost by eliminating the need for an external dual voltage LDO.
✓ Power Supply Implementation	Flexible power sequencing and supply consolidation simplifies the PMIC or discrete power implementation and allows optimization for lower BOM size and cost.
✓ Companion PMIC	TPS65214 is a 3.5mm x 3.5mm cost and space optimized power management IC (PMIC) developed to power the AM62L. This is integrated supervisor and sequencer allow to monitor all power rails and fully control the sequencing.

2 TPS65214 Overview

The TPS65214 PMIC contains five regulators; 3 Buck regulators and 2 Low Drop-out Regulators (LDOs). The Buck converters are capable of supporting up to 2A for Buck1, and 1A each for the remaining buck regulators. LDO1 can support a maximum output current of 300mA, and LDO2 can support a maximum output current of 500mA. Both LDOs can also be configured as load switches. With a VIN range of 2.5V to 5.5V, the PMIC can support a common 3.3V or 5V system voltage. Figure 2-1 shows a summary of the voltage and current capabilities for each of the analog resources. With an I2C interface, two GPIO pins, and three multi-function pins, the TPS65214 PMIC provides the full power package to supply the AM62L SoC and the principal peripherals.

There are different orderable part numbers (OPNs) of the TPS65214 device with unique OTP settings to support different application use cases. Each TPS65214 device is distinguished by the part number and TI_DEV_ID / NVM_ID register fields. Digits #9-10 of the part number represent the default OTP configuration. For example, TPS6521401 has unique OTP settings to support the voltage and sequencing requirements of the AM62L SoC.

Note

TPS6521401 is used in the AM62L EVM

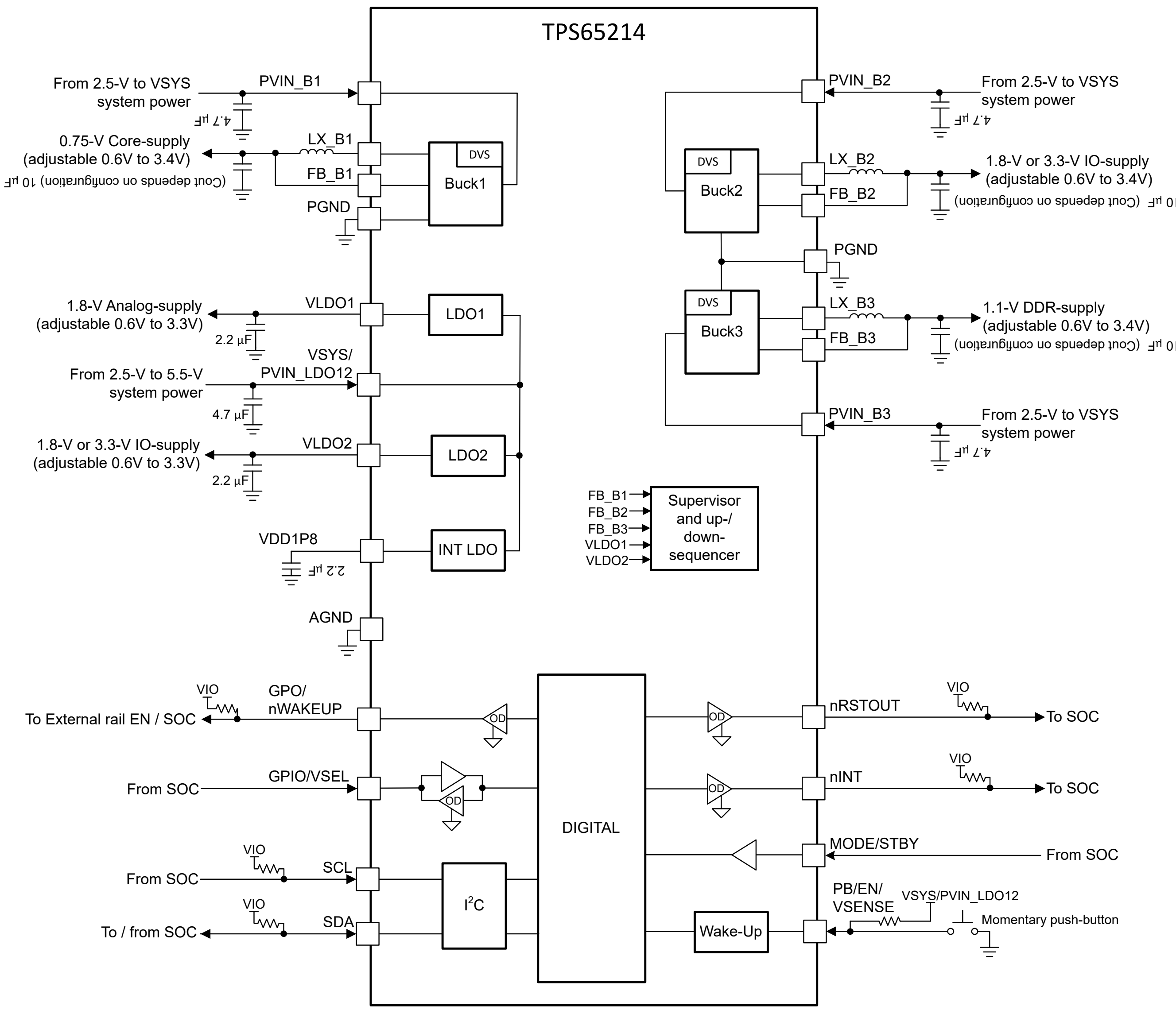

Figure 2-1. TPS65214 Functional Block Diagram

3 Low Power Modes and Power Supply Optimization

The AM62L offers the following low power modes: RTC only, RTC + IO + DDR, DeepSleep and Standby. Refer to the Power section of the *AM62L Technical Reference Manual* for a detailed description of each low power mode and the supported wakeup sources. At a high level, during *RTC only* the RTC rails (VDDS_RTC / VDD_RTC) stay ON and the remaining power rails are turned-off. During *RTC + IO + DDR* the main CORE (VDD_CORE) and the 1.8V analog (VDDA) are turned-off while the remaining rails stay-ON. In contrast, when supporting DeepSleep and Standby all the external power rails stay ON. Table 3-1 shows three PDNs for different power optimization based on the required low power modes.

For applications not using low power modes: PDN#1 is recommended if the total 3.3V IO current is lower than 500mA. If total 3.3V IO current is higher than 500mA, PDN#2 is recommended.

Table 3-1. AM62L Power Delivery Network (PDN)

Power Supply Optimization	Low Power Modes			
	RTC only	RTC + IO + DDR	DeepSleep	Standby
BOM size, cost (PDN#1) (1)			✓	✓
Lowest Suspend Power (PDN#2)		✓	✓	✓
Fully Flexible Design (PDN#3)	✓	✓	✓	✓

(1) PDN#1 uses a custom PMIC configuration that is available upon request for high volume applications.

3.1 PDN#1: Optimized Power Design for BOM Size and Cost

The Power Delivery Network (PDN) described in this section offers a power design optimized for smaller BOM size and lower cost. It uses a single 3.5mm x 3.5mm Power Management IC (PMIC) to supply all the SoC power domains. Alternatively, discrete components can be used to implement the power design. Figure 3-1 shows the PMIC implementation. This PDNs can be used for applications not using *RTC only* and *RTC + IO + DDR* low power modes.

Highlights:

- Estimated BOM size: **36.97mm²** (does not include PCB clearance).
- All SoC voltage domains are supplied with a single PMIC if total current on 3.3V IO (including AM62L + peripherals) is lower than 500mA.
- If total current on 3.3V IO (including AM62L + peripherals) is higher than 500mA, refer to Section 3.2
- When using 3.3V input supply (lowest power consumption), PMIC LDO2 is configured as 3.3V load-switch.
- When using 5V input supply, PMIC LDO2 is configured as 3.3V LDO.

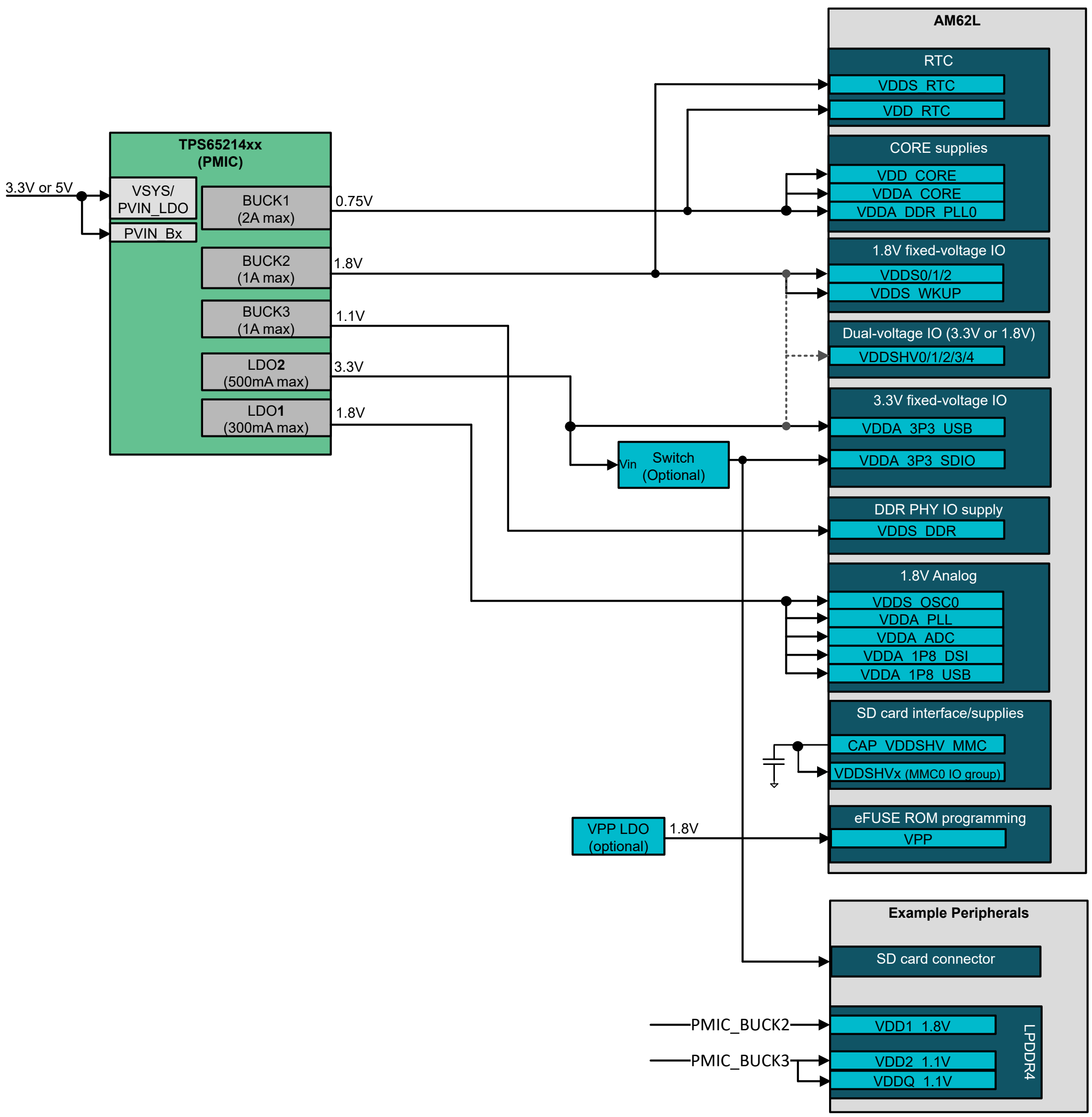

Figure 3-1. AM62L PDN Optimized for BOM Size and Cost

Note

The power-switch connected to VDDA_3P3_SDIO is optional and only needed if the application uses SD card. The VPP 1.8V LDO is optional and only needed if on-board eFuse programming is required. Refer to Appendix A for an example discrete implementation.

Figure 3-2 shows the digital connections between SoC and PMIC for PDN#1. It also shows the digital pins that require external pull-up resistors. The PMIC enable pin (EN/PB/VSENSE) can be driven with the power-good signal of the pre-regulator. Alternatively, this signal can be pulled up to PMIC_VSYS if the pre-regulator does not integrate a power-good signal. The PMIC nRSTOUT drives the RTC power-on reset (RTC_PORz) and SoC main reset (PORz). This is allowed when not supporting *RTC only* and *RTC + IO + DDR* low power modes. The PMIC_LPM_EN0 drives the PMIC MODE/STBY pin to switch the DCDC switching mode from forced-PWM to auto-PFM and to improve power efficiency during DeepSleep and Standby/OS Idle low power modes. This is optional and require the PMIC MODE/STBY pin to be configured as "MODE".

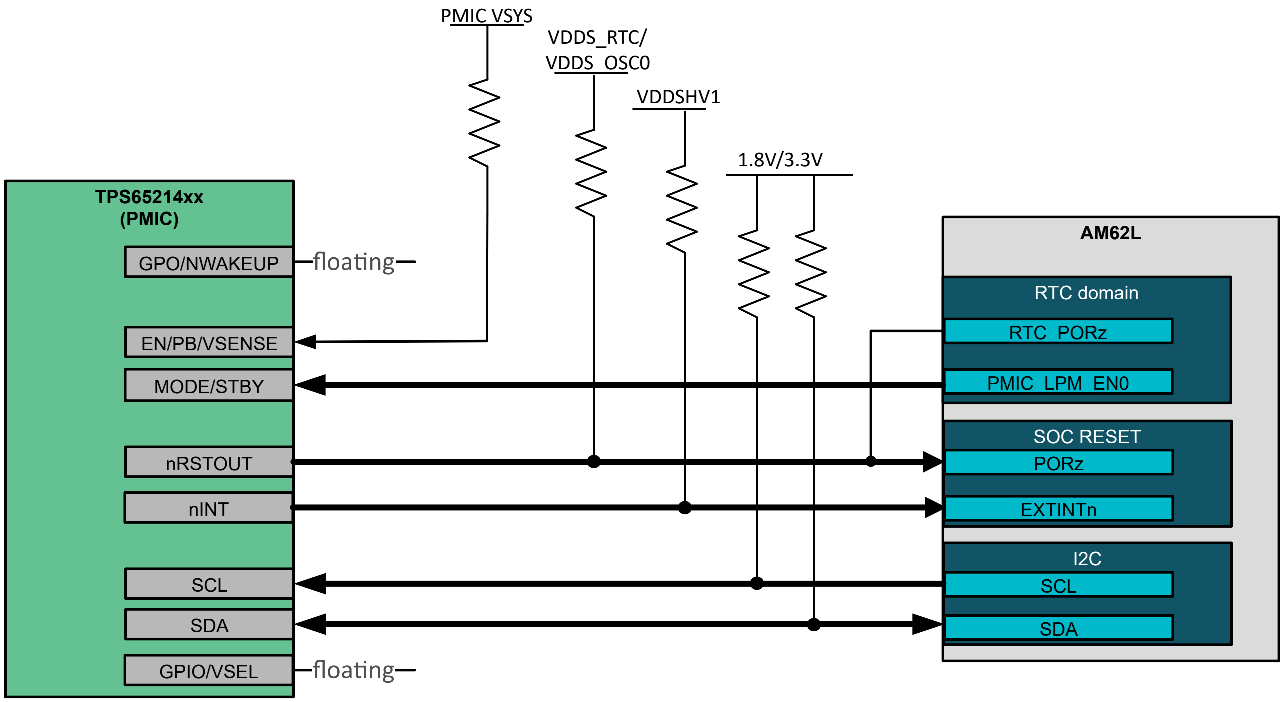

Figure 3-2. SoC - PMIC Digital Connections for PDN#1

Note

PMIC_LPM_EN0 does not require an external pull-up resistor; The SoC has an internal pullup resistor that drives the signal high if VDDS_RTC is powered. PORz is 3.3V tolerant and the external pull-up resistor can be connected to a 1.8V supply or 3.3V supply as long as VDDS_OSC0 is powered.

AM62L	Power Supply		Qty	Example component	Component Value	Length (mm)	Width (mm)	Area (mm2)
NA	PMIC rails	PMIC IC package	1	TPS65214	N/A	3.5	3.5	12.25
		VSYS/PVIN_LDO	1	C1608X7S1A475K080AC	4.7uF	1.6	0.8	1.28
		VDD1P8 - Cout	1	C1005X7S1A225K050BC	2.2uF	1	0.5	0.5
VDD_CORE VDD_RTC		BUCK1-L	1	TFM201208BLE-R47MTCF	0.47µH	2	1.2	2.4
		BUCK1-Cin	1	C1608X7S1A475K080AC	4.7µF	1.6	0.8	1.28
		BUCK1-Cout	2	GRM21BZ71A226ME15L	22µF	2	1.25	5
VDDS_DDR		BUCK3-L	1	TFM201208BLE-R47MTCF	0.47µH	2	1.2	2.4
		BUCK3-Cin	1	C1608X7S1A475K080AC	4.7µF	1.6	0.8	1.28
		BUCK3-Cout	1	GRM21BZ71A226ME15L	22µF	2	1.25	2.5
1.8V IO		BUCK2-L	1	TFM201208BLE-R47MTCF	0.47µH	2	1.2	2.4
		BUCK2-Cin	1	C1608X7S1A475K080AC	4.7µF	1.6	0.8	1.28
		BUCK2-Cout	1	GRM21BZ71A226ME15L	22µF	2	1.25	2.5
3.3V IO		LDO1-Cin	0	shares Cin with VSYS	NA	0	0	0
		LDO1-Cout	1	C1005X7S1A225K050BC	2.2µF	1	0.5	0.5
VDDA (1.8V analog)		LDO2-Cin	0	shares Cin with VSYS	NA	0	0	0
		LDO2-Cout	1	C1005X7S1A225K050BC	2.2uF	1	0.5	0.5
Resistors		Digital Pull-up Res	5	Example: 0201 10K pull-ups	NA	0.6	0.3	0.9
							Total Size	36.97

Figure 3-3. PMIC BOM Example

3.2 PDN#2: Optimized Power Design for Lowest Suspend Power

The Power Delivery Network (PDN) described in this section is optimized for the lowest suspend power and supports all low power modes except *RTC only* mode. The PDN uses a 3.5mm x 3.5mm PMIC and an external 3.3V discrete regulator to supply all the SoC power domains. This PDN is recommended for applications using *RTC + IO + DDR* low power mode or requiring more than 500mA current on the 3.3V IO. This PDN is designed to turn-OFF VDD_CORE and VDDA when entering *RTC + IO + DDR* low power mode to reduce power consumption. Figure 3-4 shows the PMIC implementation using TPS6521401 configuration.

Highlights:

- Uses TPS6521401 PMIC. This PMIC configuration is used in the AM62L EVM. Hardware design files available.
- Estimated BOM size for 3.3V input supply (PMIC + 3.3V power-switch): **41.69mm²** (does not include PCB clearance). Power-switch example: TPS22954.
- Estimated BOM size for 5V input supply (PMIC + 3.3V Buck): **58.68mm²** (does not include PCB clearance). Buck example: TPS62A01.
- External 3.3V discrete is scalable based on the total current needed for 3.3V IO (including SoC + peripherals).

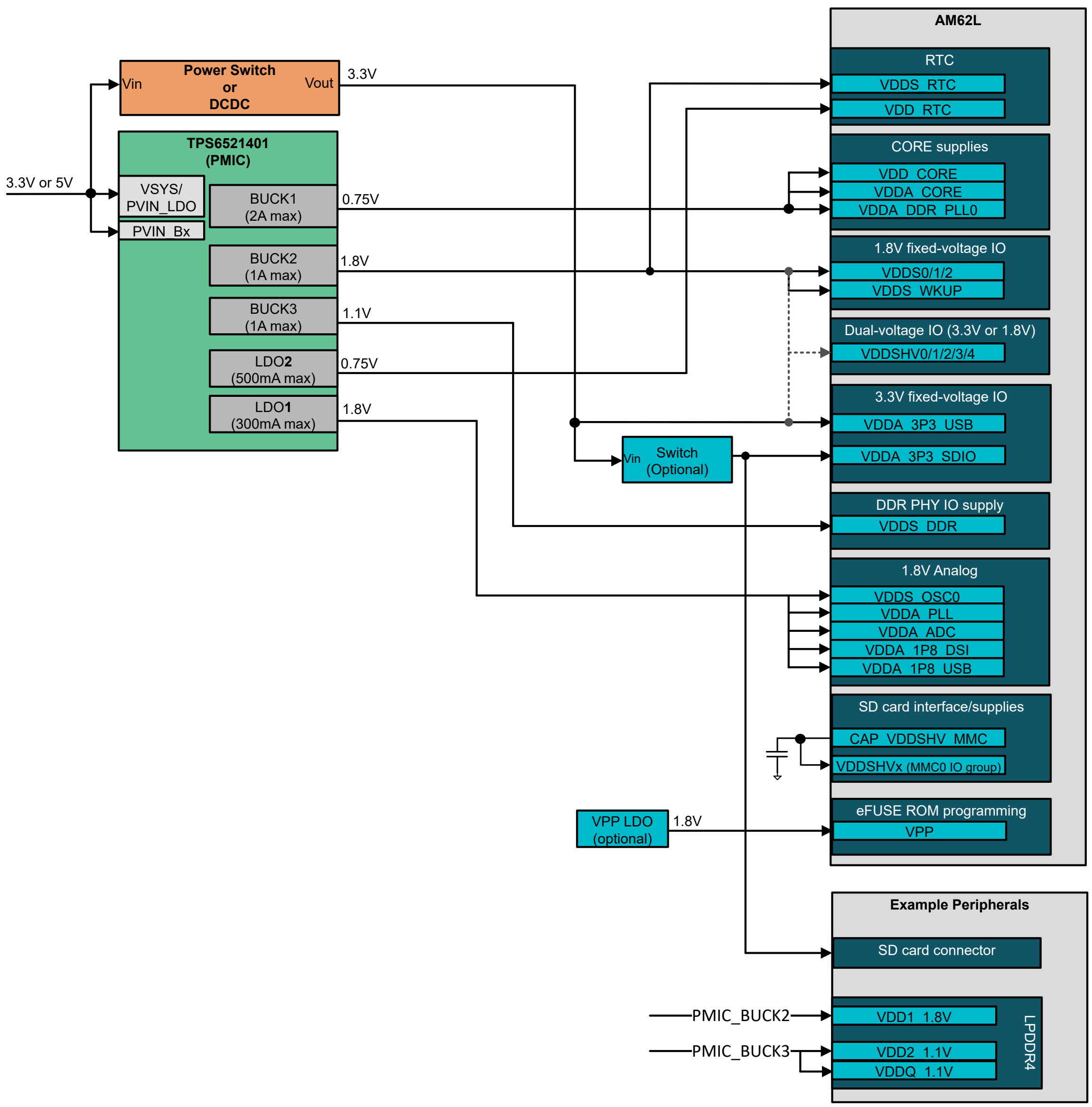

Figure 3-4. AM62L PDN Optimized for Lowest Suspend Power

Note

The power-switch connected to VDDA_3P3_SDIO is optional and only needed if the application uses SD card. The VPP 1.8V LDO is optional and only needed if on-board eFuse programming is required.

Figure 3-5 shows the digital connections between SoC and PMIC for PDN#2. It also shows the digital signals that require external pull-up resistors. The PMIC enable pin (EN/PB/VSENSE) can be driven with the power-good signal of the pre-regulator. Alternatively, this signal can be pulled up to PMIC_VSYS if the pre-regulator does not integrate a power-good signal. The PMIC nRSTOUT and the power-good signal of the 3.3V IO drives the main SoC reset (PORz). PMIC GPO is configured to act as the power-good signal of the RTC rails (BUCK2 and LDO2) and drives the RTC power-on reset (RTC_PORz). The PMIC_LPM_EN0 drives the PMIC MODE/STBY pin to pull PORz low and turn-off VDD_CORE (BUCK1) as well as VDDA (LDO1) when entering "RTC + IO + DDR" low power modes.

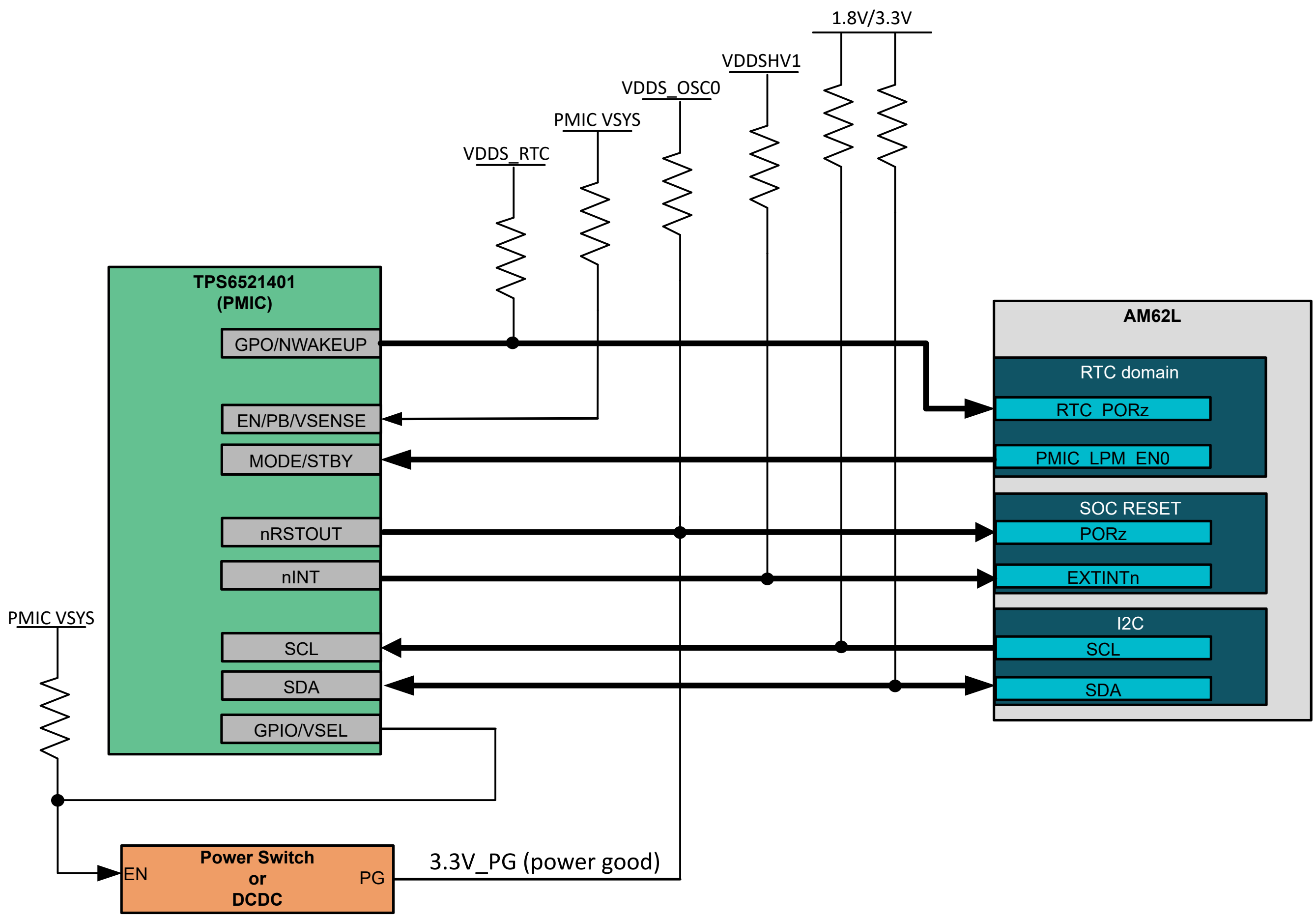

Figure 3-5. SoC - PMIC Digital Connections for PDN#2

Note

PMIC_LPM_EN0 does not require an external pull-up resistor; The SoC has an internal pullup resistor that drives the signal high if VDDS_RTC is powered. PORz is 3.3V tolerant and the external pull-up resistor can be connected to a 1.8V supply or 3.3V supply as long as VDDS_OSC0 is powered.

Table 3-2. TPS6521401 Digital Config

	OTP Config	Polarity
EN/PB/VSENSE	Configured as *Enable*	• High: PMIC executes power-on sequence. • Low: PMIC executes power-down sequence.
MODE/STBY	Mode and Standby	• High: PMIC in Active state. All rails enabled. Bucks operate in forced-PWM. • Low: PMIC in Standby state. Buck1 and LDO1 are turned-OFF. Bucks operate in auto-PFM.
GPIO/nWAKEUP	Open-drain GPO	• Configured to act as the *power-good* signal of Buck2 and LDO2. This digital pin drives RTC_PORz and stays high/Z when PMIC enters Standby state to support the AM62L RTC+DDR low power mode.
GPIO/VSEL	Open-drain GPO	• Configured to enable/disable external 3.3V discrete device.

Note

Refer to the *TPS6521401 Technical Reference Manual* to access the full list of default PMIC OTP register settings.

3.3 PDN#3: Fully Flexible Power Design

The Power Delivery Network (PDN) described in this section offers a flexible PMIC + discrete power solution that allows supporting all the SoC low power modes. This PDN supports *RTC only* low power mode by isolating VDDS_RTC (1.8V) and VDD_RTC (0.75V) from the remaining power rails. Supplying the RTC domain with always-ON discrete devices allows to significantly reduce power consumption during *RTC only* low power mode by turning-OFF the entire PMIC and the external 3.3V discrete while only keeping the RTC rails ON. When entering *RTC only* low power mode, the AM62L PMIC_LPM_EN signal drives the PMIC enable pin low. Figure 3-6 shows the PMIC + discrete power implementation.

Highlights:

- This PDN can be implemented with the TPS6521**401** PMIC (PMIC OTP configuration used in the AM62L EVM).
- Supports all AM62L low power modes.
- BOM size is highly dependent on the selected discrete devices for the RTC rails and the 3.3 IO.
- When using 3.3V input supply (lower power consumption), external 3.3V power switch is used. Example IC: TPS22954.
- When using 5V input supply, external 3.3V DCDC is used. Example IC: TPS62A01.
- External 3.3V discrete current rating is scalable based on the total current needed for 3.3V IO.

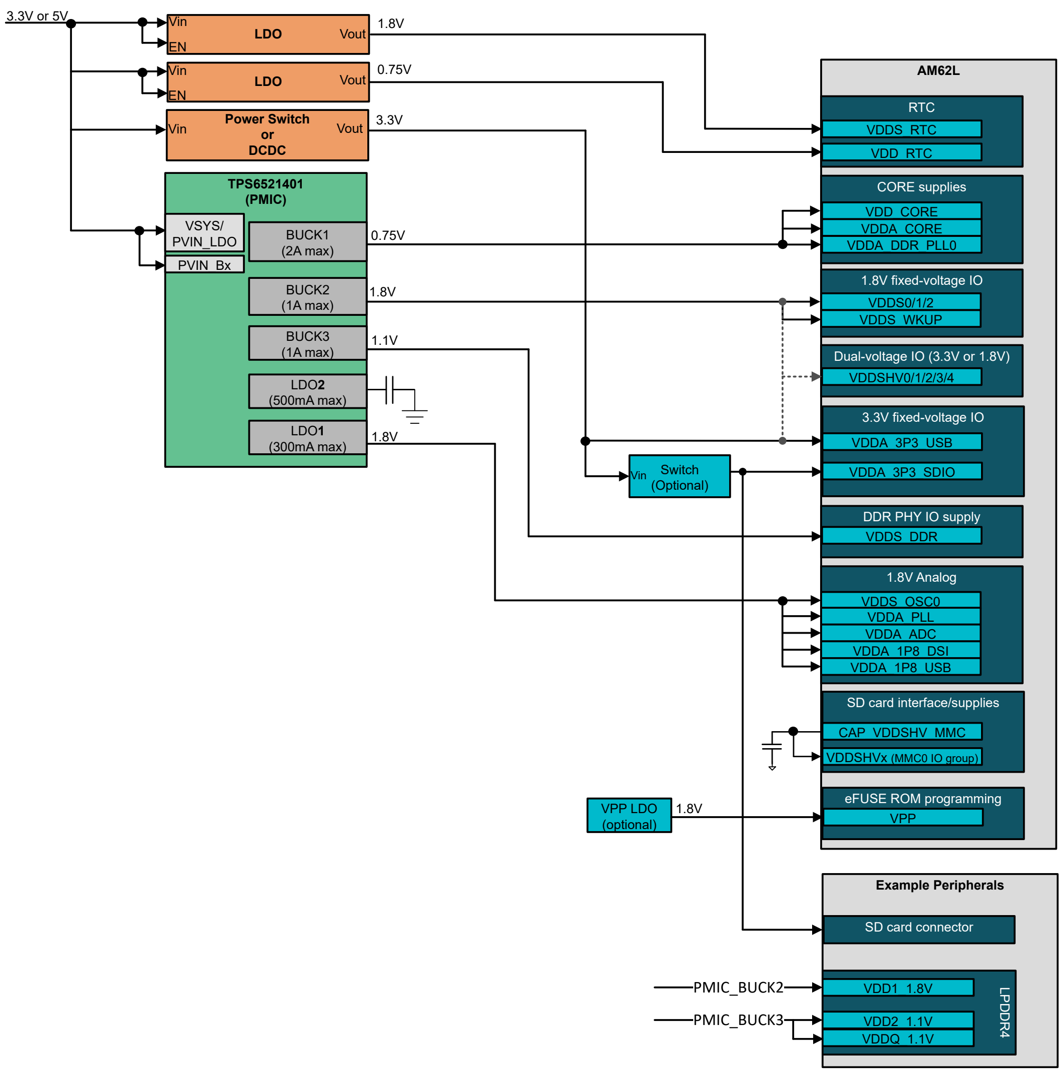

Figure 3-6. AM62L Fully Flexible PDN

Note

The power-switch connected to VDDA_3P3_SDIO is optional and only needed if the application uses SD card. The VPP 1.8V LDO is optional and only needed if on-board eFuse programming is required.

Figure 3-7 shows the digital connections between SoC and PMIC for PDN#3. It also shows the digital signals that require external pull-up resistors. The SoC PMIC_LPM_EN0 drives the PMIC enable pin (EN/PB/VSENSE) to turn-OFF the PMIC when entering *RTC only* low power mode. The combined power-good signals of the discrete LDOs that supply the RTC rails drive RTC_PORz. Additionally, an open-drain buffer between the two power-on resets allows to pull the PORz low and keep the SoC in reset if a fault is detected on the external discrete LDOs. The PMIC nRSTOUT, the power-good signal of the 3.3V IO and the output of the open-drain buffer drive the main SoC reset (PORz).

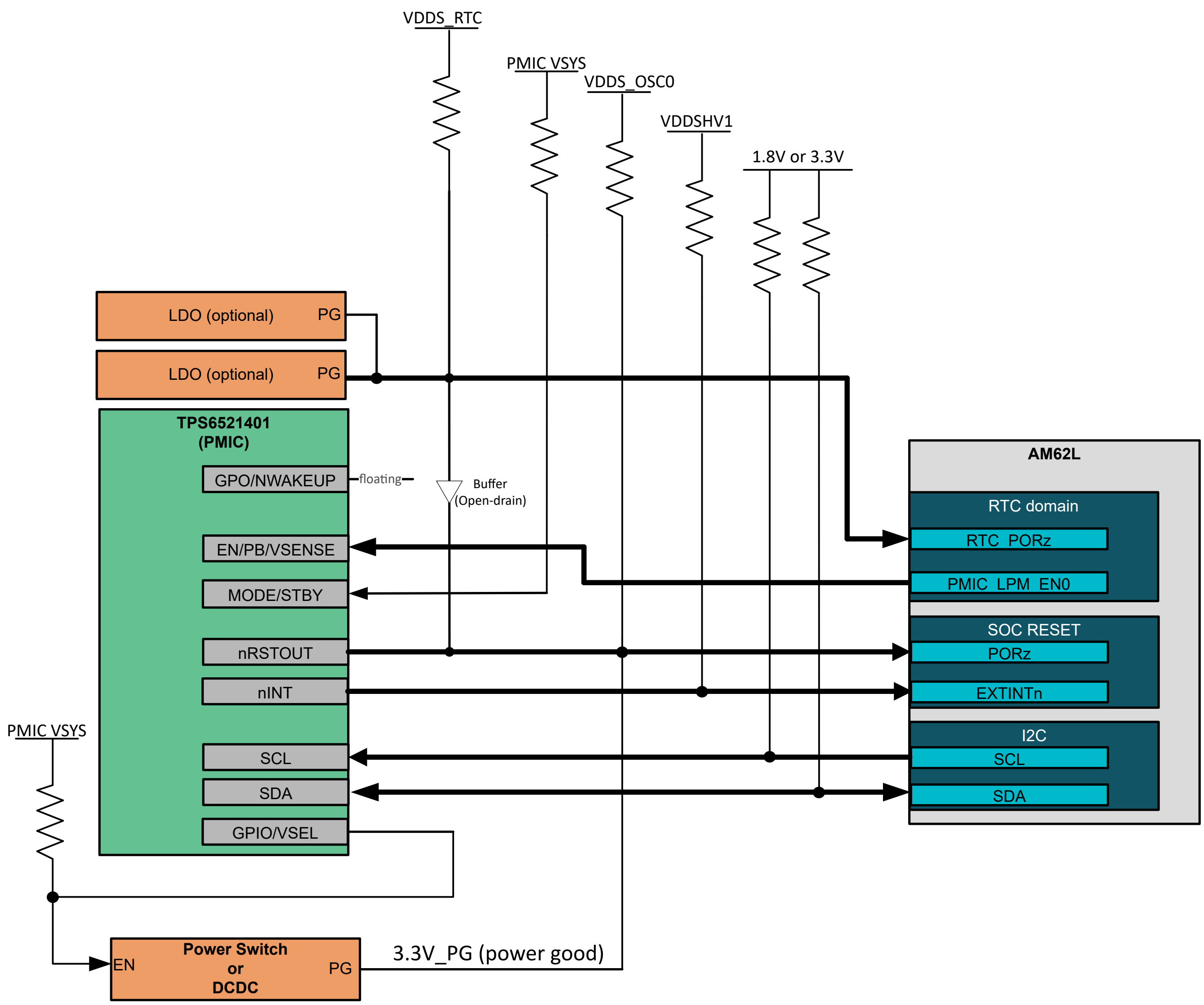

Figure 3-7. SoC - PMIC Digital Connections for PDN#3

Note

PMIC_LPM_EN0 does not require an external pull-up resistor; The SoC has an internal pullup resistor that drives the signal high if VDDS_RTC is powered. PORz is 3.3V tolerant and the external pull-up resistor can be connected to a 1.8V supply or 3.3V supply as long as VDDS_OSC0 is powered.

4 Power-Up Sequence

Figure 4-1 shows the power-up sequencing using the TPS6521401 OTP configuration as a reference. Refer to the AM62L data sheet for a detailed sequencing waveforms and requirements.

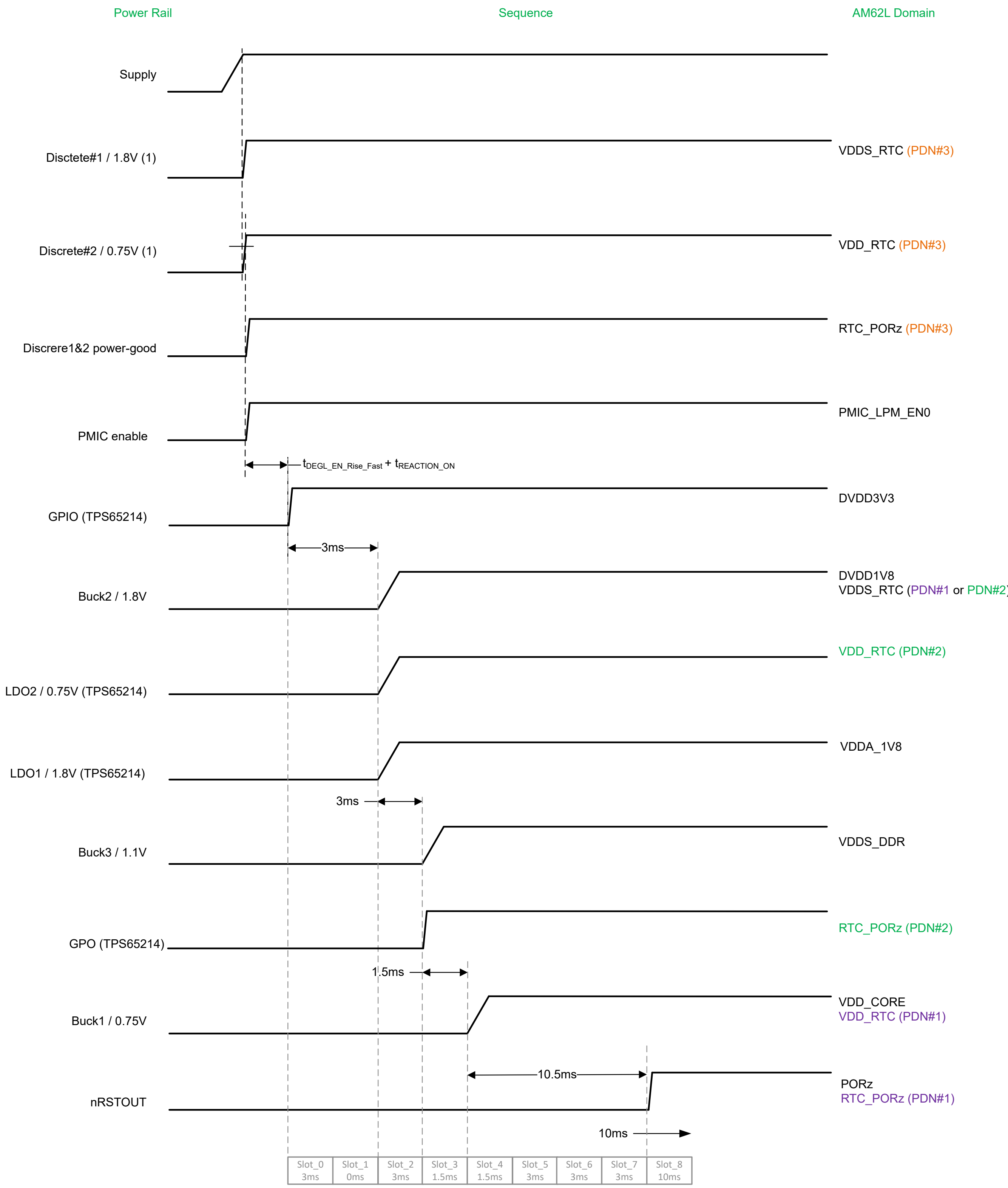

Figure 4-1. AM62L Power-Up Sequence

5 Power-Down Sequence

Figure 5-1 shows the power-down sequencing using the TPS6521401 OTP configuration as a reference. This power-down sequence do not cover the SoC sequencing from Active to Low Power Modes. The diagram only represents the power-down sequence when an OFF request is sent to the PMIC by hardware (pulling the enable pin low) or by software (I2C OFF request). Refer to the AM62L data sheet for a detailed sequencing waveforms and requirements.

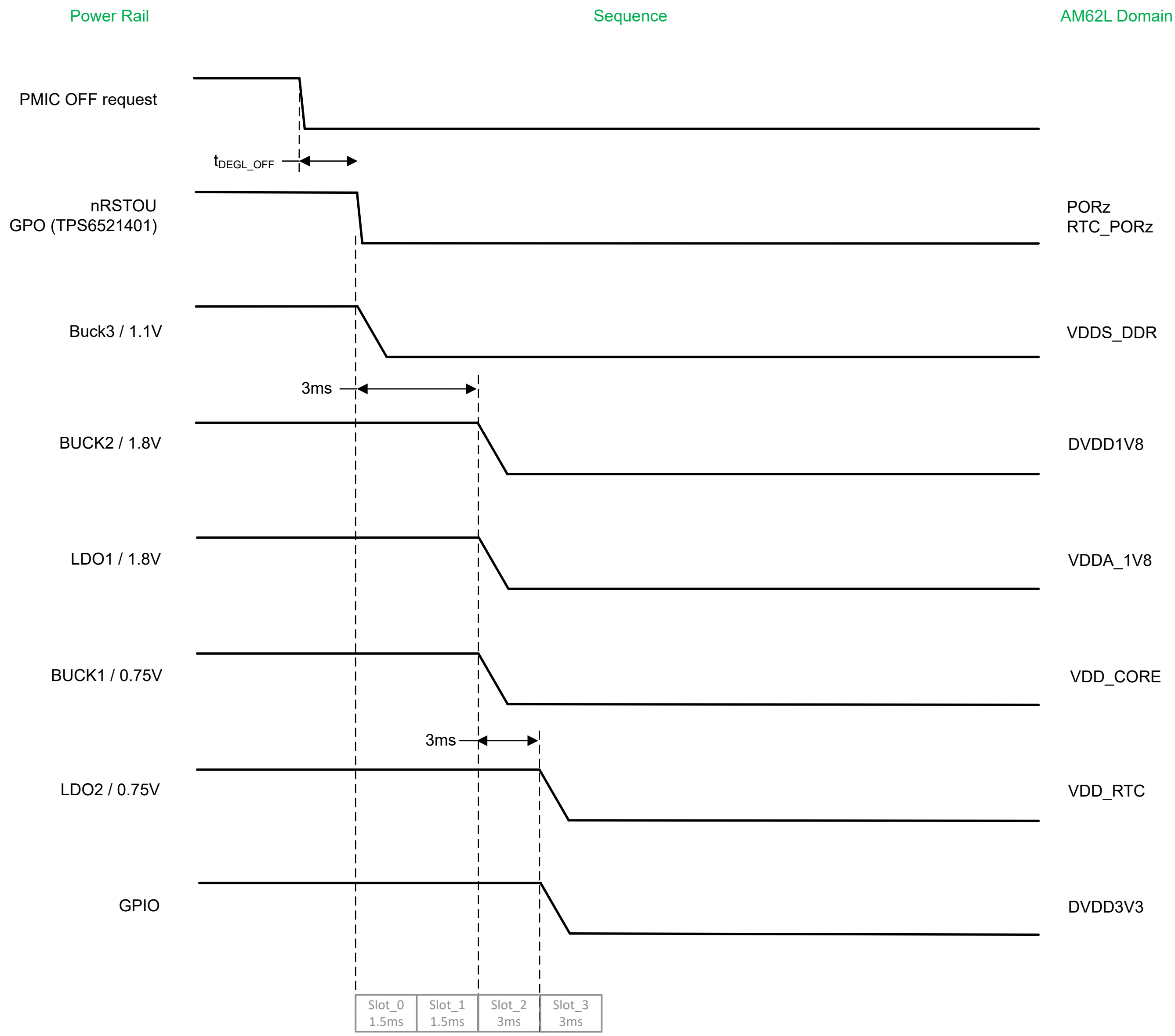

Figure 5-1. AM62L Power-Down Sequence

6 Summary

The AM62L power architecture was developed with features that allow designers to reduce power consumption as well as BOM area and cost. The three power delivery network (PDNs) described in this application note show examples of how the power design can be optimized to meet system level requirements that include lowering BOM area, cost and power consumption during low activity.

7 References

- Texas Instruments, *AM62Lx Sitara™ Processors*, data sheet.
- Texas Instruments, *AM62L Technical Reference Manual*.
- Texas Instruments, *TPS65214 Integrated Power Management IC Processors*, data sheet.
- Texas Instruments, *TPS6521401 Technical Reference Manual*.

A Appendix A: Discrete Power Implementation for PDN#1

This section describes the discrete power implementation for PDN#1. The Optimized Power Solution for BOM size and cost can also be implemented using discrete components with attributes equivalent to the devices listed below. Figure A-1 shows an example supply diagram for a 5V input supply and LPDDR4 use case.

- VDD_CORE (0.75V): TPS62A02
- VDDS_DDR (1.1V): TPS62A01
- VDDSHV (3.3V IO / 1.8V IO)
  - if total current > 500mA: TPS62A01 (DCDC)
  - if total current < 500mA: TPS74501 (LDO)
- VDDA (1.8V analog): LP5912 (low noise LDO)

Note

This discrete PDN is an example supply implementation and has not been tested or validated by TI.

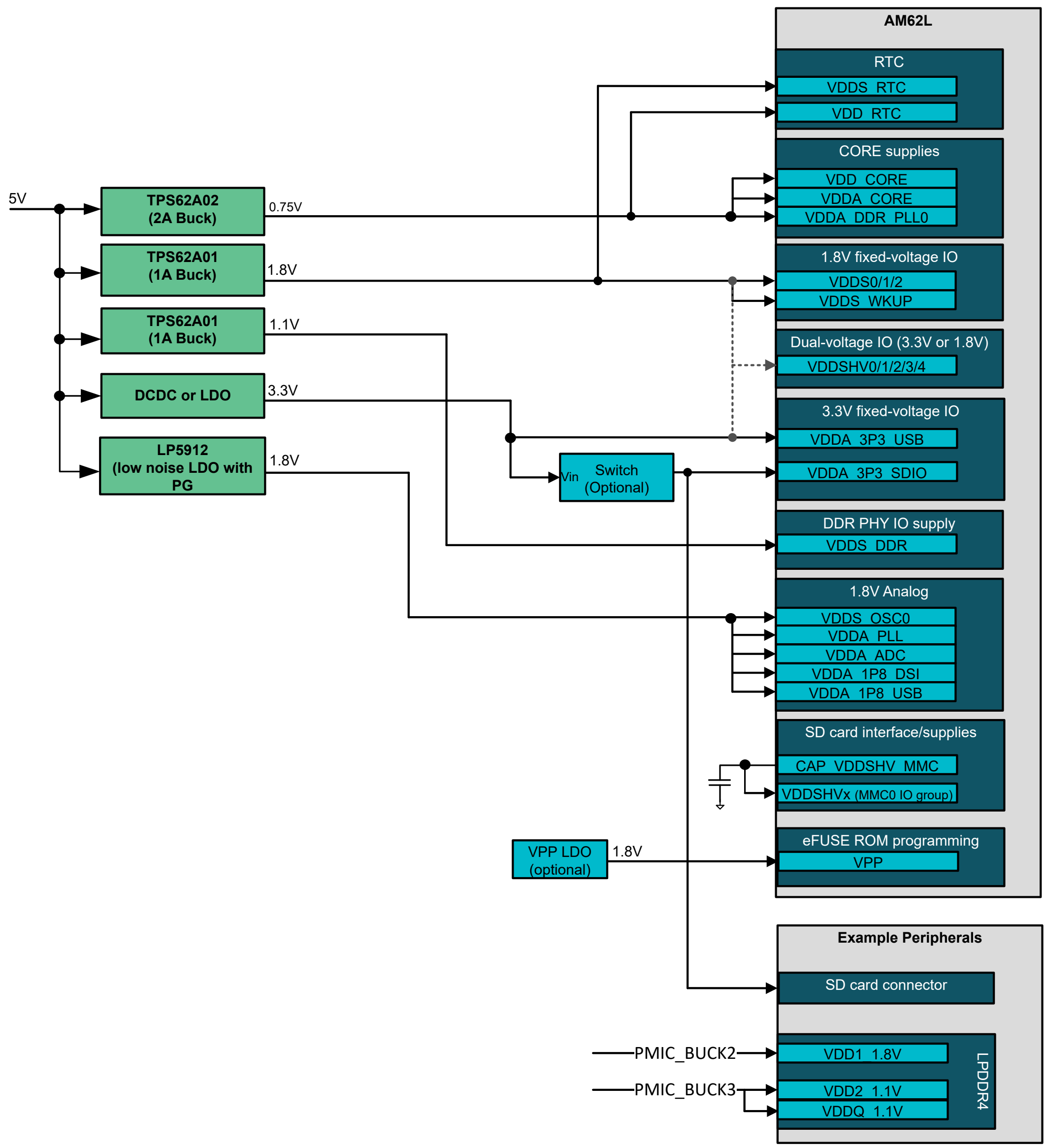

Figure A-1. PDN Optimized for BOM Size and Cost - Discrete Implementation

Note

The power-switch connected to VDDA_3P3_SDIO is optional and only needed if the application uses SD card. The VPP 1.8V LDO is optional and only needed if on-board eFuse programming is required.

AM62L	Discrete Power	Qty	Example component	Component Value	Length (mm)	Width (mm)	Area (mm2)
VDD_CORE VDD_RTC	Buck IC	1	TPS62A02DRLR	2A Buck	1.6	1.6	2.56
	BUCK1-L	1	XGL3520-102MEC	1.0uH	3.5	3.2	11.2
	BUCK1-Cin	1	GRM21BR71A475KA73L	4.7uF	2	1.25	2.5
	BUCK1-Cout	2	GRM21BZ71A226KE15L	22uF	2	1.25	5
	Resistors	3	Resistor, Chip, 0.1 W, 1%	0603 std resistor	1.6	0.8	3.84
VDDS_DDR	Buck IC	1	TPS62A01DRLR	1A Buck	1.6	1.6	2.56
	BUCK3-L	1	DFE252012F-1R0M	1.0uH	3.5	3.2	11.2
	BUCK3-Cin	1	GRM21BR71A475KA73L	4.7uF	2	1.25	2.5
	BUCK3-Cout	1	GRM21BZ71A226KE15L	22uF	2	1.25	2.5
	Resistors	3	Resistor, Chip, 0.1 W, 1%	0603 std resistor	1.6	0.8	3.84
1.8V IO	Buck IC	1	TPS62A01DRLR	1A Buck	1.6	1.6	2.56
	BUCK2-L	1	DFE252012F-1R0M	1.0uH	3.5	3.2	11.2
	BUCK2-Cin	1	GRM21BR71A475KA73L	4.7uF	2	1.25	2.5
	BUCK2-Cout	1	GRM21BZ71A226KE15L	22uF	2	1.25	2.5
	Resistors	3	Resistor, Chip, 0.1 W, 1%	0603 std resistor	1.6	0.8	3.84
3.3V IO	Buck IC	1	TPS62A01DRLR	1A Buck	1.6	1.6	2.56
	BUCK2-L	1	DFE252012F-1R0M	1.0uH	3.5	3.2	11.2
	BUCK2-Cin	1	GRM21BR71A475KA73L	4.7uF	2	1.25	2.5
	BUCK2-Cout	1	GRM21BZ71A226KE15L	22uF	2	1.25	2.5
	Resistors	3	Resistor, Chip, 0.1 W, 1%	0603 std resistor	1.6	0.8	3.84
VDDA (1.8V analog)	IC	1	LP5912	low noise LDO	2	2	4
	LDO - Cin	1	GRT033C81A105ME13D	1uF	0.6	0.3	0.18
	LDO - Cout	1	GRT033C81A105ME13D	1uF	0.6	0.3	0.18
						Total Size	97.26

Figure A-2. Discrete BOM Example

A proper logic implementation is required to meet the SoC sequencing requirements and reset architecture. Figure A-3 shows an example using LM3380 sequencer and a 6 channel open-drain buffer. The connections highlighted in orange represent the power-good signals of the devices that supply the SoC rails and the system power.

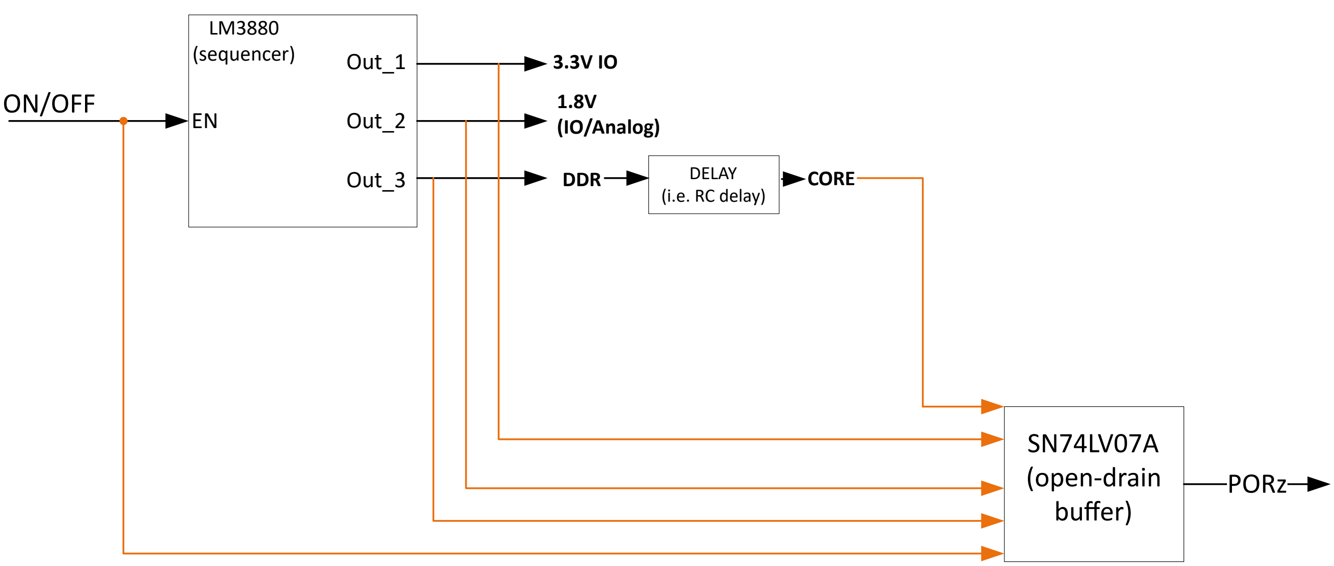

Figure A-3. Logic Implementation - Example