TEXAS INSTRUMENTS

SLVP087 Buck Converter Evaluation Module

User's Guide

1998

Mixed Signal Linear Products

TEXAS INSTRUMENTS

Printed in U.S.A.
07/98

SLVU003A

SLVP087 Buck Converter Evaluation Module User's Guide

Literature Number: SLVU003A
July 1998

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Preface

Read This First

About This Manual

This user's guide is a reference manual for the SLVP087 Buck Converter Evaluation Module used to evaluate the performance of the TL5001 PWM Controller. This document provides information to assist managers and hardware engineers in application development.

How to Use This Manual

This manual provides the information and instructions necessary to design, construct, operate, and understand the SLVP087. Chapter 1 describes and lists the hardware requirements; Chapter 2 describes design considerations and procedures; and Appendix A contains the data sheet for the TL5001 PWM Controller

Related Documentation From Texas Instruments

The following books describe the TL5001 and related support tools. To obtain a copy of any of these TI documents, call the Texas Instruments Literature Response Center at (800) 477–8924. When ordering, please identify the book by its title and literature number.

TL5001 Pulse-Width-Modulation Control Circuits Data Sheet (Literature number SLVS084C) contains electrical specifications, available temperature options, general overview of the device, and application information.

Designing with the TL5001C PWM Controller Application Report (Literature number SLVA034).

If You Need Assistance . . .

If you want to . . .	Contact Texas Instruments at . . .	
Visit TI online	World Wide Web:	http://www.ti.com
Request more information about Texas Instruments Mixed Signal Products (MSP)	World Wide Web:	http://www.ti.com/sc/docs/pic/home.htm
	Call the Product Information Center (PIC) hotline:	(972) 644–5580
	Send a fax:	(972) 480–7800
	Write to:	Texas Instruments Incorporated Product Information Center, MS 3123 P.O. Box 660246 Dallas, Texas 75266
Ask questions about product operation or report suspected problems	Call the Product Information Center (PIC) hotline:	(972) 644–5580
Order Texas Instruments documentation (see Note 1)	Call the Product Information Center (PIC) hotline:	(972) 644–5580
Make suggestions about or report errors in documentation (see Note 2)	Send a fax:	MSP Marketing Documentation Correction (972) 480–3160
	Write to:	Texas Instruments Incorporated MSP Marketing Documentation Correction, MS 8710 P.O. Box 660199 Dallas, Texas 75266–0199

Notes: 1) The literature number for the book is required; see the lower-right corner on the back cover.

2) Please mention the full title of the book, the literature number from the lower-right corner of the back cover, and the publication date from the spine or front cover.

FCC Warning

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

Trademarks

TI is a trademark of Texas Instruments Incorporated.

Contents

Figures

Tables

Chapter 1

Hardware

The SLVP087 Buck Converter Evaluation Module (SLVP087) provides a method for evaluating the performance of the TL5001 pulse-width-modulation (PWM) controller. This manual explains how to construct basic power conversion circuits, including the design of the control chip functions and the basic loop. This chapter includes the following topics:

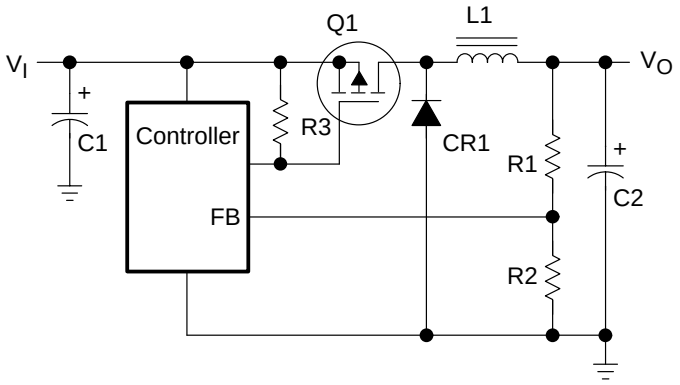
Topic **Page**

1.1 Introduction

Low cost and design simplicity make buck converters popular solutions in dc/dc step-down applications where lack of isolation from the input source is not a concern. Easy control design is another advantage of buck converters. Because continuous current mode is desirable, it is used for the low peak-to-average current ratio, easing the component worst-case design parameters.

Figure 1–1 shows a diagram of a typical buck converter. The converter passes a duty-cycle modulated waveform through a low-pass output filter (L1, C2). To maintain the desired output voltage a controller senses the output voltage, compares it to an internal reference voltage, and adjusts the width of the power switch (Q1) on time. When the power switch is turned off, a commutating diode (CR1) maintains continuous current through the inductor.

Figure 1–1. Typical Buck Converter Diagram

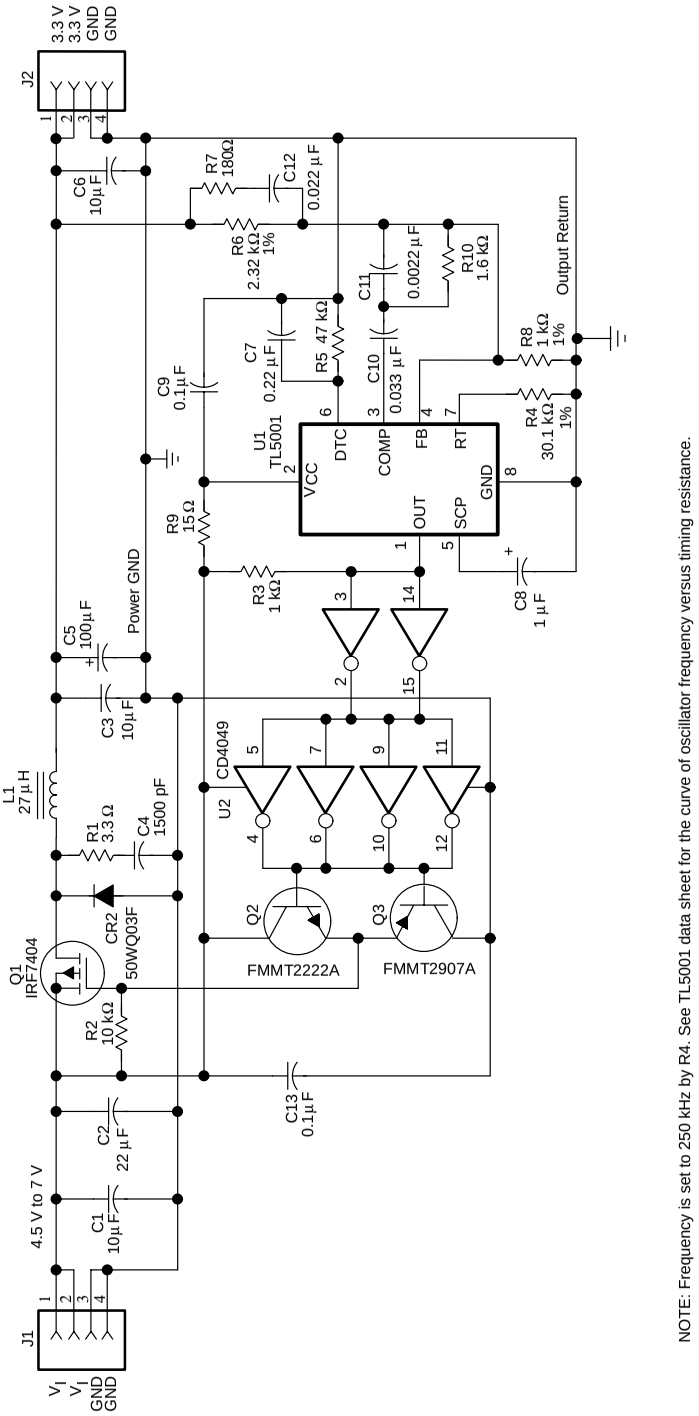


The SLVP087 buck converter uses the Texas Instruments TL5001 PWM controller to give a 0- to 3-A, 3.3-V output. The converter operates over an input voltage range of 4.5 V to 7 V with a typical efficiency of 85 percent. Chapter 2 lists full design specifications.

1.2 Schematic

Figure 1–2 shows the SLVP087 schematic.

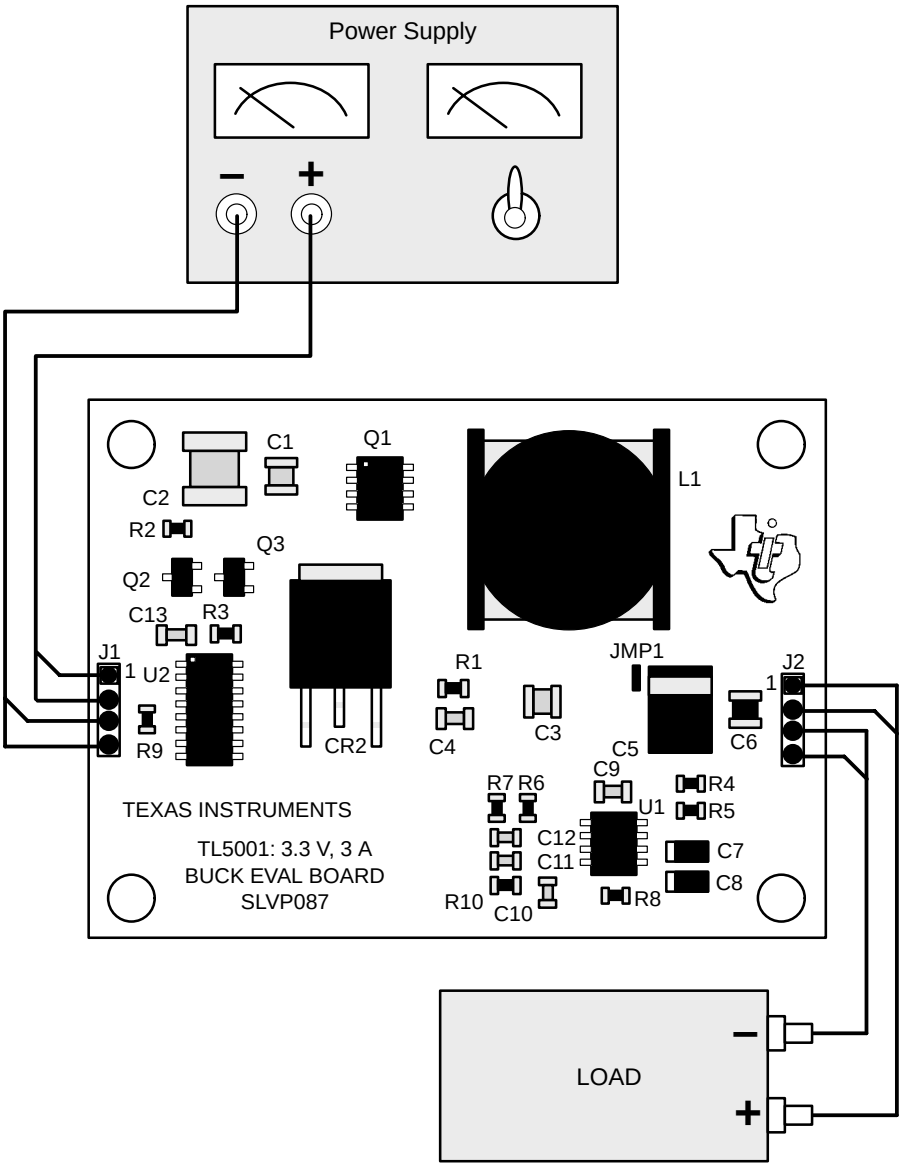
Figure 1–2. SLVP087 Schematic



1.3 Input/Output Connections

Figure 1–3 shows the SLVP087 input and output connections.

Figure 1–3. I/O Connections

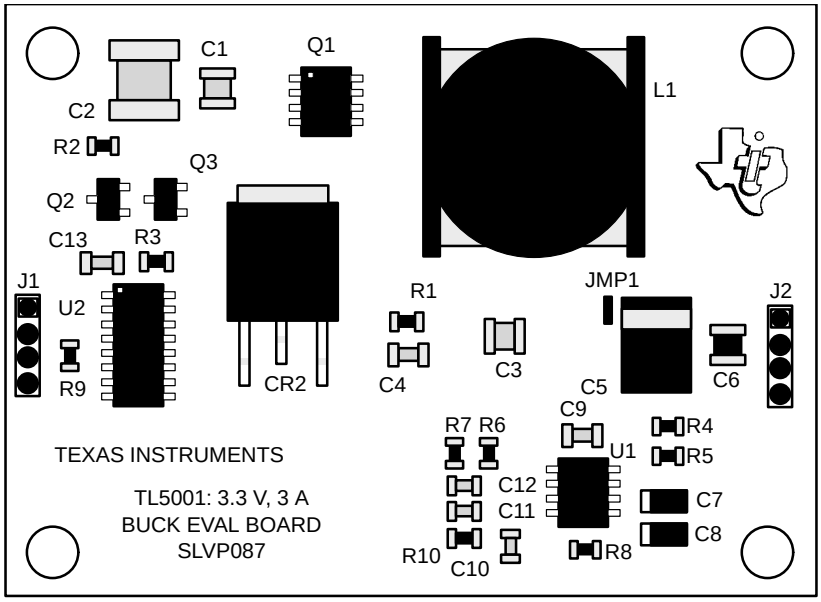


Notes: 1) Source power should be able to supply a minimum of 3 A at 4.5-V input and/or 2 A at 7-V input.
2) Load should be able to sink up to 3 A with adequate power rating. Resistive loads with adequate ratings may be used.

1.4 Board Layout

Figure 1–4 shows the SLVP087 board layout

Figure 1–4. Board Layout



1.5 Bill of Material

Table 1–1 lists materials required for the SLVP087.

Table 1–1. Bill of Materials

Qty	Reference	Part Number	Mfr	Description
3	C1, C3, C6	C3225Y5V1C106Z	TDK	Capacitor, Cer, 10 μF, 10 V, Y5V, 1210
1	C2	THCR60E1E226Z	Marcon	Capacitor, Cer, 22 μF, 25 V, Y5V, 2220
1	C4	Standard		Capacitor, Cer, 1500 pF, 5%, NPO, 0805
1	C5	TPSD107M010R0100	AVX	Capacitor, Tant, 100 μF, 10 V, D Case
1	C7	Standard		Capacitor, Cer, 0.22 μF, 10%, X7R, 1210
1	C8	ECS-T1CY105R	Panasonic	Capacitor, Tant, 1.0 μF, 20%, A Case
2	C9, C13	Standard		Capacitor, Cer, 0.1 μF, 10%, X7R, 1206
1	C10	Standard		Capacitor, Cer, 0.033 μF, 10%, X7R, 1206
1	C11	Standard		Capacitor, Cer, 0.0022 μF, 10%, X7R, 0805
1	C12	Standard		Capacitor, Cer, 0.022 μF, 10%, X7R, 0805
1	CR2	50WQ03F	IR	Diode, Schottky, 5 A, 30 V, D-Pak
2	J1, J2	TSW-104-14-G-S	Samtec	Header, 4-pin, 0.1 Sp. Gold
1	L1	SML3023	Nova Magnetics	Inductor, 27 μH, 20%, 3 A (972−272−8278)
1	Q1	IRF7404	IR	Transistor, MOSFET, p-ch, 20 V, 5.3 A, SO-8
1	Q2	FMMT2222ACT	Zetex	Transistor, NPN, 40 V, 800 mA, SOT-23
1	Q3	FMMT2907ACT	Zetex	Transistor, PNP, 50 V, 600 mA, SOT-23
1	R1	Standard		Resistor, CF, 3.3 Ω, 5%, 0805
1	R2	Standard		Resistor, CF, 10 kΩ, 5%, 0805
1	R3	Standard		Resistor, CF, 1.0 kΩ, 5%, 0805
1	R4	Standard		Resistor, MF, 30.1 kΩ, 1%, 0805
1	R5	Standard		Resistor, CF, 47 kΩ, 5%, 0805
1	R6	Standard		Resistor, MF, 2.32 kΩ, 1%, 0805
1	R7	Standard		Resistor, CF, 180 Ω, 5%, 0805
1	R8	Standard		Resistor, MF, 1.00 kΩ, 1%, 0805
1	R9	Standard		Resistor, CF, 15 Ω, 5%, 0805
1	R10	Standard		Resistor, CF, 1.6 kΩ, 5%, 0805
1	U1	TL5001CD	TI	IC, PWM Controller, SO-8
1	U2	CD4049UBM	National	IC, CMOS Hex Inverter, SO-18
1		SLVP087		PWB, 2 Layer

1.6 Test Results

Tables 1–2 and 1–3, along with Figures 1–5 through 1–9, show the test results for the SLVP087.

Table 1–2. Line/Load Regulation, 3.3 V (Total Variation)

Line/Load	0.3 A	0.9 A	1.5 A	3.0 A	5.0 A	Load Reg.
4.5 V Vo(V)	3.321	3.320	3.319	3.315	3.309	0.18%
5.0 V Vo(V)	3.322	3.320	3.318	3.315	3.309	0.21%
5.5 V Vo(V)	3.322	3.321	3.319	3.315	3.310	0.21%
6.0 V Vo(V)	3.322	3.321	3.319	3.315	3.310	0.21%
6.5 V Vo(V)	3.322	3.321	3.319	3.315	3.310	0.21%
7.0 V Vo(V)	3.322	3.322	3.319	3.315	3.310	0.21%
Line Reg.	0.03%	0.06%	0.03%	0.00%	0.03%	

Note: The calculation for load regulation only accounts for the worst case of load variation under the normal voltage condition (i.e., 3.3 V at 3.0 A). All voltages were measured at the PCB header pins.

Table 1–3. Load Regulation and Ripple, 3.3 V (5-V Input)

Load	0 A	0.5 A	1 A	1.5 A	2 A	2.5 A	3 A	5 A	Reg.
Vo(V)	3.323	3.321	3.320	3.319	3.317	3.316	3.315	3.309	0.24%
Vo Ripple (mV P–P)	4	10	10	12	14	16	17	25	
Vo Spikes (mV P–P)	8	12	18	18	25	28	32	37	

Figure 1–5. Efficiency Vs Load Current

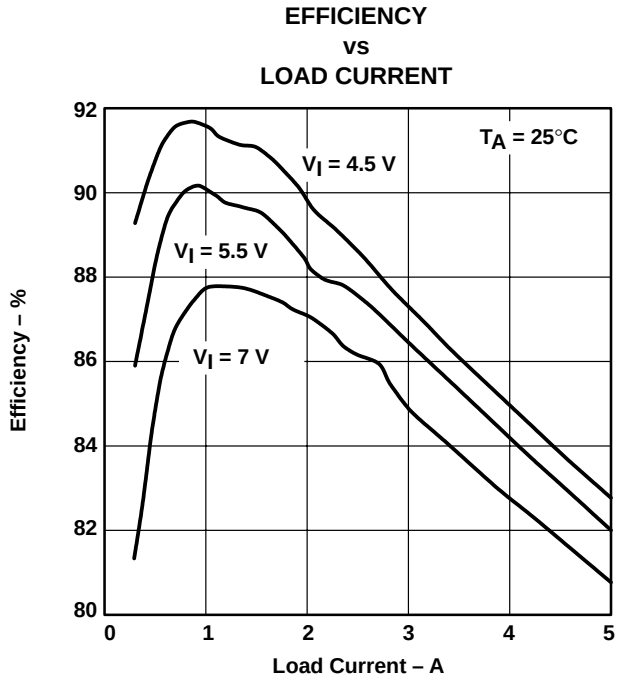


Figure 1–6. Q1 Turn On

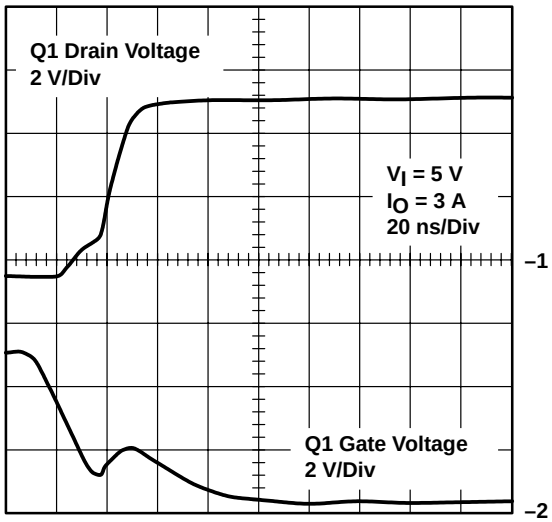


Figure 1–7. Q1 Turn Off

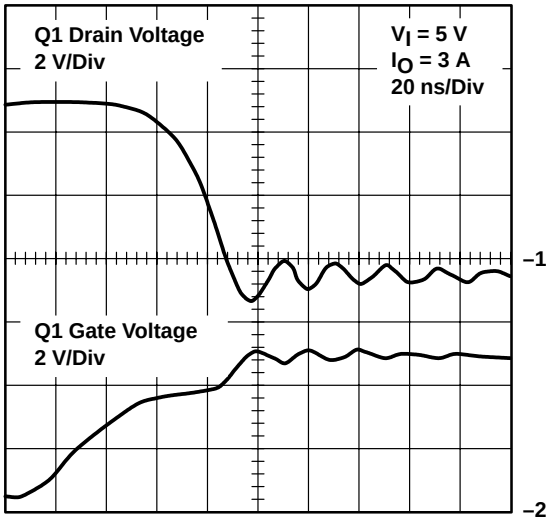


Figure 1–8. Ripple

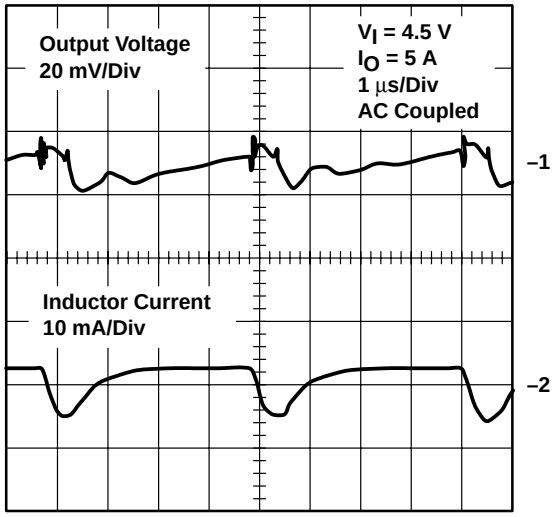
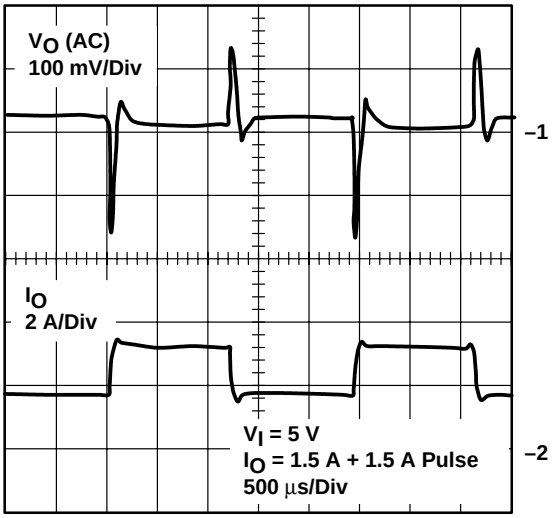


Figure 1–9. Pulse Response



Chapter 2

Design Procedure

There are many possible ways to proceed when designing power supplies. This chapter shows the procedure used in the design of the SLVP087. The chapter includes the following topics:

Topic **Page**

2.1 Introduction

The SLVP087 is a dc-dc buck converter module that provides a 3.3-V output at up to 3 A with an input voltage range of 4.5 V to 7 V. The controller is a TL5001 PWM operating at a nominal frequency of 250 kHz. The TL5001 is configured for a maximum duty cycle of 100 percent and has short-circuit protection built in.

2.2 Operating Specifications

Table 2–1 lists the operating specifications for the SLVP087.

Table 2–1. Operating Specifications

Specification	Min	Typ	Max	Unit
Input Voltage Range	4.5		7	V
Output Voltage Range	3.10	3.30	3.50	V
Output Current Range	0		3	A
Operating Frequency		250		kHz
Output Ripple			50	mV
Line Regulation		0.05%	0.1%	
Load Regulation		0.24%	0.5%	
Lifetime Regulation (including line, load, temperature)		0.5%	1%	
Efficiency	80%	85%		
Ambient Operating Temperature	–20		55	°C
Ambient Storage Temperature	–40		150	°C

2.3 Design Procedures

The application report *Designing With the TL5001C PWM Controller* (literature number SLVA034) from Texas Instruments gives detailed steps in the design of a buck-mode converter. This section shows the basic steps involved in this design.

2.3.1 Duty Cycle Estimate

The duty cycle for a continuous-mode step-down converter is approximately:

$$D = \frac{V_O + V_d}{V_I - V_{SAT}}$$

Assuming that the catch diode forward voltage V_d = 0.12 V and the power switch on-voltage V_{SAT} = 0.25 V, the duty cycle for V_I = 4.5 and 7 V is 0.80 and 0.51, respectively.

2.3.2 Output Filter

A buck converter uses a single-stage low-pass LC filter. Choose an inductor to maintain continuous-mode operation down to 5 percent of the rated output load:

$$\Delta I_O = 2 \times 0.05 \times I_O = 2 \times 0.05 \times 3 = 0.3 \text{ A}$$

The inductor value is:

$$L = \frac{(V_I - V_{SAT} - V_O) \times D \times t}{\Delta I_O}$$

$$= \frac{(7 - 0.25 - 3.3) \times 0.51 \times \left(4 \times 10^{-6}\right)}{0.3} = 23.5 \ \mu\text{H}$$

Inductor ripple current flowing through the output capacitor produces an output voltage ripple component due to too little output capacitance or too much series resistance within the capacitor. Assuming that all inductor ripple current flows through the capacitor, and the effective series resistance (ESR) is zero, the capacitance needed is:

$$C = \frac{\Delta I_O}{8 \times f \times (\Delta V_O)} = \frac{0.3}{8 \times (250 \times 10^3) \times 0.05} = 3 \ \mu\text{F}$$

Assuming the capacitance is very large, the ESR needed to limit the ripple to 50 mV is:

$$\text{ESR} = \frac{\Delta V_O}{\Delta I_O} = \frac{0.05}{0.3} = 0.167 \ \Omega$$

The output filter capacitor should be rated at least ten times the calculated capacitance and 30–50 percent lower than the calculated *ESR*. This design used a 100-μF capacitor in parallel with a multilayer ceramic to reduce *ESR*.

2.3.3 Power Switch

Based on estimates, $r_{DS(ON)}$ should be less than 0.25 V ÷ 3 A = 83 mΩ. The IRF7404 is a 20-V p-channel MOSFET with $r_{DS(ON)}$ = 40 mΩ. Power dissipation (conduction + switching losses) can be estimated as:

$$P_D = \left(I_O^2 \times r_{DS(ON)} \times D\right) + (0.5 \times V_i \times I_O \times t_{r+f} \times f)$$

Assuming total switching time, t_{r+f}, = 150 ns, a 55°C maximum ambient temperature, and $r_{DS(ON)}$ adjustment factor = 1.30, then:

$$P_D = \left[3^2 \times (0.040 \times 1.30) \times 0.80\right] + \left[0.5 \times 4.5 \times 3 \times \left(0.15 \times 10^{-6}\right) \times \left(250 \times 10^3\right)\right] = 0.63 \text{ W}$$

The thermal impedance $R_{\theta JA}$ = 90°C/W for FR-4 with 2-oz. copper and a one-inch-square pattern, thus:

$$T_J = T_A + (R_{\theta JA} \times P_D) = 55 + (90 \times 0.63) = 112°C$$

2.3.4 Commutating Rectifier

The catch rectifier conducts current during the time interval when the power switch is off. The 50WQ03F is a 5-A, 30-V rectifier in a D-Pak power surface-mount package. The power dissipation is:

$$P_D = I_O \times V_D\left(1 - D_{Min}\right) = 3 \times 0.55 \times 0.49 = 0.81 \text{ W}$$

Using a junction-to-ambient thermal resistance of 70°C/W, the maximum junction temperature is:

$$T_J = T_A + (R_{\theta JA} \times P_D) = 55 + (70 \times 0.81) = 112°C$$

2.3.5 Snubber Network

A snubber network is usually needed to suppress the ringing at the node where the power switch drain, output inductor, and the catch rectifier connect. This is usually a trial-and-error sequence of steps to optimize the network with the PC board layout; but as a starting point, select a snubber capacitor with a value that is 4–10 times larger than the estimated capacitance of the catch rectifier. Then, measuring a ringing time constant of 5 ns, *R* is:

$$R1 = \frac{5 \times 10–9}{C} = \frac{5 \times 10^{-9}}{1500 \times 10^{-12}} = 3.3 \ \Omega$$

2.3.6 Controller Functions

The controller functions, oscillator frequency, soft-start, dead-time control, short-circuit protection, and sense-divider network, are discussed in this section.

The oscillator frequency is set by selecting the resistance value from the graph in Figure 6 of the TL5001 data sheet. For 250 kHz, a value of 30.1 kΩ is selected.

Dead-time control provides a minimum off-time for the power switch in each cycle. Set this time by connecting a resistor between DTC and GND. For this design, a maximum duty cycle of 100% is chosen. Then *R*5 is calculated as:

$$R5 \geqq (R4 + 1.25) \times 10^3 \times \left[D\left(V_{O(100\%)} - V_{O(0\%)} \right) + V_{O(0\%)} \right]$$

$$\geqq (30.1 + 1.25) \times 10^3 \times [1(1.35–0.55) + 0.55] = 42.3\ k\Omega \Rightarrow 47\ k\Omega$$

Soft-start is added to reduce power-up transients. This is implemented by adding a capacitor across the dead-time resistor. In this design, a soft-start time of 10 ms is used:

$$C7 = \frac{t_R}{R_{DT}} = \frac{0.010\ s}{47\ k\Omega} = 0.213\ \mu F \Rightarrow 0.22\ \mu F$$

The TL5001 has short circuit protection (SCP) instead of a current sense circuit. If not used the SCP terminal must be connected to ground to allow the converter to start up. If a timing capacitor is connected to SCP, it should have a time constant that is much greater than the soft-start time constant. This time constant is chosen to be 75 ms:

$$C8(\mu F) = 12.46 \times t_{SCP} = 12.46 \times 0.075\ s = 0.93\ \mu F$$

2.3.7 Loop Compensation

Loop compensation is necessary to stabilize the converter over the full range of load, line, and gain conditions. A continuous-mode buck-mode converter has a two-pole LC output filter with a 40-dB-per-decade rolloff. The total closed-loop response needed for stability is a 20-dB-per-decade rolloff, with a minimum phase margin of 30 degrees over the full bandwidth for all conditions. In addition, sufficient bandwidth must be designed into the circuit to assure that the converter has good transient response. Both of these requirements are met by adding compensation components around the error amplifier to modify the total loop response.

The first step in design of the loop compensation network is the design of the output sense divider. This sets the output voltage, and the top resistor determines the relative size of the rest of the compensation design. Since the TL5001 input bias current is 0.5 μA (worst case), the divider current should be at least 0.5 mA. Using a 1-kΩ resistor for the bottom of the divider gives a divider current of 1 mA. The top of the divider is calculated as:

$$R6 = \frac{V_O - 1}{1\ mA} = \frac{(3.3–1)}{0.001} = 2.3\ k\Omega$$

The pulse-width modulator gain can be estimated as the change in output voltage divided by the change in PWM input voltage:

$$A_{PWM} = \frac{\Delta V_O}{\Delta V_{COMP}} = \frac{5.5–0}{1.35–0.55} = 7.86 \Rightarrow 17.9\ dB$$

The LC filter has a double pole at:

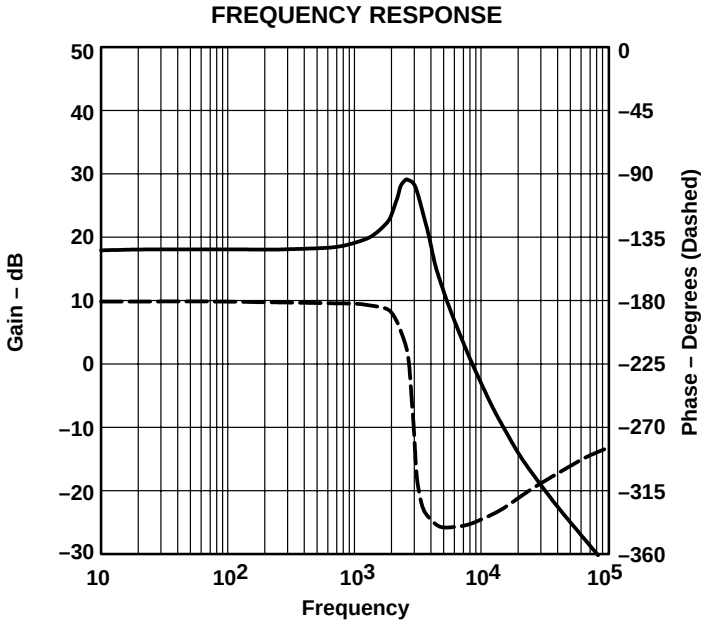
$$\frac{1}{2\pi\sqrt{LC}} = \frac{1}{2\pi\sqrt{27\ \mu h \times 120\ \mu F}} = 2.8\ kHz$$

and rolls off at 40-dB per decade after that until the ESR zero is reached at:

$$\frac{1}{2\pi RC} = \frac{1}{2\pi(0.050)\left(120 \times 10^{-6}\right)} = 26.5 \text{ kHz}$$

This information is enough to calculate the required compensation values. Figure 2–1 shows the power stage gain and phase plots.

Figure 2–1. Power Stage Bode Plot

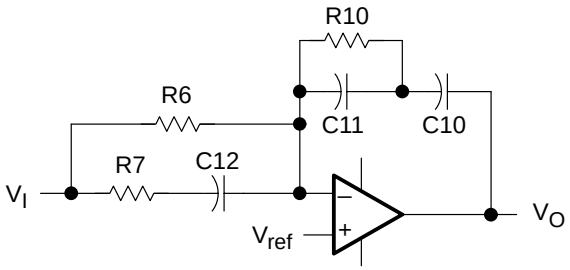


To arrive at the ideal –20-dB-per-decade rolloff, this response must be corrected by addition of the following:

- A pole at zero to give high dc gain
- Two zeroes at approximately 2.8 kHz (used 3 kHz) to cancel the LC poles
- A pole at approximately 27 kHz (used 40 kHz) to cancel the ESR zero
- A final pole to roll off high-frequency gain (used 50 kHz)

The compensation network shown in Figure 2–2 can be used to implement these conditions.

Figure 2–2. Compensation Network



The transfer function for this circuit is:

$$\frac{V_O}{V_I} = \frac{[1 + sR10(C10 + C11)][1 + sC12(R6 + R7)]}{sC10R6(1 + sC11R10)(1 + sC12R7)} = \frac{\left(f_{Z1}\right)\left(f_{Z2}\right)}{\left(f_{P1}\right)\left(f_{P2}\right)\left(f_{P3}\right)}$$

Resistor R6 is already known at 2.32 kΩ. The remaining values are calculated below.

The desired output regulation is ±6 percent total deviation. The PWM controller tolerance is ±5 percent, and the divider resistors are ±1 percent; therefore, the control loop must be very precise. A minimum dc gain of 1000 (60 dB) gives a 0.1 percent tolerance. The integrator (R6, C10) sets the gain of the compensation network. The minimum modulator gain is 18 dB, therefore, the compensation network must have at least 42 dB of gain. With a desired crossover frequency of 20 kHz and a desired slope of 20 dB per decade, choose an integrator frequency of 2 kHz. This gives a gain at 10 Hz of 46 dB, which is sufficient for this application. If more gain is desired, increasing the integrator frequency will accomplish this. Resistor R6 is already known and, assuming that C10 $\gg$ C11, then C10 is calculated as:

$$C10 = \frac{1}{2\pi(f_{PI})(R6)} = \frac{1}{2\pi(2\ \text{kHz})(2.32\ \text{k}\Omega)} = 0.034\ \mu\text{F} \Rightarrow 0.033\ \mu\text{F}$$

Setting f_{Z2} = 3 kHz to compensate for one of the LC poles, and assuming that R6 $\gg$ R7, gives:

$$C12 = \frac{1}{2\pi(f_{Z2})(R6)} = \frac{1}{2\pi(3\ \text{kHz})(2.32\ \text{k}\Omega)} = 0.023\ \mu\text{F} \Rightarrow 0.022\ \mu\text{F}$$

Now R7 can be calculated using f_{P3} (40 kHz), the ESR compensating zero:

$$R7 = \frac{1}{2\pi(f_{P3})(C12)} = \frac{1}{2\pi(40\ \text{kHz})(0.022\ \mu\text{F})} = 181\ \Omega \Rightarrow 180\ \Omega$$

The other LC filter compensating zero uses R10 and C10 (again assuming C10 $\gg$ C11):

$$R10 = \frac{1}{2\pi(f_{Z1})(C10)} = \frac{1}{2\pi(3\ \text{kHz})(0.0033\ \mu\text{F})} = 1.6\ \text{k}\Omega$$

The final rolloff pole (selected at 50 kHz) uses C11 and R10:

$$C11 = \frac{1}{2\pi(f_{P2})(R10)} = \frac{1}{2\pi(50\ \text{kHz})(1.6\ \text{k}\Omega)} = 0.002\ \mu\text{F} \Rightarrow 0.022\ \mu\text{F}$$

Figure 2–3 shows the bode plot for the compensation network.

Figure 2–3. Compensation Network Response

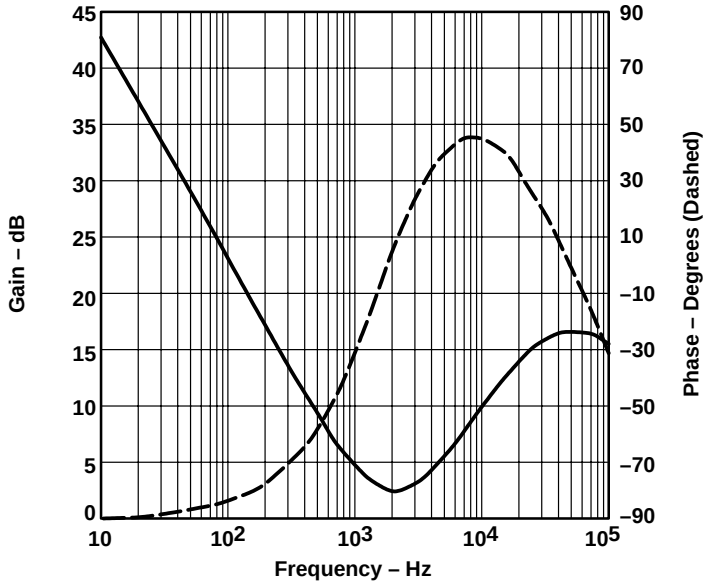


Figure 2–4 shows the output response. Note that the minimum phase margin is 60 degrees and the bandwidth is 17 kHz under nominal operating conditions.

Figure 2–4. Output Response