

Evaluation Module for TPS62737 Ultra Low Power Buck Converter

This user's guide describes the TPS62737 evaluation module (EVM). The TPS62737 device is a high-frequency synchronous stepdown dc-dc converter optimized for ultralow-power energy harvesting applications. The converter can provide up to 2900 mA of continuous current to a 1.3- to 5.3-V output from input voltages up to 5.5 V.

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1 Introduction

1.1 TPS62737 IC Features

The TPS62737 is a highly integrated ultra low power buck converter solution that is well suited for meeting the special needs of ultra low power applications such as energy harvesting. The TPS62737 provides the system with an externally programmable regulated supply in order to preserve the overall efficiency of the power management stage versus a linear step down converter. Although intended to have input power from an energy storage element such as a Li-Ion battery or super cap, the TPS62737 can accept any input voltage up to 5.5 V, while supplying the rail to low voltage electronics.

The TPS62737 integrates an optimized hysteretic controller for low power applications. The internal circuitry utilizes a time based sampling system in order to reduce the average quiescent current. This allows for the quiescent current consumption to scale with output load levels. The regulated output has been optimized to provide high efficiency across low output currents ($< 10 \mu\text{A}$) to high currents (200 mA).

To further assist users in the strict management of their energy budgets, the TPS62737 toggles the input good (VIN_OK) flag to signal an attached microprocessor when the voltage on the input supply has dropped below a pre-set critical level. The intent of VIN_OK is to trigger the reduction of load currents to prevent the system from entering an undervoltage condition. Two separate enable signals allow the user to enable/disable the regulated output or place IC into an ultra-low quiescent sleep state. Two separate enable signals allow the enabling or disabling of the regulated output or allow putting the IC into an ultra-low quiescent sleep state.

The output voltage regulation point and input good threshold are set by external resistors. **In order to maximize efficiency at light load, the use of voltage level setting resistors $> 1 \text{ M}\Omega$ is recommended. However, during board assembly or modification, contaminants such as solder flux and even some board cleaning agents can leave residue that may form parasitic resistors across the physical resistors and/or from one end of a resistor to ground, especially in humid, fast airflow environments. This can result in the voltage regulation and threshold levels changing significantly from those expected per the installed resistor values. Therefore, the boards must be carefully cleaned then rinsed with de-ionized water until the ionic contamination of that water. If this is not feasible, then it is recommended that the sum of the voltage setting resistors be reduced.**

1.2 TPS62737EVM Features

1. Input voltage range from 2.0 V to 5.5 V
2. Output voltage set to 1.8 V but adjustable from 1.3 V to 5.3 V with external resistors
3. VIN_OK threshold of 2.9 V but adjustable from VOUT to 5.3 V with external resistors
4. Easily accessible headers for IN, IN-SENSE, OUT, OUT-SENSE, GND, VIN_OK
5. Jumpers for EN1 and EN2

1.3 TPS62737EVM Schematic

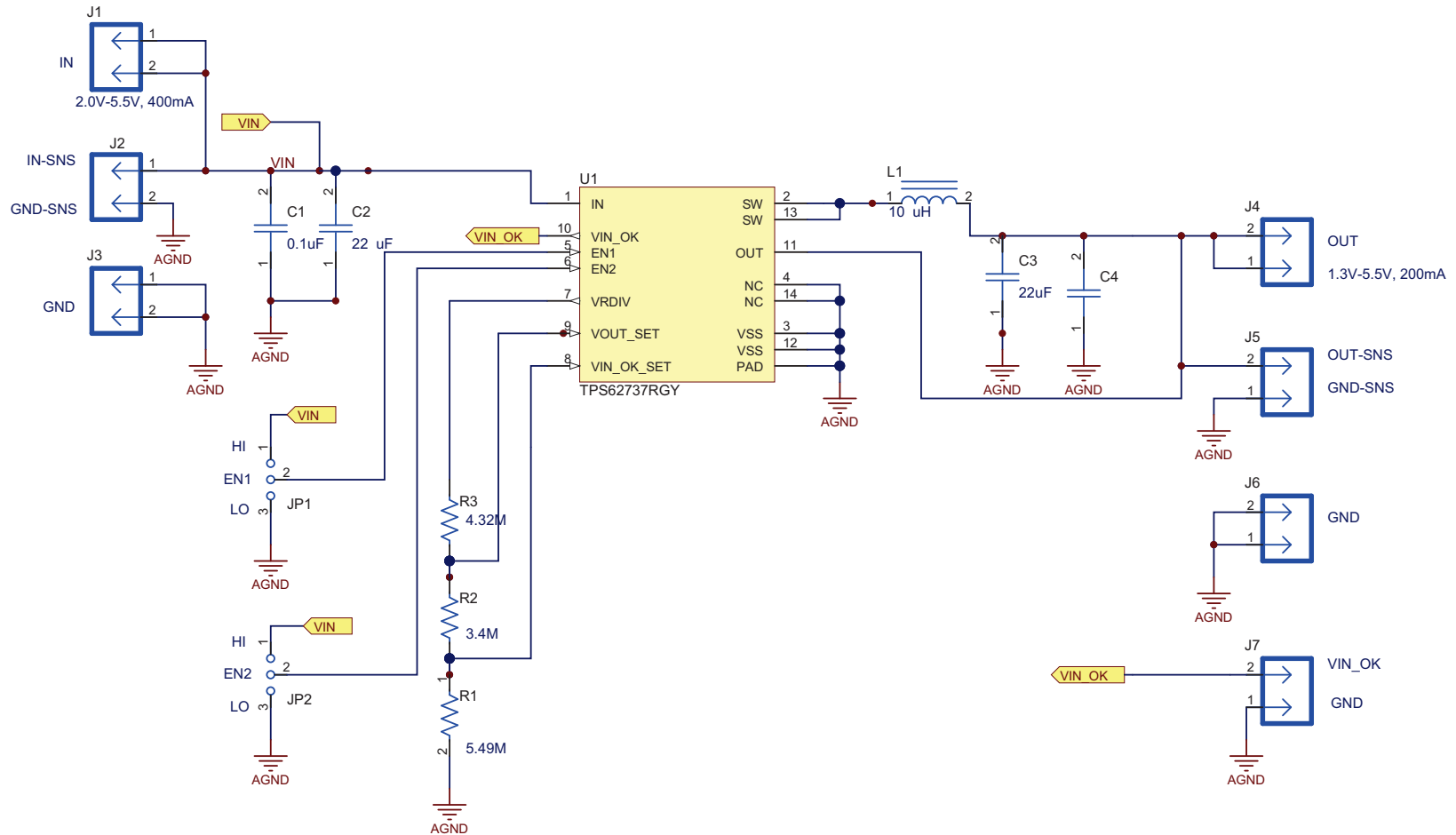


Figure 1. TPS62737 EVM Board Schematic

2 Performance Specification Summary

Specification	Conditions	MIN	TYP	MAX	UNIT
Input dc voltage, IN		2.0		5.5	V
Output dc voltage, OUT	Adjustable by changing external resistors from 1.3 V to 5.3 V		1.8		V
VBAT_OK threshold	Adjustable by changing external resistors from OUT to 5.3 V		2.9		V
Output current		0		200	mA

3 Test Summary

3.1 Recommended Equipment

- Adjustable dc power supply between 2.0 V and 5.5 V with the adjustable current limit set to approximately 400 mA
- Load: system load or resistive load $\geq 9 \Omega$
- Two digital multimeters configured to measure voltage (equivalent or better)
- Two digital multimeters configured to measure current (equivalent or better). **NOTE:** Due to the input current pulses inherent to a hysteretically-controlled converter, the input current meter must be capable of filtering and/or averaging in order to measure the correct value. Adding a large ($> 100 \mu\text{F}$) capacitor between IN and GND may be used to assist with filtering; however, such capacitors tend to have high leakage currents that may artificially increase quiescent current measurements at no load. Use of a sourcemeter, configured to regulate voltage and measure current, or power, or both current and power is also recommended when taking efficiency measurements.
- Oscilloscope with up to four voltage probes

3.2 Equipment and EVM Setup

Table 1. Setup I/O Connections and Configuration for Measuring Efficiency of TPS62737 EVM

Jack and Component (Silk Screen)	Description	Connect or Adjustment To:
J1 (IN)		Negative lead of current meter (CM#1)
J2-1 (+ IN SNS)	Kelvin connection to capacitance	Positive lead of voltmeter (VM#1)
J2-2 (- GND SNS)	Kelvin connection to capacitance	Negative lead of voltmeter (VM#1)
J3 (GND)		Power supply negative lead
J4 (OUT)		Positive lead of current meter (CM#2)
J5-1 (+ OUT SNS)	Kelvin connection to capacitance	Positive lead of voltmeter (VM#2)
J5-2 (- GND SNS)	Kelvin connection to capacitance	Negative lead of voltmeter (VM#2)
J6 (GND)		Negative lead to load resistance
J7-1 (VIN_OK)	Push-pull output of comparator that indicates the status of the input voltage	n/a
J7-2 (GND)		n/a
JP1 (EN1)	EN1 = HI and EN2 = x implements full standby mode. Switching converter and VIN_OK indication is off (ship mode).	EN1 = LO
JP2 (EN2)	EN1 = LO and EN2 = HI implements full buck converter mode. EN1 = LO and EN2 = LO implements partial standby mode. Switching converter is off, but VIN_OK indication is on.	EN2 = HI

Table 1 and Figure 2 show the test setup for measuring efficiency.

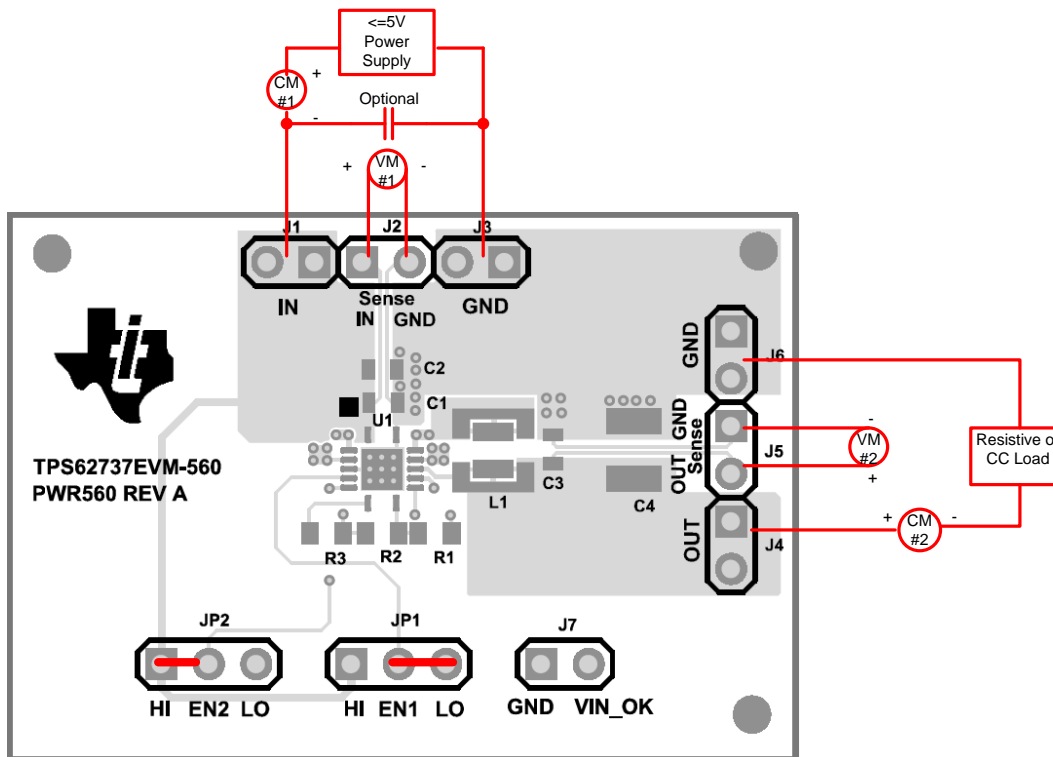


Figure 2. EVM Test Setup for Measuring Efficiency

3.3 Tips when Measuring Efficiency

1. Ensure that the EVM setup is according to Table 1 and Figure 2, and preset the power supply to a voltage less than 5.5 V at a current limit of approximately 400 mA.
2. Slowly increase the system load current until 200 mA is reached.
3. The TPS62737 datasheet has efficiency plots at various input voltages, output voltages and load currents.

3.4 Tips for Taking Scope Plots

1. A current loop was inserted in series with the inductor for taking the inductor current measurements.
2. If measuring DC waveforms, set the timebase as shown in the plot and connect the probes to the applicable headers (IN, OUT, VBAT_OK) or SW pin and the closest GND header.
3. If measuring AC waveforms such as output voltage ripple, set the timebase as shown in the plot, remove the voltage probe hat, connect the probe tip to the top of capacitor C3 and a short ground lead to capacitor C3's ground.
4. Please note that when measuring switching waveforms, the timebase may need to be adjusted as the output load current adjusts due to the hysteretic control methodology.

3.5 Test Results

Figure 3 through Figure 6 detail various test results for the EVM.

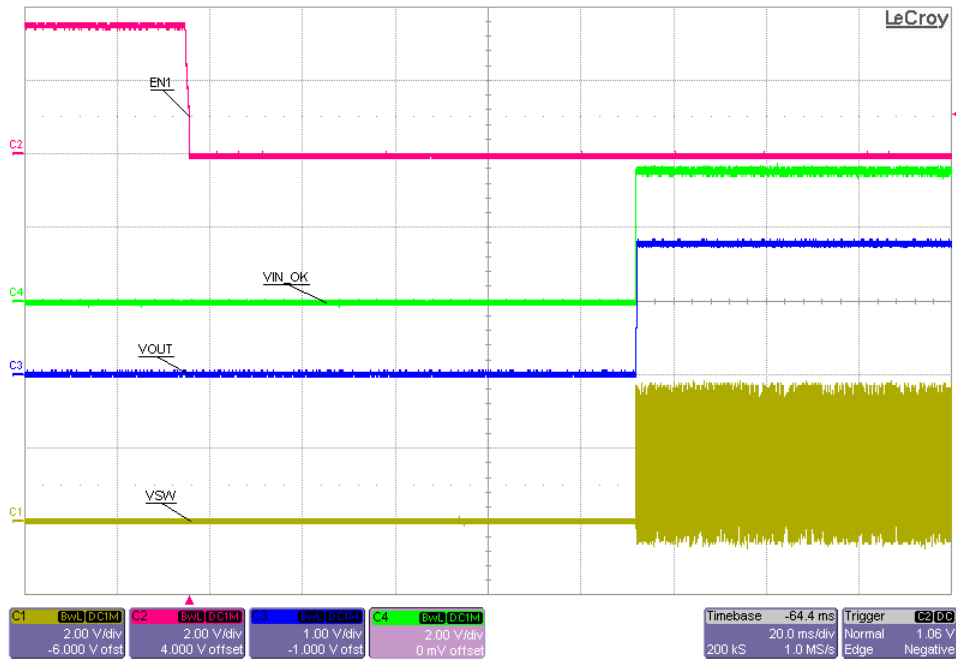


Figure 3. Ship-Mode Startup Behavior, $V_{IN} = 3.6V$, $V_{OUT} = 1.8V$

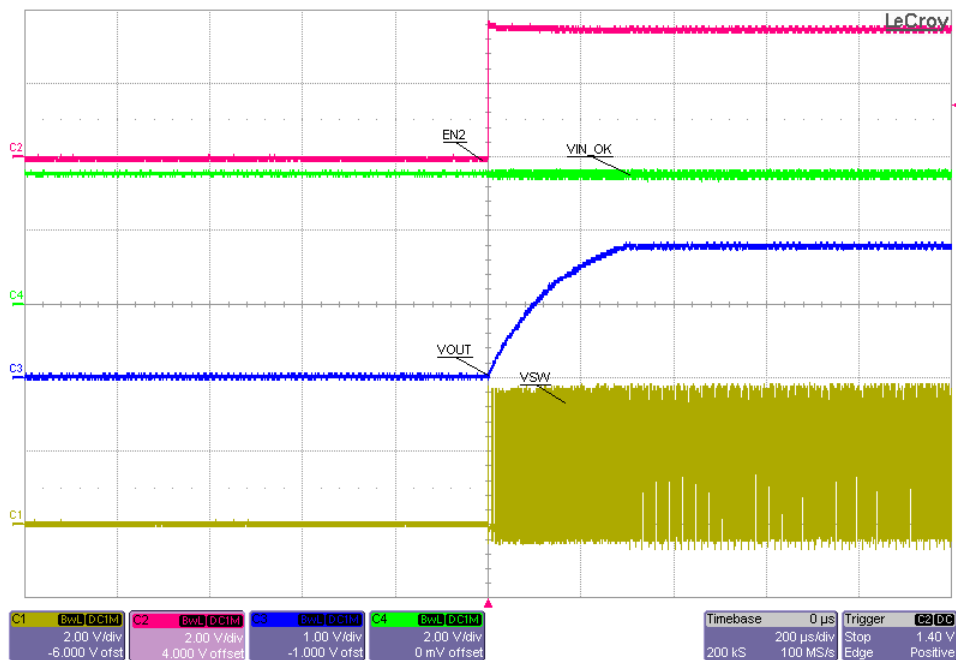


Figure 4. Standby Mode Startup Behavior, $V_{IN} = 3.6V$, $V_{OUT} = 1.8V$

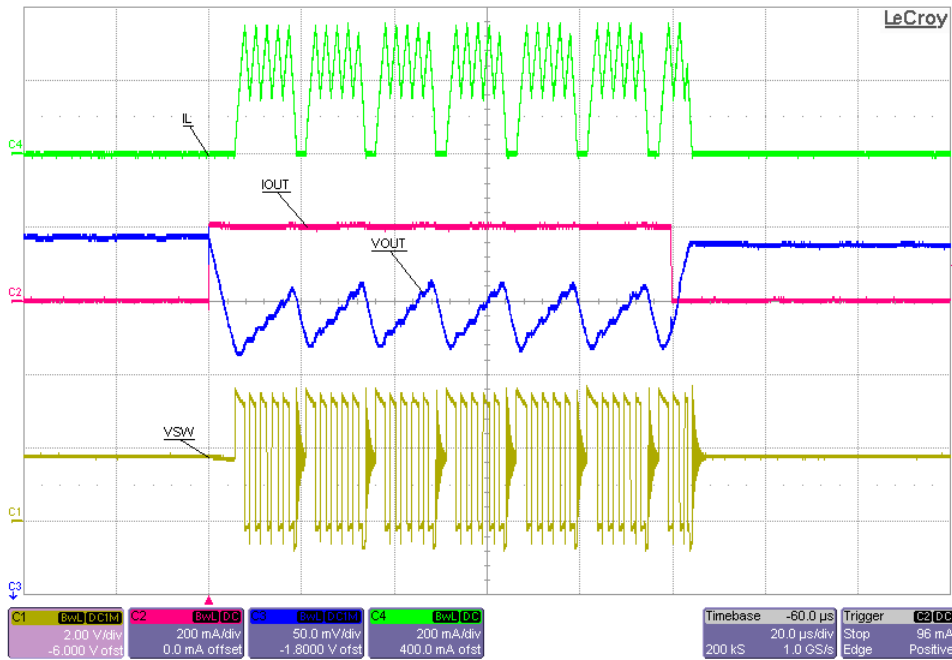


Figure 5. Load Transient Response, $V_{IN} = 3.6\text{ V}$, $V_{OUT}=1.8\text{V}$

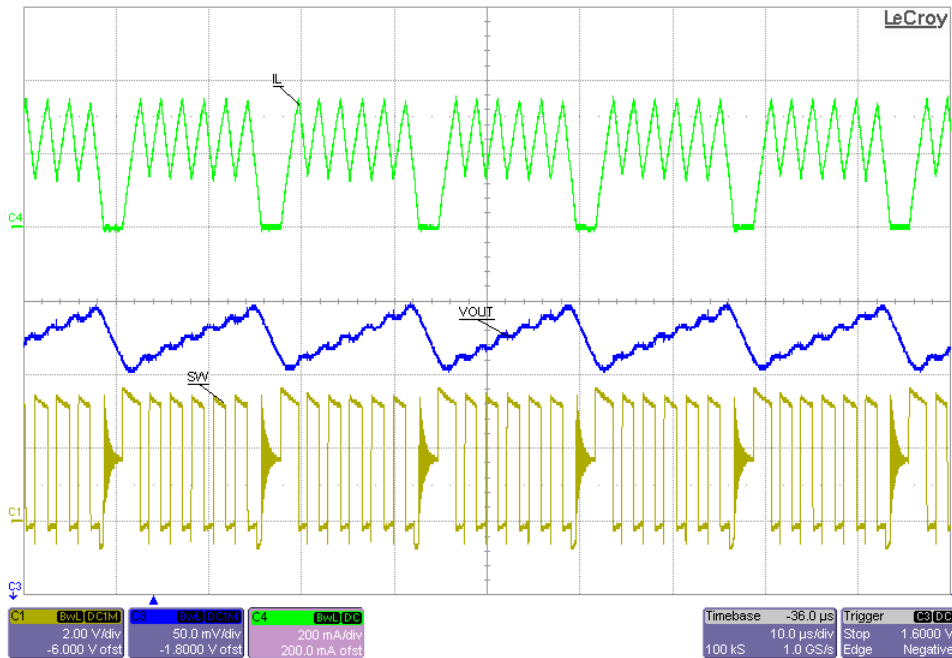


Figure 6. Steady State Operation, $V_{IN} = 3.6\text{V}$, $V_{OUT} = 1.8\text{V}$, $R_{OUT}= 9\ \Omega$

4 PWR560 PCB Layout and Bill of Materials

4.1 REV A PCB Layout

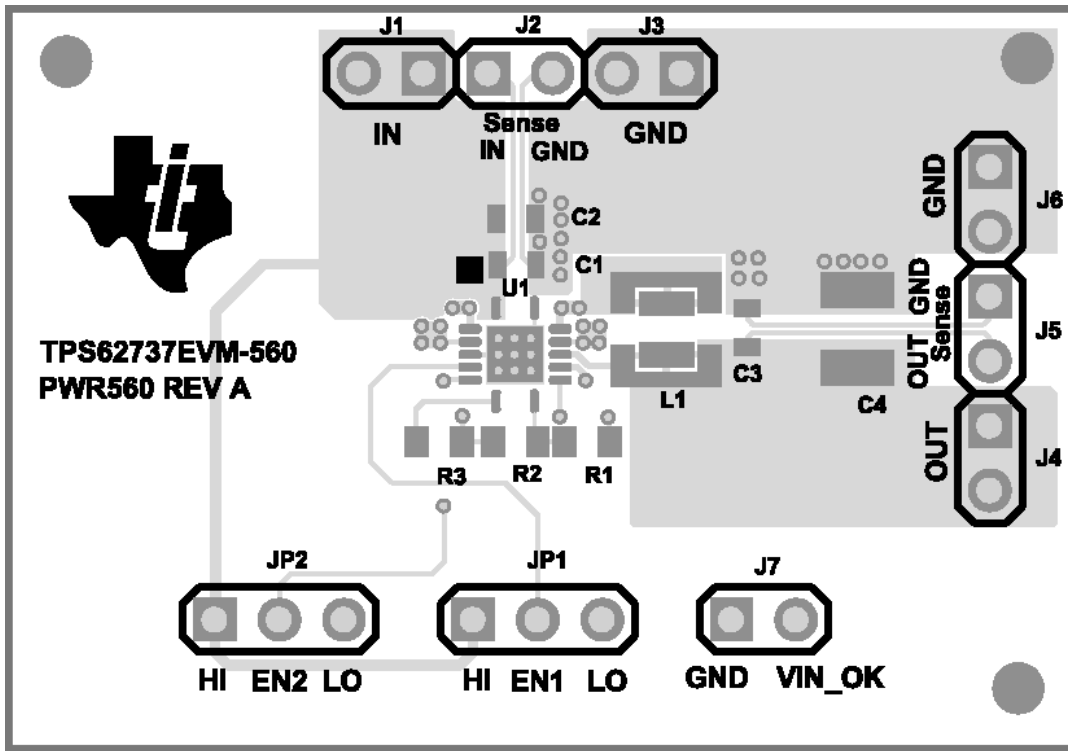


Figure 7. Top Layer

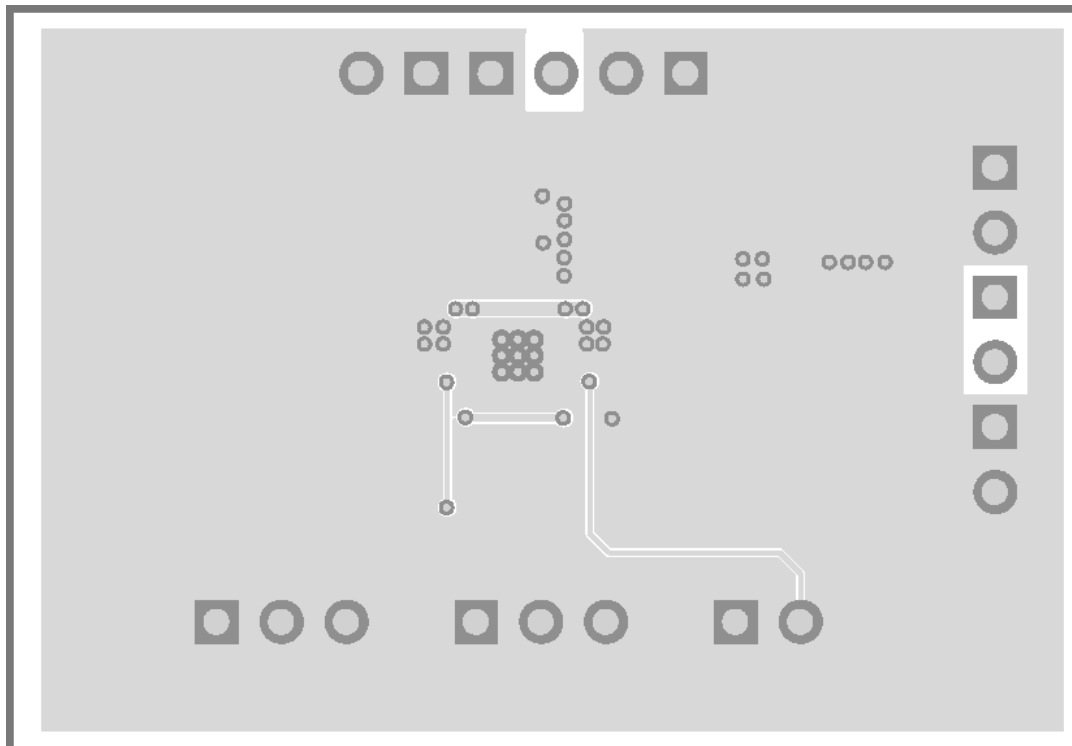


Figure 8. Bottom Layer

4.2 Bill of Materials

Table 2 lists the BOM for this EVM.

Table 2. PWR560 Bill of Materials

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer
PCB	1		Printed Circuit Board		PWR560	Any
C1	1	0.1uF	Capacitor, Ceramic Chip, 10 V, X7R, ±10%	603	C0603C104K8RACTU	Kemet
C2	1	22 uF	Capacitor, Ceramic Chip, 10 V, X5R, ±10%	603	C1608X5R1A226M080AC	TDK
C3	1	22uF	Capacitor, Ceramic Chip, 10 V, X5R, ±10%	603	C1608X5R1A226M080AC	TDK
C4	0	Open	Capacitor, Ceramic Chip, xxV, ±10%	1210	Std	STD
J1, J2, J3, J4, J5, J6, J7	7	PEC02SAAN	Header, Male 2-pin, 100mil spacing,	0.100 inch x 2	PEC02SAAN	Sullins
JP1, JP2	2	PEC03SAAN	Header, Male 3-pin, 100mil spacing,	0.100 inch x 3	PEC03SAAN	Sullins
L1	1	10 uH	Inductor, SMT, 1.4A, 216mΩ Inductor SMT, 500mA, 500mΩ Inductor SMT, 500mA, 390mΩ	2.5mm x 2.0mm x 1.20mm 2.5mm x 2.0mm x 1.20mm 2.8mm x 2.8mm x 1.35mm	DFE252012C-1239AS-H-100M 74479889310 744029100	Toko Würth Elektronik Würth Elektronik
R1	1	5.49M	Resistor, Chip, 1/16W, 1%	603	CRCW06033M40FKEA	Vishay
R2	1	3.4M	Resistor, Chip, 1/16W, 1%	603	CRCW06033M40FKEA	Vishay
R3	1	4.32M	Resistor, Chip, 1/16W, 1%	603	CRCW06034M32FKEA	Vishay
U1	1		Programmable Output Voltage Ultra-Low Power Buck Converter with up to 50mA / 200 mA Output Current, RGY0014A	RGY0014A	TPS62737RGY	Texas Instruments

Revision History

Changes from Original (July 2013) to A Revision	Page
• Changed bill of materials.	9

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Industry Canada Compliance (English)

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Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

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If user uses EVMs in Japan, user is required by Radio Law of Japan to follow the instructions below with respect to EVMs:

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after user obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after user obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless user gives the same notice above to the transferee. Please note that if user does not follow the instructions above, user will be subject to penalties of Radio Law of Japan.

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東京都新宿区西新宿 6 丁目 2 4 番 1 号

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<http://www.tij.co.jp>

Texas Instruments Japan Limited

(address) 24-1, Nishi-Shinjuku 6 chome, Shinjuku-ku, Tokyo, Japan

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