*User's Guide*

# *TPS54336A Step-Down Converter Evaluation Module User's Guide*


**ABSTRACT**

This user's guide contains background information for the TPS54336A as well as support documentation for the TPS54336AEVM-010 evaluation module (BSR010-002). The user's guide also includes performance specifications, the schematic, and the bill of materials for the TPS54336AEVM-010.


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# 1 Introduction

This user's guide contains background information for the TPS54336A as well as support documentation for the TPS54336AEVM-010 evaluation module (BSR010-002). Also included are the performance specifications, the schematic, and the bill of materials for the TPS54336AEVM-010.

## 1.1 Background

The TPS54336A dc/dc converter is designed to provide up to a 3-A output from an input voltage source of 4.5 V to 28 V. Rated input voltage and output current range for the evaluation module are given in Table 1-1. This evaluation module is designed to demonstrate the small printed-circuit-board areas that may be achieved when designing with the TPS54336A regulator. The switching frequency is internally set at a nominal 340 kHz. The high-side and low-side MOSFETs are incorporated inside the TPS54336A package along with the gate-drive circuitry. The low drain-to-source on resistance of the MOSFETs allow the TPS54336A to achieve high efficiencies and helps keep the junction temperature low at high output currents. The compensation components are external to the integrated circuit (IC), and an external divider allows for an adjustable output voltage. Additionally, the TPS54336A provides adjustable slow start and undervoltage lockout inputs. The absolute maximum input voltage is 30 V for the TPS54336AEVM-010.

**Table 1-1. Input Voltage and Output Current Summary**

| EVM | INPUT VOLTAGE RANGE | OUTPUT CURRENT RANGE |
|---|---|---|
| TPS54336AEVM-010 | VIN = 8 V to 28 V | 0 A to 3 A |

## 1.2 Performance Specification Summary

A summary of the TPS54336AEVM-010 performance specifications is provided in Table 1-2. Specifications are given for an input voltage of $V_{IN}$ = 24 V and an output voltage of 5.0 V, unless otherwise specified. The TPS54336AEVM-010 is designed and tested for $V_{IN}$ = 8 V to 28 V. The ambient temperature is 25°C for all measurements, unless otherwise noted.

**Table 1-2. TPS54336AEVM-010 Performance Specification Summary**

| SPECIFICATION | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IN}$ operating voltage range | | | 8 | 24 | 28 | V |
| $V_{IN}$ start voltage | | | | 7.12 | | V |
| $V_{IN}$ stop voltage | | | | 6.12 | | V |
| Output voltage set point | | | | 5 | | V |
| Output current range | $V_{IN}$ = 8 V to 28 V | | 0 | | 3 | A |
| Line regulation | $I_O$ = 1.5 A, $V_{IN}$ = 8 V to 28 V | | | ±0.05% | | |
| Load regulation | $V_{IN}$ = 24 V, $I_O$ = 0 A to 3 A | | | ±0.3% | | |
| Load transient response | $I_O$ = 0.75 A to 2.25 A | Voltage change | | –190 | | mV |
| | | Recovery time | | 150 | | µs |
| | $I_O$ = 2.25 A to 0.75 A | Voltage change | | 190 | | mV |
| | | Recovery time | | 150 | | µs |
| Loop bandwidth | $V_{IN}$ = 24 V, $I_O$ = 1.5 A | | | 31.6 | | kHz |
| Phase margin | $V_{IN}$ = 24 V , $I_O$ = 1.5 A | | | 55 | | ° |
| Input ripple voltage | $I_O$ = 3 A | | | 400 | | $mV_{PP}$ |
| Output ripple voltage | $I_O$ = 3 A | | | <30 | | $mV_{PP}$ |
| Output rise time | | | | 3.47 | | ms |
| Operating frequency | | | | 340 | | kHz |
| Maximum efficiency | TPS54336AEVM-010, $V_{IN}$ = 8 V, $I_O$ = 0.7 A | | | 96.5% | | |

## 1.3 Modifications

These evaluation modules are designed to provide access to the features of the TPS54336A. Some modifications can be made to this module.

### 1.3.1 Output Voltage Set Point

The voltage divider, R7 and R8, is used to set the output voltage. To change the output voltage of the EVM, it is necessary to change the value of resistor R8. Changing the value of R8 can change the output voltage above 0.8 V. The value of R8 for a specific output voltage can be calculated using Equation 1. Use 100 kΩ for R7.

$$R8 = \frac{R7 \times 0.8\ V}{V_{OUT} - 0.8V} \tag{1}$$

Table 1-3 lists the R9 and R10 values for some common output voltages. Note that $V_{IN}$ must be in a range so that the minimum on-time is greater than 145 ns, and the maximum duty cycle is less than 100%. The values given in Table 1-3 are standard values, not the exact value calculated using Equation 1.

**Table 1-3. Output Voltages Available**

| OUTPUT VOLTAGE (V) | R7 VALUE (kΩ) | R8 VALUE (kΩ) |
|---|---|---|
| 1.2 | 100 | 200 |
| 1.8 | 100 | 80.6 |
| 2.5 | 100 | 47.5 |
| 3.3 | 100 | 32.4 |
| 5.0 | 100 | 19.1 |

### 1.3.2 Adjustable UVLO

The under voltage lock out (UVLO) can be adjusted externally using R1 and R2. The EVM is set for a start voltage of 7.12 V and a stop voltage of 6.12 V using R1 = 220 kΩ and R2 = 43.2 kΩ. Use Equation 2 and Equation 3 to calculate required resistor values for different start and stop voltages.

$$R1 = \frac{V_{START}\left(\frac{V_{ENFALLING}}{V_{ENRISING}}\right) - V_{STOP}}{I_p\left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}}\right) + I_h} \tag{2}$$

$$R2 = \frac{R1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R1\left(I_p + I_h\right)} \tag{3}$$

$I_p$ = 1.15 µA, $I_h$ = 3.3 µA, $V_{ENFALLING}$ = 1.17 V and $V_{ENRISING}$ = 1.21 V

### 1.3.3 Adjustable Slow Start

The TPS54336A has an adjustable slow start function. The slow start time can be adjusted with C3, using Equation 4

$$C3(nF) = \frac{T_{SS}(msec) \times I_{SS}(\mu A)}{V_{REF}(V)} \tag{4}$$

$I_{SS}$ = 2.3 µA, $V_{REF}$ = 0.8 V.

# 2 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS54336AEVM-010 evaluation module. The section also includes test results typical for the evaluation module and covers the following:

- Efficiency
- Output voltage regulation
- Load transients
- Loop response
- Output ripple
- Input ripple
- Start-up

## 2.1 Input/Output Connections

The TPS54336AEVM-010 is provided with input/output connectors and test points as shown in Table 2-1. A power supply capable of supplying 2 A must be connected to J1 through a pair of 20-AWG wires. The load must be connected to J4 through a pair of 20-AWG wires. The maximum load current capability must be at least 4 A to use the full capability of this EVM. Wire lengths must be minimized to reduce losses in the wires. Test-point TP1 provides a place to monitor the $V_{IN}$ input voltages with TP2 providing a convenient ground reference. TP6 is used to monitor the output voltage with TP7 as the ground reference.

**Table 2-1. EVM Connectors and Test Points**

| REFERENCE DESIGNATOR | FUNCTION |
|---|---|
| J1 | $V_{IN}$ (see Table 1-1 for $V_{IN}$ range) |
| J2 | $V_{OUT}$, 5 V at 3-A maximum |
| JP1 | 2-pin header for enable. Connect EN to ground to disable, open to enable. |
| TP1 | $V_{IN}$ test point at $V_{IN}$ connector |
| TP2 | GND test point at $V_{IN}$ |
| TP3 | Slow-start monitor test point for TPS54336A |
| TP4 | PH test point |
| TP5 | Test point between voltage divider network and output. Used for loop response measurements |
| TP6 | Output voltage test point at OUT connector |
| TP7 | GND test point at OUT connector |

## 2.2 Efficiency

The efficiency of this EVM peaks at a load current of about 0.5 A – 1 A, and then decreases as the load current increases towards full load. Figure 2-1 shows the efficiency for the TPS54336AEVM-010 at an ambient temperature of 25°C.

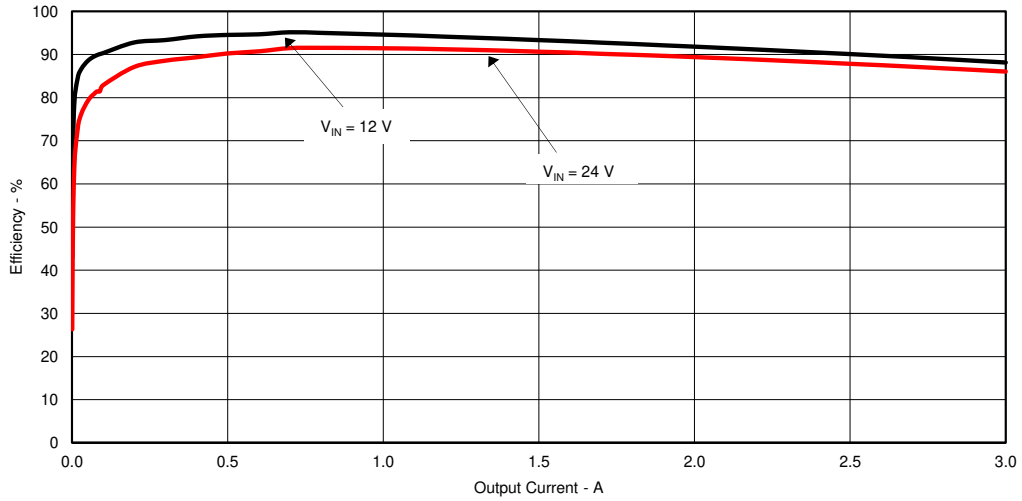


**Figure 2-1. TPS54336AEVM-010 Efficiency**

Figure 2-2 shows the efficiency for the TPS54336AEVM-010 on a semi-log scale to better show light load efficiency. The ambient temperature is 25°C.

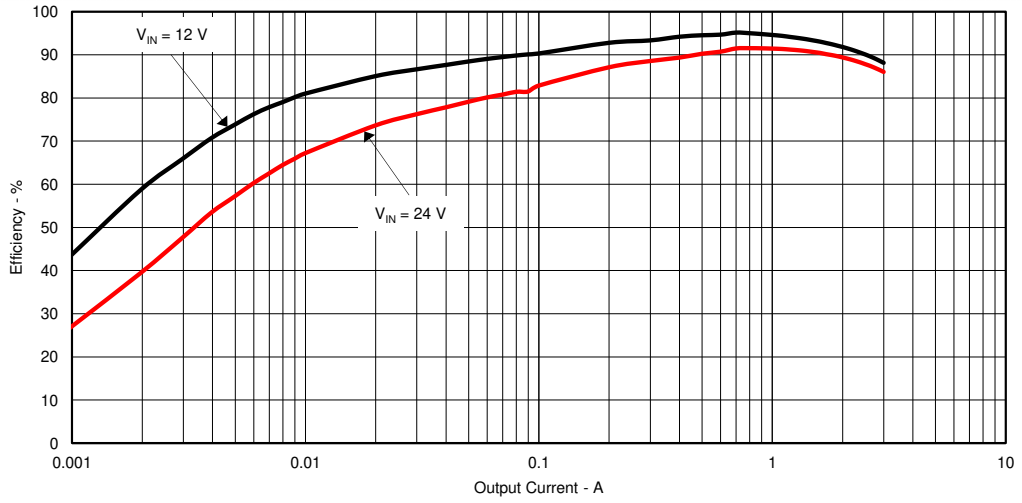


**Figure 2-2. TPS54336AEVM-010 Low Current Efficiency**

The efficiency may be lower at higher ambient temperatures, due to temperature variation in the drain-to-source resistance of the internal MOSFET.

## 2.3 Output Voltage Load Regulation

Figure 2-3 shows the load regulation for the TPS54336AEVM-010.

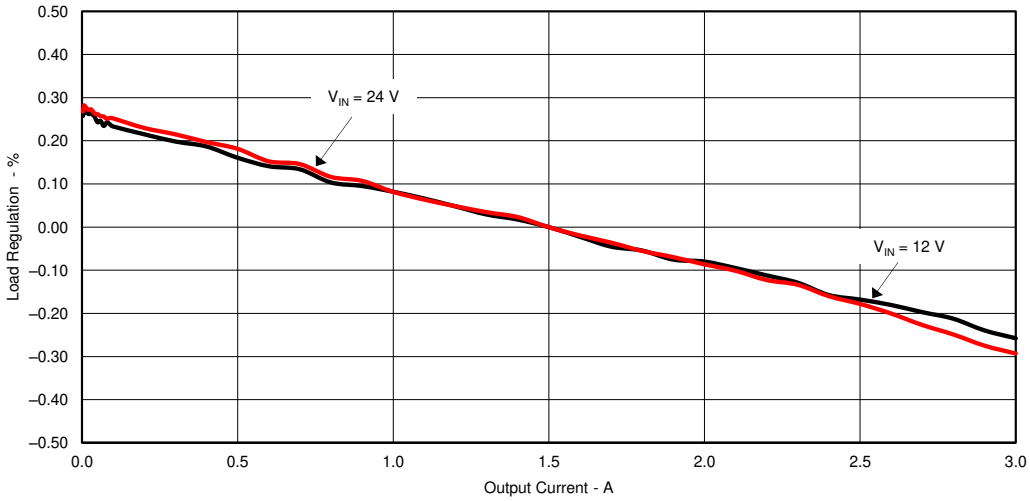


**Figure 2-3. TPS54336AEVM-010 Load Regulation**

Measurements are given for an ambient temperature of 25°C.

## 2.4 Output Voltage Line Regulation

Figure 2-4 shows the line regulation for the TPS54336AEVM-010.

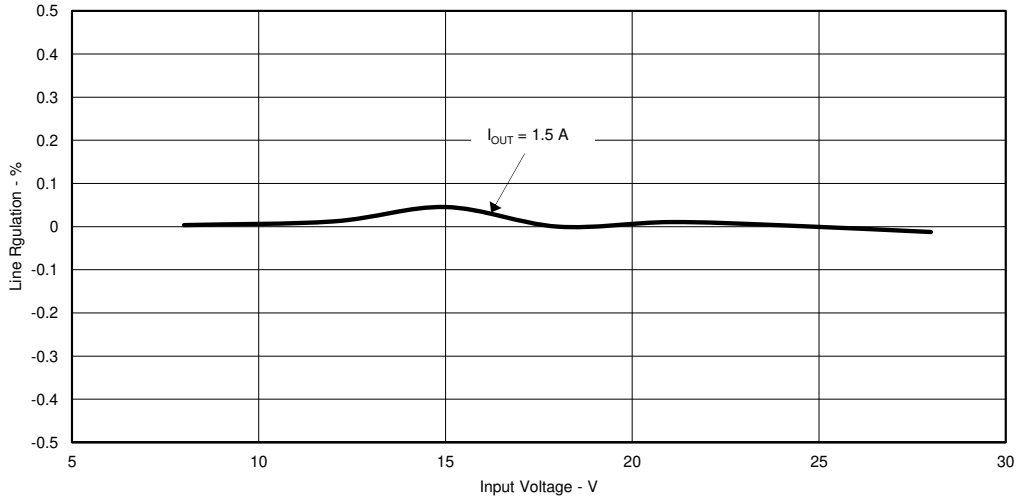


**Figure 2-4. TPS54336AEVM-010 Line Regulation**

## 2.5 Load Transients

Figure 2-5 shows the TPS54336AEVM-010 response to load transients. The current step is from 25% to 75% of maximum rated load at 24-V input. Total peak-to-peak voltage variation is as shown, including ripple and noise on the output.

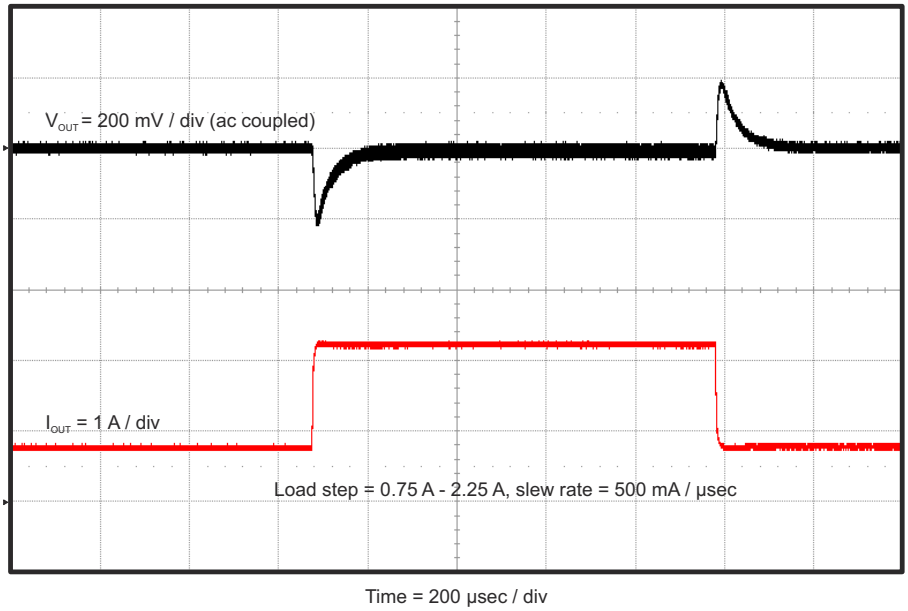


**Figure 2-5. TPS54336AEVM-010 Transient Response**

## 2.6 Loop Characteristics

Figure 2-6 shows the TPS54336AEVM-010 loop-response characteristics. Gain and phase plots are shown for $V_{IN}$ voltage of 24 V. Load current for the measurement is 1.5 A.

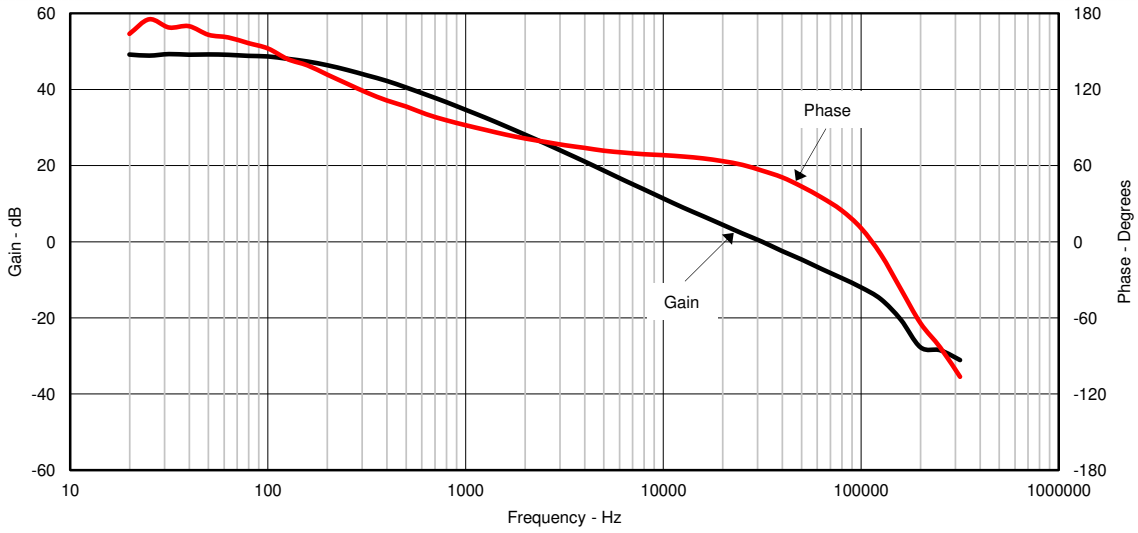


**Figure 2-6. TPS54336AEVM-010 Loop Response**

## 2.7 Output Voltage Ripple

Figure 2-7, Figure 2-8, and Figure 2-9 show the TPS54336AEVM-010 output voltage ripple for full load, light load, and skip mode operation. $V_{IN}$ = 24 V. The output The ripple voltage is measured directly across the output capacitors.

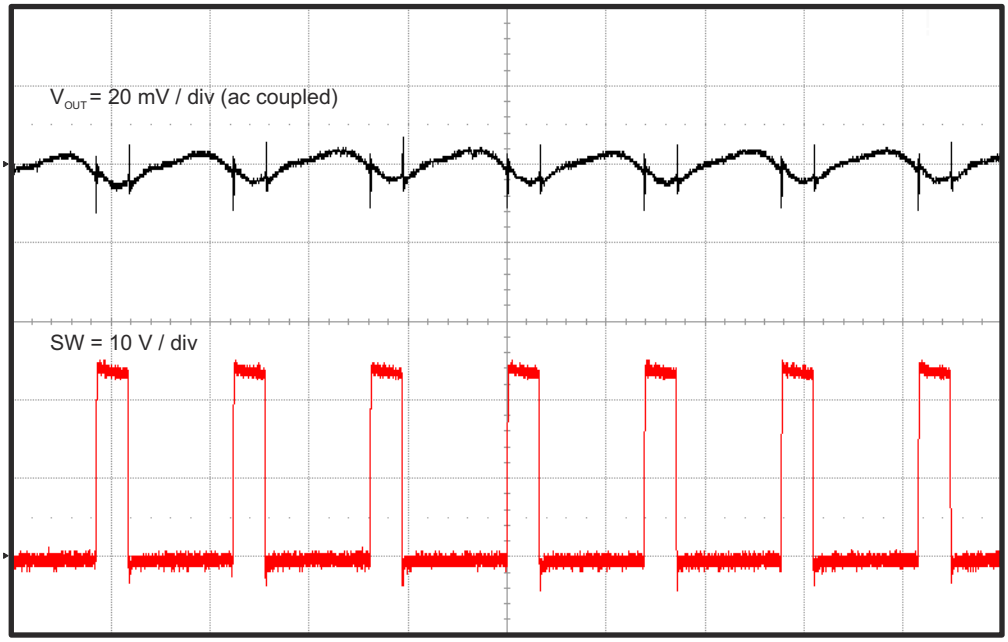


**Figure 2-7. TPS54336AEVM-010 Output Ripple, $I_{OUT}$ = 3 A**

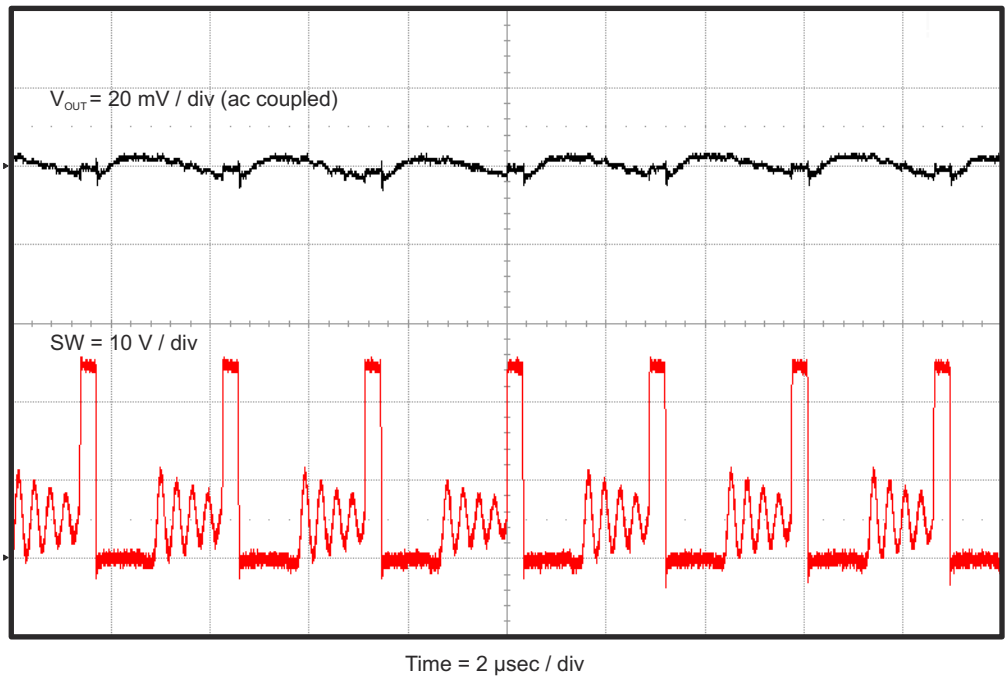


**Figure 2-8. TPS54336AEVM-010 Output Ripple, $I_{OUT}$ = 100 mA**

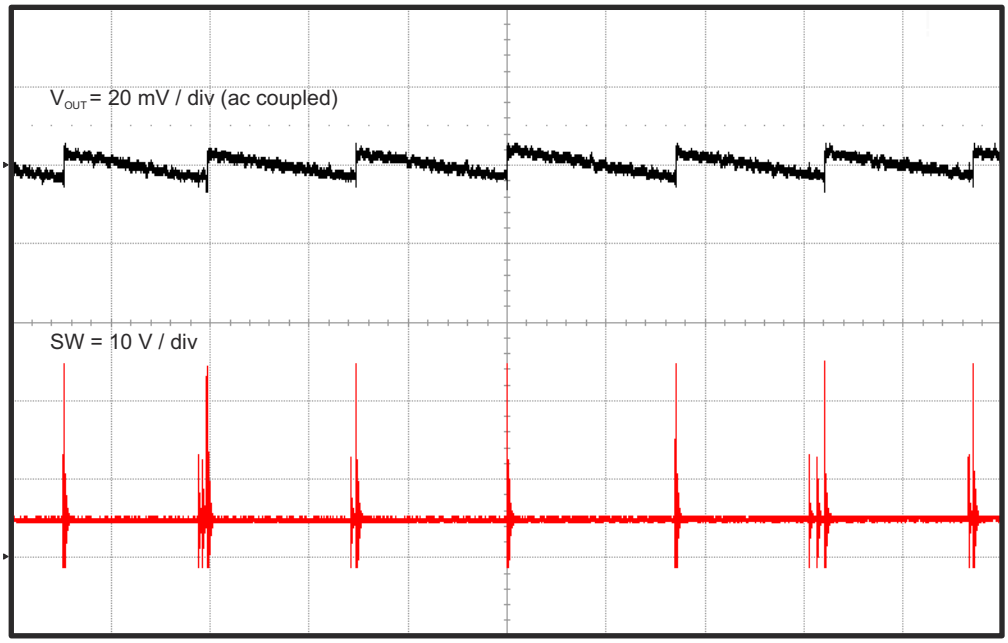


**Figure 2-9. TPS54336AEVM-010 Output Ripple, $I_{OUT}$ = 0 A**

## 2.8 Input Voltage Ripple

Figure 2-10 shows the TPS54336AEVM-010 input voltage ripple. The output current is the rated full load of 3 A and $V_{IN}$ = 24 V. The ripple voltage is measured directly across the input capacitors.

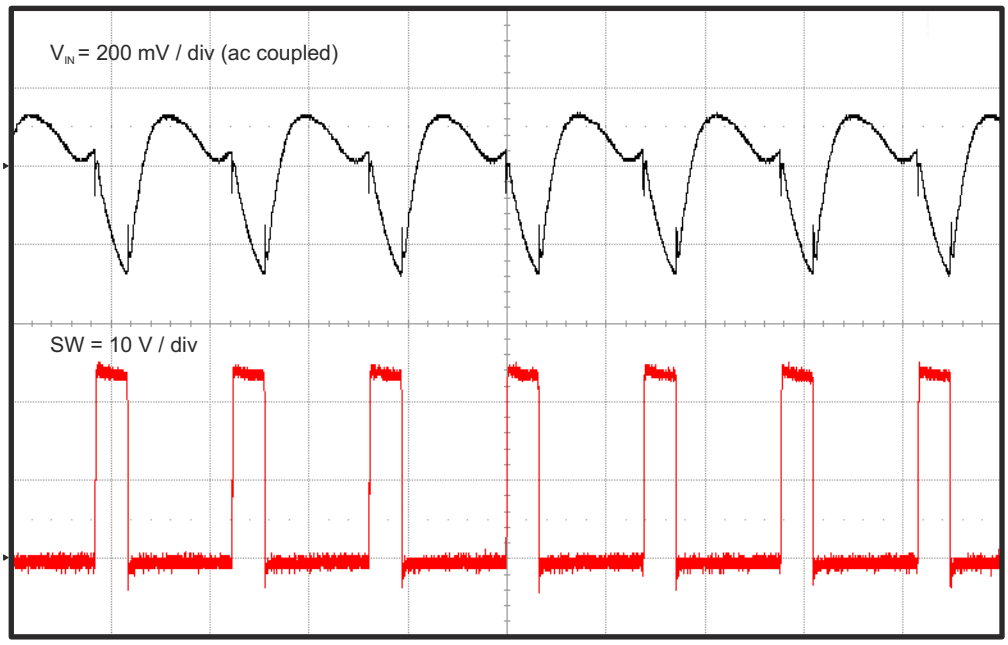


**Figure 2-10. TPS54336AEVM-010 Input Ripple**

## 2.9 Powering Up

Figure 2-11 and Figure 2-12 show the start-up waveforms for the TPS54336AEVM-010. In Figure 2-11, the output voltage ramps up as soon as the input voltage reaches the UVLO threshold as set by the R1and R2 resistor divider network. In Figure 2-12, the input voltage is initially applied and the output is inhibited by using a jumper at JP1 to tie EN to GND. When the jumper is removed, EN is released. When the EN voltage reaches the enable-threshold voltage, the start-up sequence begins and the output voltage ramps up to the externally set value of 5 V. The input voltage for these plots is 24 V and the load is 5 Ω.

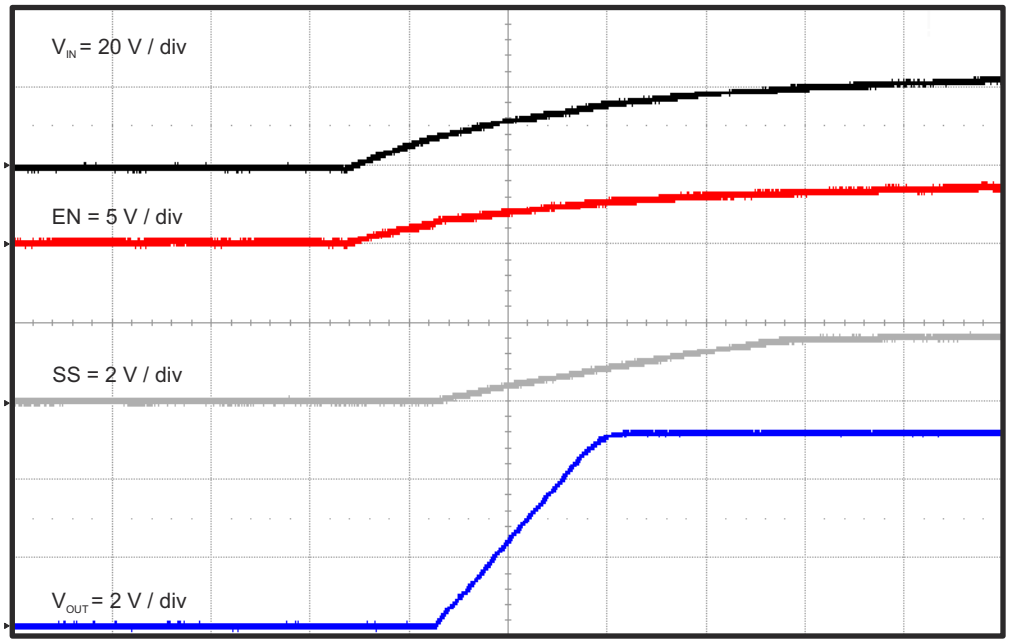


**Figure 2-11. TPS54336AEVM-010 Start-Up Relative to $V_{IN}$**

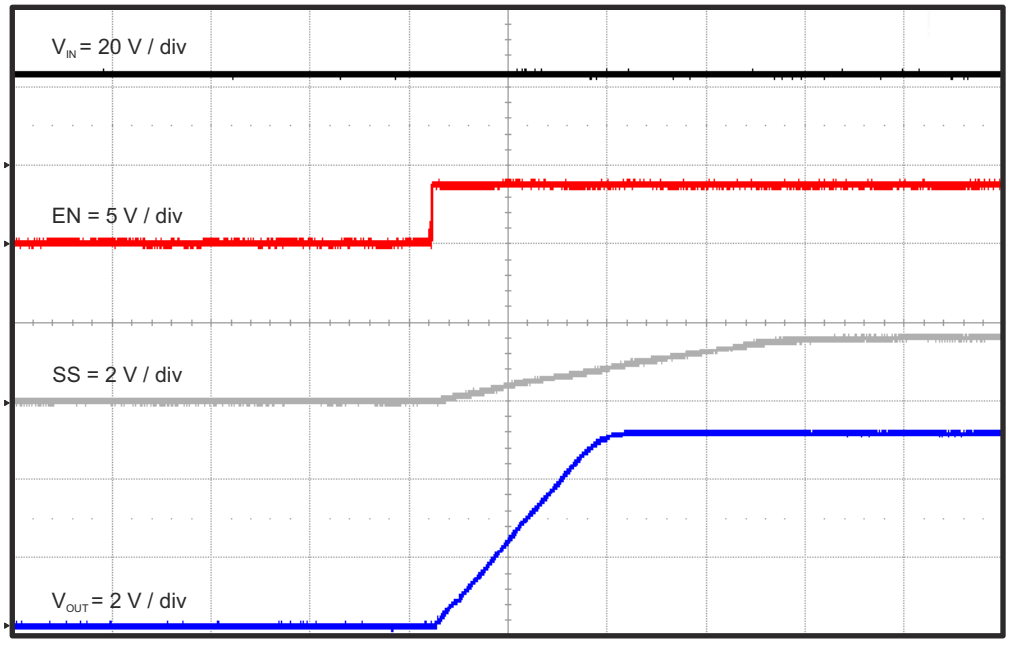


**Figure 2-12. TPS54336AEVM-010 Start-up Relative to Enable**

## 2.10 Powering Down

Figure 2-13 and Figure 2-14 show the start-up waveforms for the TPS54336AEVM-010. In Figure 2-13, the output voltage ramps down as soon as the input voltage falls below the UVLO stop threshold as set by the R1 and R2 resistor divider network. In Figure 2-14, the output is inhibited by using a jumper at JP1 to tie EN to GND. The input voltage for these plots is 24 V and the load is 5 Ω.

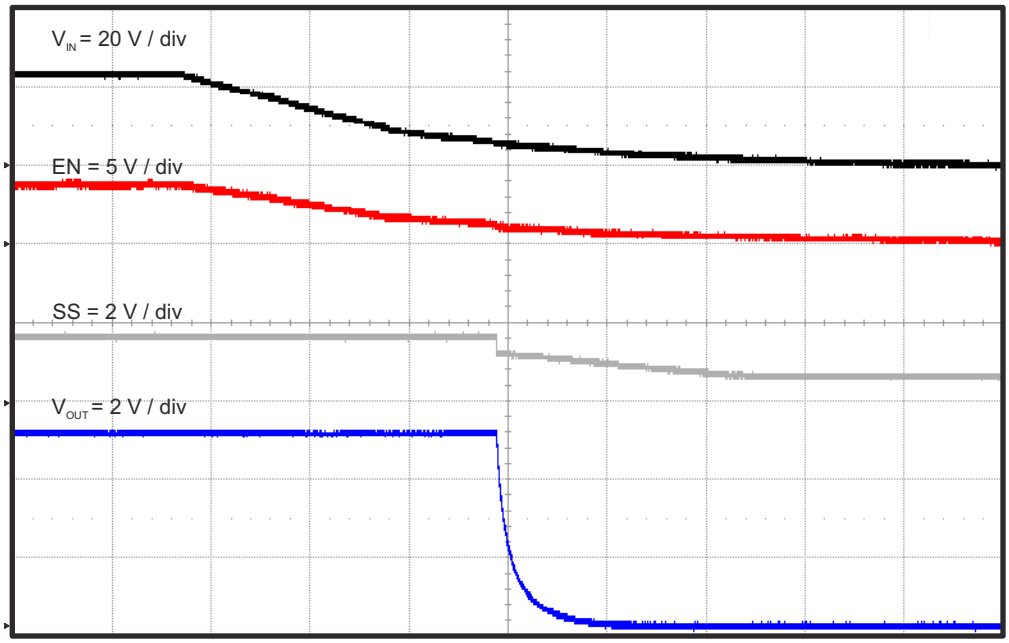


**Figure 2-13. TPS54336AEVM-010 Shut-down Relative to $V_{IN}$**

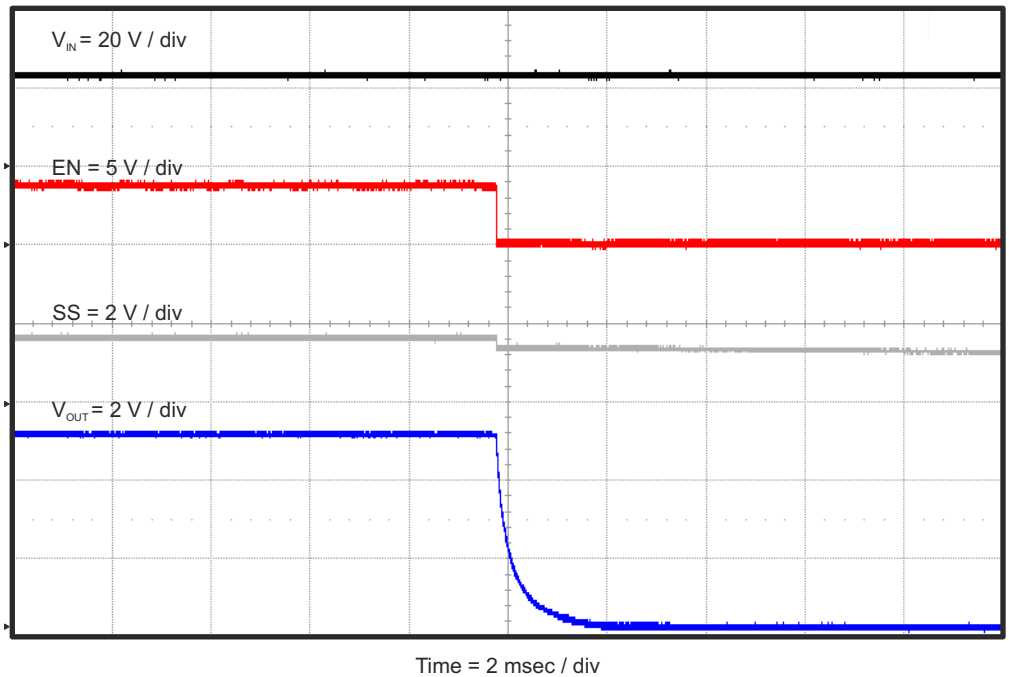


**Figure 2-14. TPS54336AEVM-010 Shut-down Relative to EN**

# 3 Board Layout

This section provides a description of the TPS54336AEVM-010, board layout, and layer illustrations.

## 3.1 Layout

Figure 3-1 through Figure 3-3 show the board layout for the TPS54336AEVM-010. The topside layer of the EVM is laid out in a manner typical of a user application. The top and bottom layers are 2-oz. copper.

The top layer contains the main power traces for $V_{IN}$, $V_{OUT}$, and VPHASE. Also on the top layer are connections for the remaining pins of the TPS54336A and a large area filled with ground. To facilitate the placement of the main input bypass capacitor as close to the $V_{IN}$ and GND pins as possible, the trace for VPHASE is routed to the bottom layer immediately at the pin 3 connection. It is routed back to the top layer at the L1 inductor and C4 BOOT capacitor. The bottom layer contains a ground plane plus a copper fill area for VPHASE, an etch run to connect the upper resistor of the voltage set point divider to the regulation point at the J2 output connector, and a trace to connect the upper resistor of the UVLO set point divider network to $V_{IN}$. The top-side ground areas are connected to the bottom and internal ground planes with multiple vias placed around the board including four vias directly under the TPS54336A device to provide a thermal path from the top-side ground area to the bottom-side and internal ground planes.

The input decoupling capacitors (C2, and C1) and bootstrap capacitor (C4) are all located as close to the IC as possible. In addition, the voltage set-point resistor divider components are also kept close to the IC. The BSR010 PCB is set up to accommodate both the TPS54335A and TPS54336A. For TPS54335A, the RT resistor R3 is used, while for TPS54336A, C3 is used to set the adjustable slow-start time. For the TPS54336A, an additional input bulk capacitor may be required, depending on the EVM connection to the input supply.

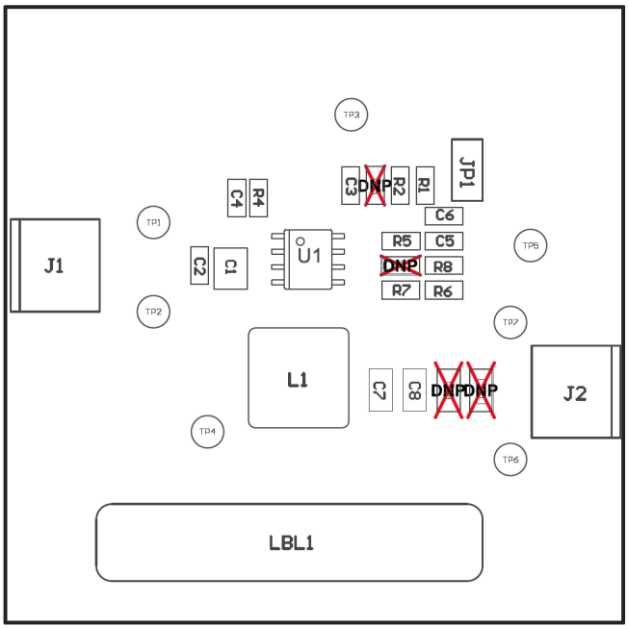


**Figure 3-1. TPS54336AEVM-010 Top-Side Assembly**

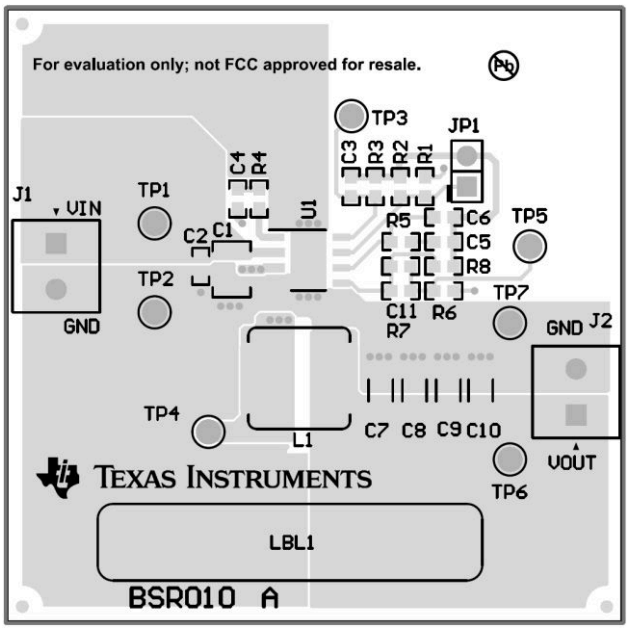


**Figure 3-2. TPS54336AEVM-010 Top-Side Layout**

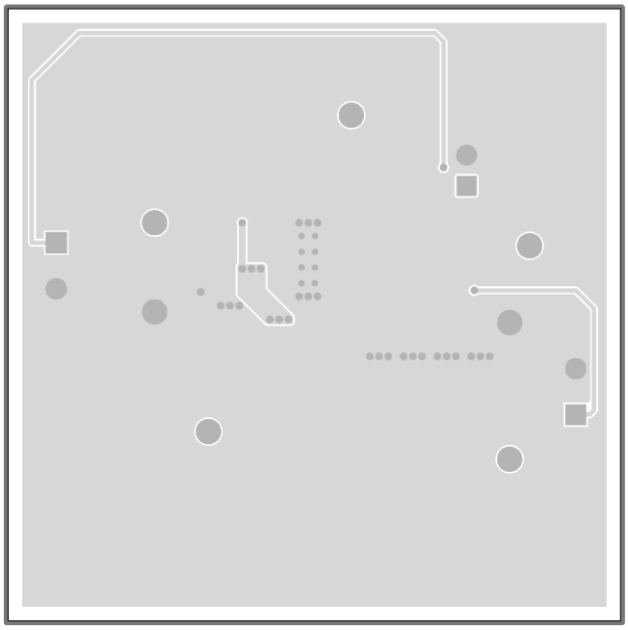

**Figure 3-3. TPS54336AEVM-010 Bottom-Side Layout**

# 4 Schematic and Bill of Materials

This section presents the TPS54336AEVM-010 schematic and bill of materials.

## 4.1 Schematic

Figure 4-1 is the schematic for the TPS54336AEVM-010.

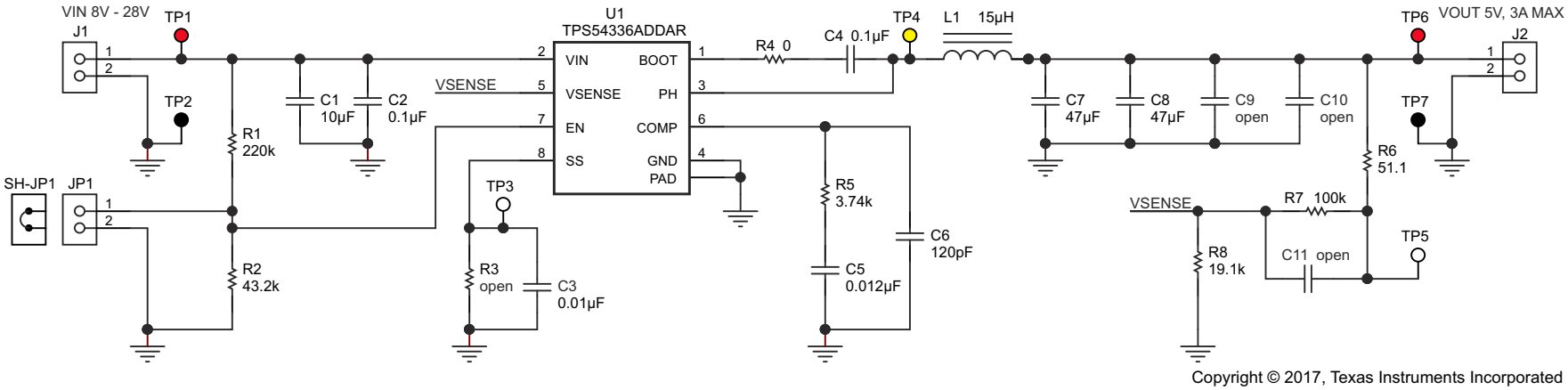


**Figure 4-1. TPS54336AEVM-010 Schematic**

## 4.2 Bill of Materials

Table 4-1 presents the bill of materials for the TPS54336AEVM-010.

**Table 4-1. TPS54336AEVM-010 Bill of Materials**

| DESIGNATOR | QUANTITY | VALUE | DESCRIPTION | PACKAGEREFERENCE | PARTNUMBER | MANUFACTURER |
|---|---|---|---|---|---|---|
| C1 | 1 | 10 µF | CAP, CERM, 10 µF, 35 V, ±10%, X7R, 1210 | 1210 | GRM32ER7YA106KA12L | MuRata |
| C2, C4 | 2 | 0.1 µF | CAP, CERM, 0.1 µF, 50 V, ±10%, X7R, 0603 | 0603 | GRM188R71H104KA93D | MuRata |
| C3 | 1 | 0.01 µF | CAP, CERM, 0.01 µF, 50 V, ±10%, X5R, 0603 | 0603 | GRM188R61H103KA01D | MuRata |
| C5 | 1 | 0.012 µF | CAP, CERM, 0.012 µF, 50 V, ±10%, X7R, 0603 | 0603 | GRM188R71H123KA01D | MuRata |
| C6 | 1 | 120 pF | CAP, CERM, 120 pF, 50 V, ±5%, C0G/NP0, 0603 | 0603 | GRM1885C1H121JA01D | MuRata |
| C7, C8 | 2 | 47 µF | CAP, CERM, 47 µF, 10 V, ±10%, X5R, 1206 | 1206 | GRM31CR61A476KE15L | MuRata |
| C9, C10 | 0 | | CAP, CERM, 1206 | 1206 | | |
| C11 | 0 | | CAP, CERM, 0603 | 603 | | |
| J1, J2 | 2 | | Conn Term Block, 2POS, 3.81 mm, TH | 2 × 1, 3.81 mm | 1727010 | Phoenix Contact |
| JP1 | 1 | | Header, TH, 100mil, 2 × 1, Gold plated, 230 mil above insulator | 2 × 1, 100 mil | TSW-102-07-G-S | Samtec, Inc. |
| L1 | 1 | 15 µH | Inductor, Shielded, Composite, 15 µH, 5.8A, 0.04 Ω, SMD | 322 × 158 × 322 mil | IHLP3232DZER150M5A | Vishay-Dale |
| R1 | 1 | 220 k | RES, 220 k ×, 1%, 0.1W, 0603 | 0603 | RC0603FR-07220KL | Yageo America |
| R2 | 1 | 43.2 k | RES, 43.2 k Ω, 1%, 0.1W, 0603 | 0603 | CRCW060343K2FKEA | Vishay-Dale |
| R3 | 0 | | RES, 0603 | 0603 | | |
| R4 | 1 | 0 | RES, 0 Ω, 5%, 0.1W, 0603 | 0603 | CRCW06030000Z0EA | Vishay-Dale |

**Table 4-1. TPS54336AEVM-010 Bill of Materials (continued)**

| DESIGNATOR | QUANTITY | VALUE | DESCRIPTION | PACKAGEREFERENCE | PARTNUMBER | MANUFACTURER |
|---|---|---|---|---|---|---|
| R5 | 1 | 3.74 k | RES, 3.74 k Ω, 1%, 0.1W, 0603 | 0603 | CRCW06033K74FKEA | Vishay-Dale |
| R6 | 1 | 51.1 | RES, 51.1 Ω, 1%, 0.1W, 0603 | 0603 | CRCW060351R1FKEA | Vishay-Dale |
| R7 | 1 | 100 k | RES, 100 k Ω, 1%, 0.1W, 0603 | 0603 | CRCW0603100KFKEA | Vishay-Dale |
| R8 | 1 | 19.1 k | RES, 19.1 k Ω, 1%, 0.1W, 0603 | 0603 | CRCW060319K1FKEA | Vishay-Dale |
| SH-JP1 | 1 | | Shunt, 100mil, Gold plated, Black | | 382811-6 | AMP |
| TP1, TP6 | 2 | Red | Test Point, TH, Miniature, Red | TH, Miniature | 5000 | Keystone |
| TP2, TP7 | 2 | Black | Test Point, TH, Miniature, Black | TH, Miniature | 5001 | Keystone |
| TP3, TP5 | 2 | White | Test Point, TH, Miniature, White | TH, Miniature | 5002 | Keystone |
| TP4 | 1 | Yellow | Test Point, TH, Miniature, Yellow | TH, Miniature | 5004 | Keystone |
| U1 | 1 | | 4.5-V TO 28-V INPUT, 3-A OUTPUT, SYNCHRONOUS STEP DOWN SWIFT CONVERTER, DDA0008E | DDA0008E | TPS54336ADDAR | Texas Instruments |
| PCB | 1 | | Printed Circuit Board | | BSR010 | Any |

# 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision * (July 2017) to Revision A (October 2021) | Page |
|---|---|
| • Updated the numbering format for tables, figures, and cross-references throughout the document. | 3 |

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