*User's Guide*

# *TPS7H1210EVM Evaluation Module (EVM)*


**ABSTRACT**

This user's guide describes operational use of the TPS7H1210EVM evaluation module (EVM) as a reference design for engineering demonstration and evaluation of the TPS7H1210-SEP, low-dropout (LDO) negative-voltage linear regulator in space enhanced plastic. This user's guide provides details about the EVM, its configuration, schematics, and bill of material (BOM).


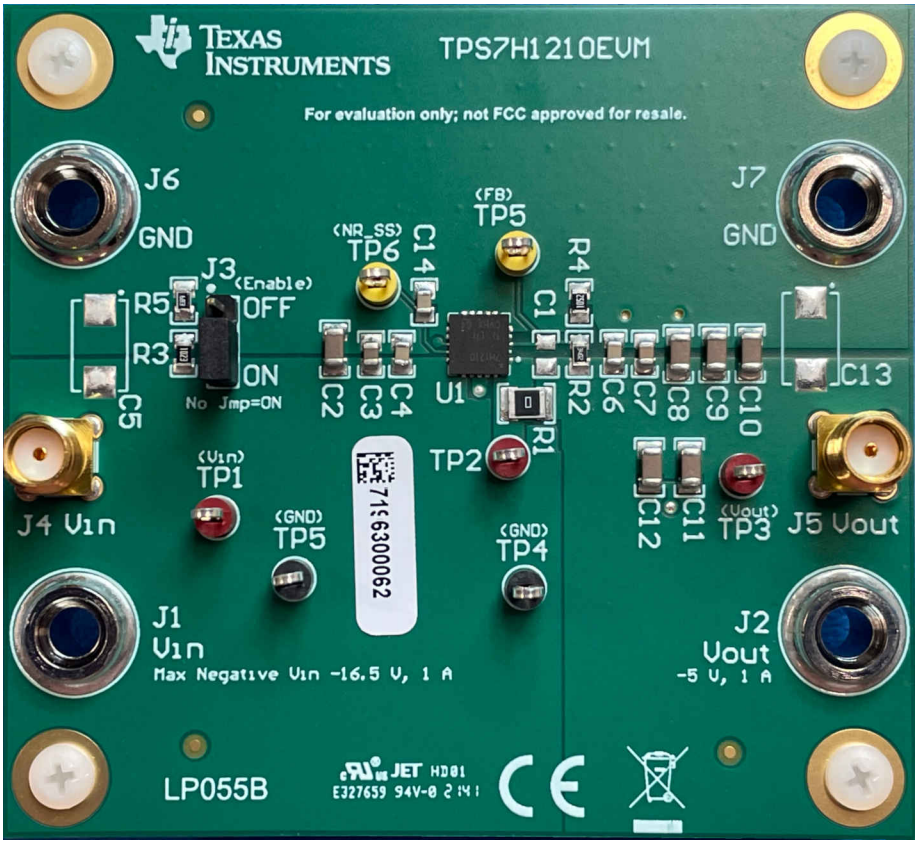


**Figure 1-1. TPS7H1210EVM (LP055B)**

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# 1 Introduction

The TPS7H1210-SEP negative voltage linear regulator is a low noise, high PSRR (power supply rejection ratio) regulator capable of sourcing a maximum load of 1 A.

The EVM is configured with a default feedback divider network to regulate to a –5-V $V_{OUT}$, with a usable $V_{IN}$ range of (–5 V – $V_{DO}$) to –16.5 V. Worst case $V_{DO}$ is 500 mV across recommended operating conditions. The EVM is intended to aid engineers in the evaluation of the operation and performance of the TPS7H1210-SEP linear regulator. The TPS7H1210-SEP low-dropout regulator allows input voltages from –3 V to –16.5 V and is capable of regulating any output voltage between –1.18 V and –15.5 V by changing the feedback resistor divider network. The EVM is capable of delivering up to 1 A to a load. Achieving the maximum load depends on multiple variables, including the input-output power dissipation, board thermal dissipation, and heat removal.

## 1.1 Features

- Low noise, high PSRR
- Input voltage range –3 V to –16.5 V
- Adjustable output range –1.18 V to –15.5 V
- Up to 1-A output
- Built-in current-limit and thermal shutdown

## 1.2 Applications

- Supports low Earth orbit (LEO) space applications
- Satellite electrical power system (EPS)
- Power for analog circuits
  - Data converters: ADCs and DACs (analog-todigital and digital-to-analog converters
  - Op amps (operational amplifiers)
  - Imaging sensors
- Post DC-DC converter regulation and ripple filtering
- Radiation-hardened ultra-clean analog supply for space constrained areas

# 2 Setup

This section describes the jumpers and connectors on the EVM as well as how to properly connect, set up, and use the TPS7H1210EVM.

## 2.1 Input/Output Connectors and Jumper Descriptions

### 2.1.1 J1, J4 (–)$V_{IN}$

Negative input power supply voltage connectors. The negative input lead and ground return lead from the input power supply should be twisted and kept as short as possible to minimize EMI transmission. Additional bulk capacitance should be added between J1 and J6 if the supply leads are greater than six inches. For example, a 47-µF electrolytic capacitor can be populated at C5 to improve the transient response of the TPS7H1210 while eliminating unwanted ringing on the input due to long wire connections. An isolated (+) power supply may be used if the (+) lead is connected to J6 (GND) and the (–) lead is connected to J1 (–$V_{IN}$). J1 is provided as a bananna jack input. J4 is provided as shielded coax SMA connection.

### 2.1.2 J6 GND

Ground-return connector for the $V_{IN}$ input power supply.

### 2.1.3 J2, J5 (–)$V_{OUT}$

Regulated (–) output voltage connectors. J2 is provided as a bananna jack connector, and J5 is provided as shielded coax SMA connection.

### 2.1.4 J7 GND

Output ground-return connector.

### 2.1.5 J3 EN

Output enable. To enable the regulator output, connect a jumper to short between pins 2 and 3. To disable the output, connect a jumper to short between pins 1 and 2. Leaving J3 without a jumper, will enable the regulator through the resistor divider. The resistor divider allows an external signal to driven between pin 2 and pin 1.

The resistor divider will reduce $V_{IN}$ applied to the EN pin to approximately 40% of $V_{IN}$. For lower $V_{IN}$ voltages, the voltage on EN may not be sufficient to meet the $V_{EN(+HI)}$ minimum threshold of 2 V to ensure the regulator is enabled. In this case connect jumper between pin 2 and pin 3 to pull the EN pin to $V_{IN}$.

### 2.1.6 TP1-5 Test Points

There are five test points on the EVM. Table 2-1 shows the connection and function for each test point.

**Table 2-1. Test Points**

| TEST POINT | CONNECTION | FUNCTION |
|---|---|---|
| TP1 | $V_{IN}$ | Provides access to the negative input voltage ($V_{IN}$). |
| TP2 | $V_{OUT}$ | Provides access to the negative output voltage ($V_{OUT}$) prior to R1 0-Ω resistor. R1 may be removed and replaced with wire, or precision resistor for current measurement. |
| TP3 | $V_{OUT}$ | Provides access to negative output voltage ($V_{OUT}$). |
| TP4 | GND | Provides access to ground plane (GND) near $V_{IN}$ plane. |
| TP5 | GND | Provides access to ground plane (GND) near $V_{OUT}$ plane. |

### 2.2 Equipment Setup

1. Before connecting power to J1, turn off the input power supply after verifying that its output voltage is set to a greater absolute value than –5.5 V (–6 V recommended; –16.5 V maximum). Connect the negative voltage lead from the input power supply to $–V_{IN}$, at the J1 connector of the EVM. Connect the ground lead from the input power supply to GND at the J6 connector of the EVM. If using a (+) power supply, connect the (+) lead is to J6 (GND) and the negative lead to J1 ($–V_{IN}$).
2. Connect oscilloscope coax cables to SMA jacks J4 $V_{IN}$, and/or J5 $V_{OUT}$ if desired. Set scope channels to high impedance.
3. Connect desired (≤1 A) load between the $–V_{OUT}$ connector J2, and the GND at connector J7.

**WARNING**

Large $|V_{IN} – V_{OUT}|$ differentials can lead to excessive internal power dissipation when operating at higher $I_{LOAD}$ currents. Internal power dissipation can be calculated with $|V_{IN} – V_{OUT}| \times I_{LOAD}$.

## 3 Operation

1. Enable supply. If J3 has jumper set to disable (short between pin 1 and pin 2), remove jumper to enable, or place jumper on pin 2 and pin 3. For initial operation, it is recommended that the input power supply, $–V_{IN}$ on J1, be set to –6 V.
2. Vary the load and $–V_{IN}$ voltage as necessary for test purposes.

# 4 Adjustable Operation

The nominal output voltage for the typical LDO circuit employing the TPS7H1210-SEP is set by two external resistors, $R_{FB\_TOP}$ and $R_{FB\_BOT}$, as illustrated in Figure 4-1. $R_{FB\_TOP}$ and $R_{FB\_BOT}$ can be calculated for any output voltage using Equation 1and Equation 2. $V_{FB}$ is the Vref voltage found in the device data sheet under the Electrical Characteristics and is nominally 1.182 V.

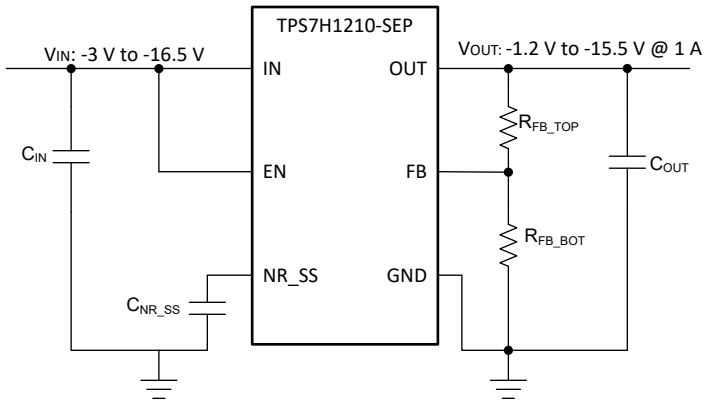


**Figure 4-1. TPS7H1210-SEP LDO Schematic Showing Adjustment Resistors**

$$R_{FB\_BOT} = \frac{R_{FB\_TOP}}{\frac{V_{OUT}}{V_{FB}} - 1} \tag{1}$$

where

$$\frac{V_{OUT}}{R_{FB\_TOP} + R_{FB\_BOT}} \geq 5\ \mu A \tag{2}$$

Once the resistor values have been calculated, the new resistors can be installed appropriately in the correct place using the PCB and schematic diagrams of Figure 6-1 through Figure 6-4 and Figure 7-1.

For additional information on adjustable operation, see the TPS7H1210-SEP data sheet (SBVS414).

# 5 Test Results

This section provides typical performance waveforms for the TPS7H1210EVM.

## 5.1 Enable, Disable, and Soft Start Timing

Figure 5-1 shows the enable and disable characteristic where $-V_{IN}$ is –6 V, EN is toggled from ground to –2.4 V while the output drives a 1-A load. The waveform for $V_{FB}$ is also shown for reference. $C_{NR\_SS}$ of 100 nF results in a soft start time of approximately 120 ms.

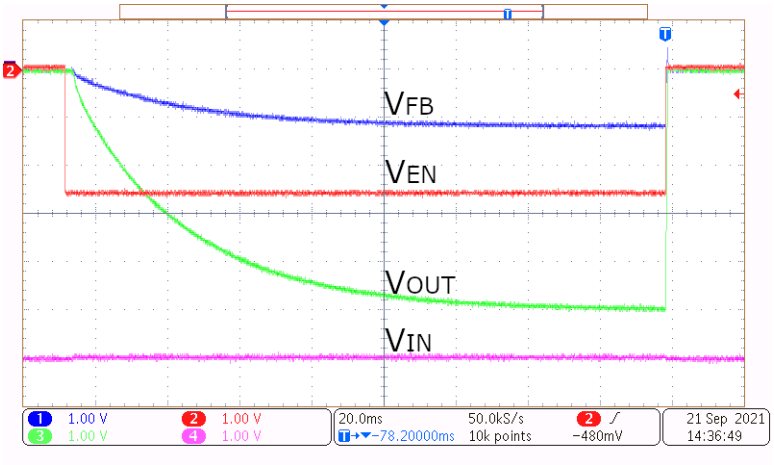


**Figure 5-1. Enable and Disable Timing**

## 5.2 Output Load Transients

Figure 5-2 shows the load transient response (Chan 2 $V_{OUT}$, red) for a load step transient from 1 mA to 500 mA (Chan 4 $V_{IN}$, purple). The TPS7H1210EVM was operating at stock configuration with $V_{IN}$ = –6 V, $V_{OUT}$ = –5 V. Figure 5-2 shows the load transient from 500 mA to 1 mA.

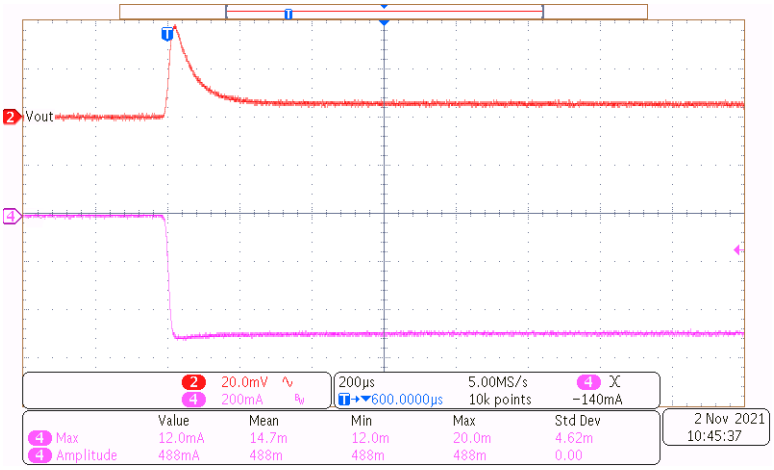


**Figure 5-2. Load Step Transient Response Rising**

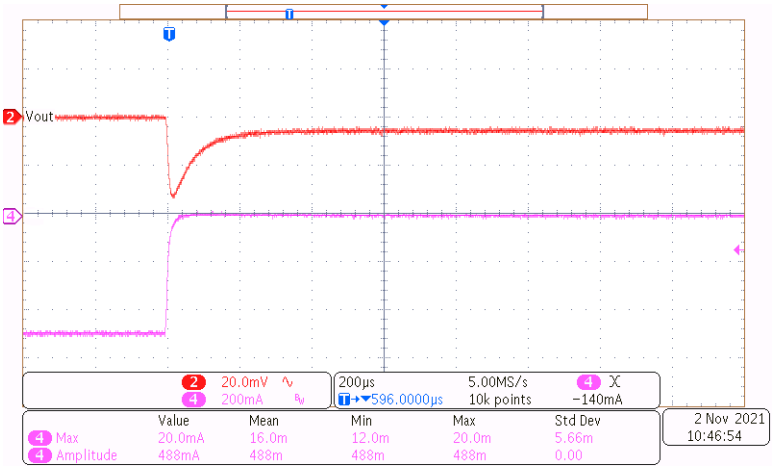


**Figure 5-3. Load Step Transient Response Falling**

## 5.3 PSRR

Figure 5-4 shows the typical PSRR performance of the TPS7H1210EVM operating with the following conditions: $V_{IN}$ = –6 V, $V_{OUT}$ = –5 V, $I_{LOAD}$ = 1 A, $C_{IN}$ removed, Vinjection = ±100 mV.

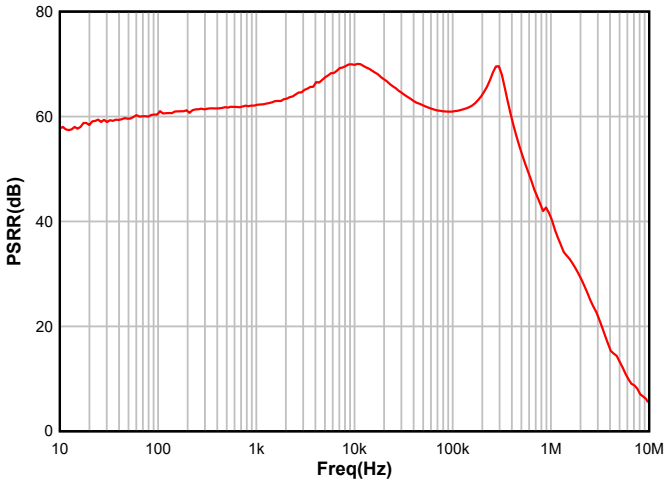


**Figure 5-4. TPS7H1210EVM PSRR**

## 5.4 Noise Spectral Density

Figure 5-5 shows the typical noise spectral density (NSD) performance of the TPS7H1210EVM operating with the following conditions: $V_{IN}$ = –6 V, $V_{OUT}$ = –5 V, $I_{LOAD}$ = 1 A.

10-Hz to 100-kHz integrated RMS noise $V_N$ = 27.2 $\mu V_{RMS}$.

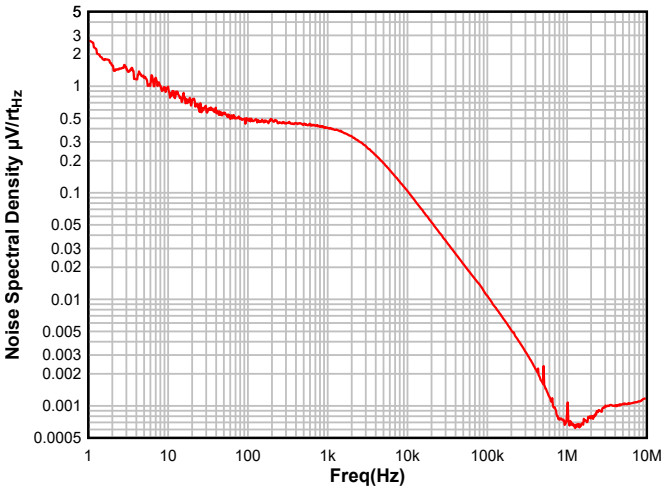


**Figure 5-5. TPS7H1210EVM NSD**

## 6 Board Layout

The following images represent the board design layers.

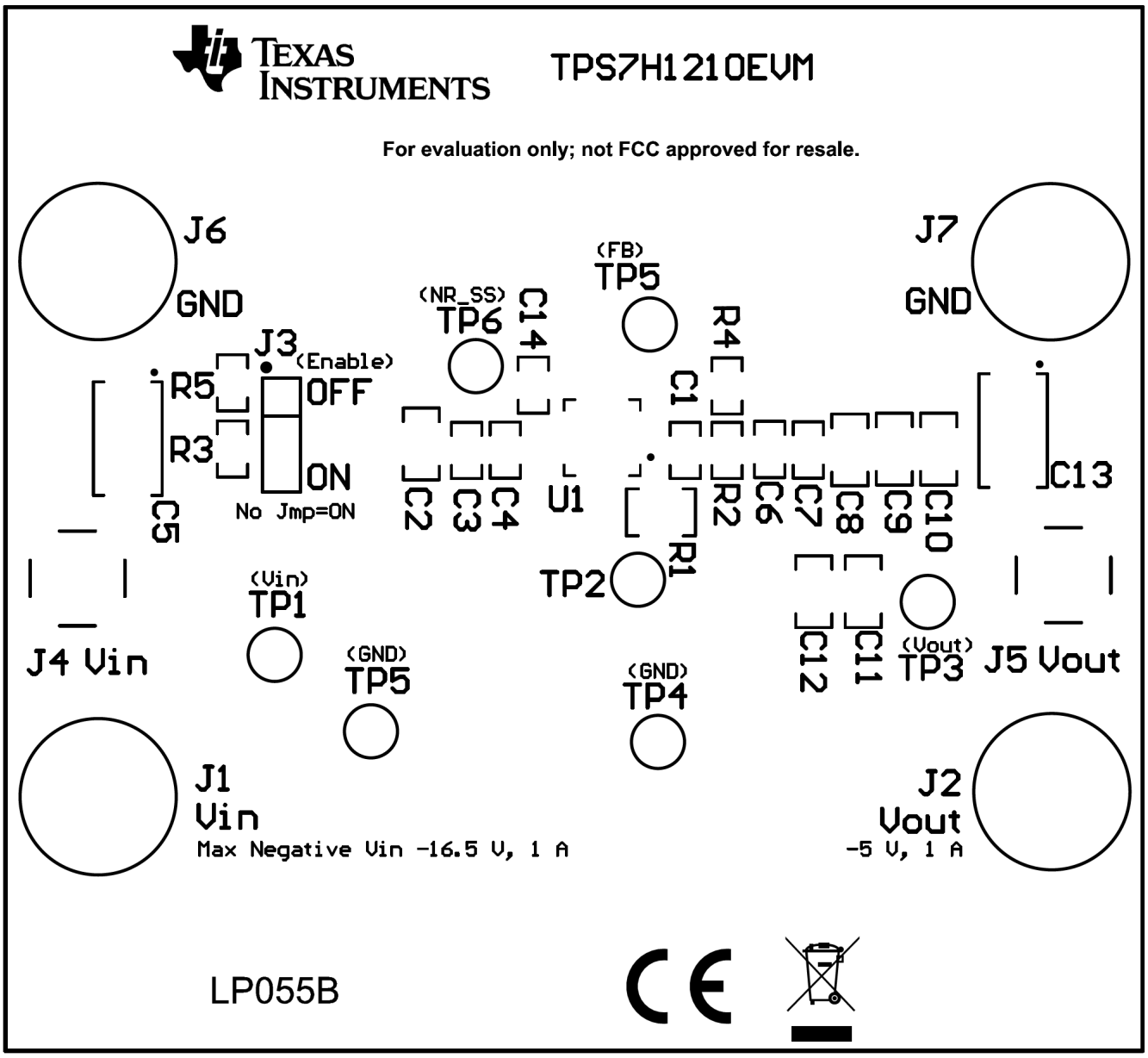


**Figure 6-1. Top Overlay Silkscreen**

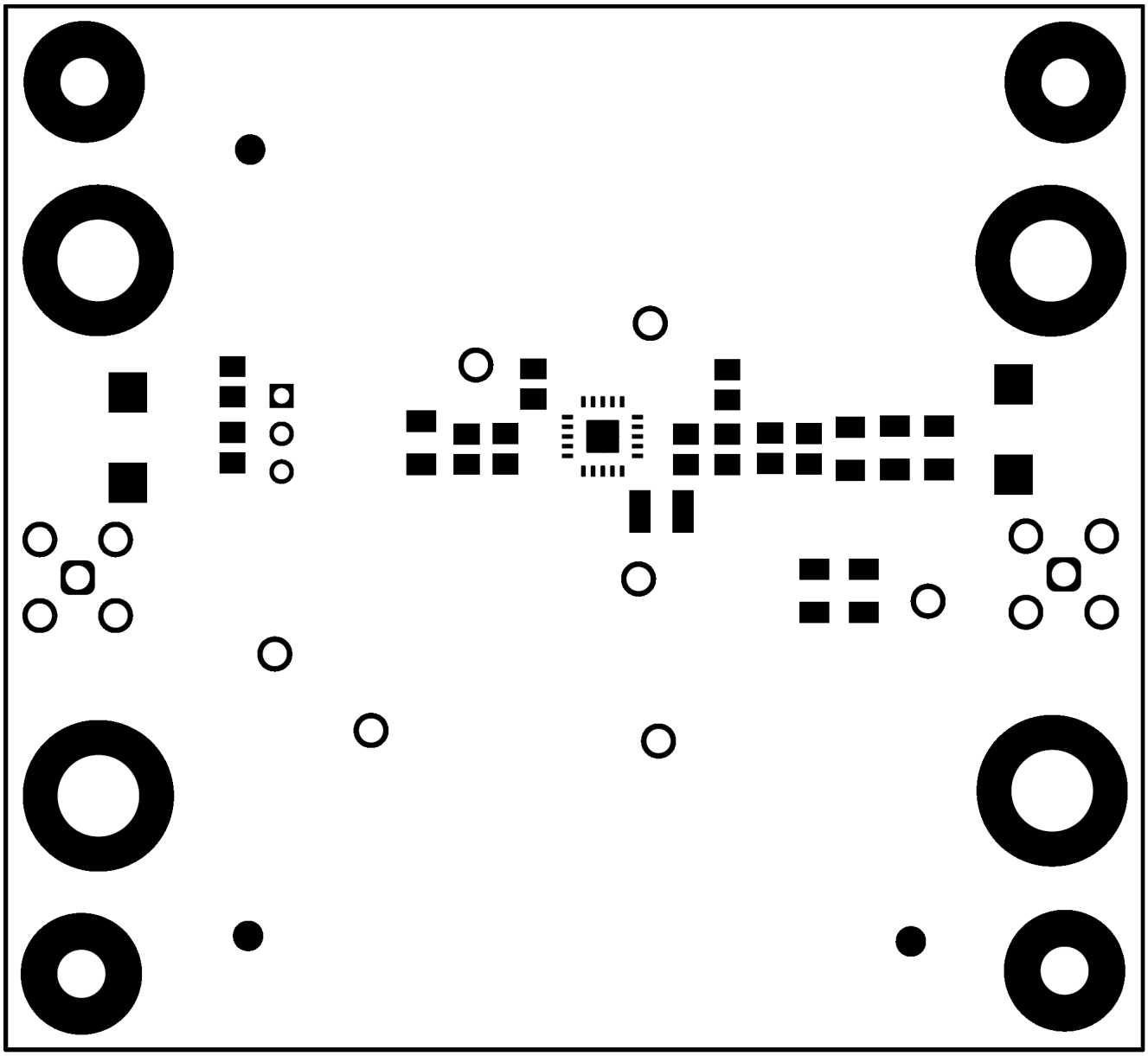

**Figure 6-2. Top Solder Mask**

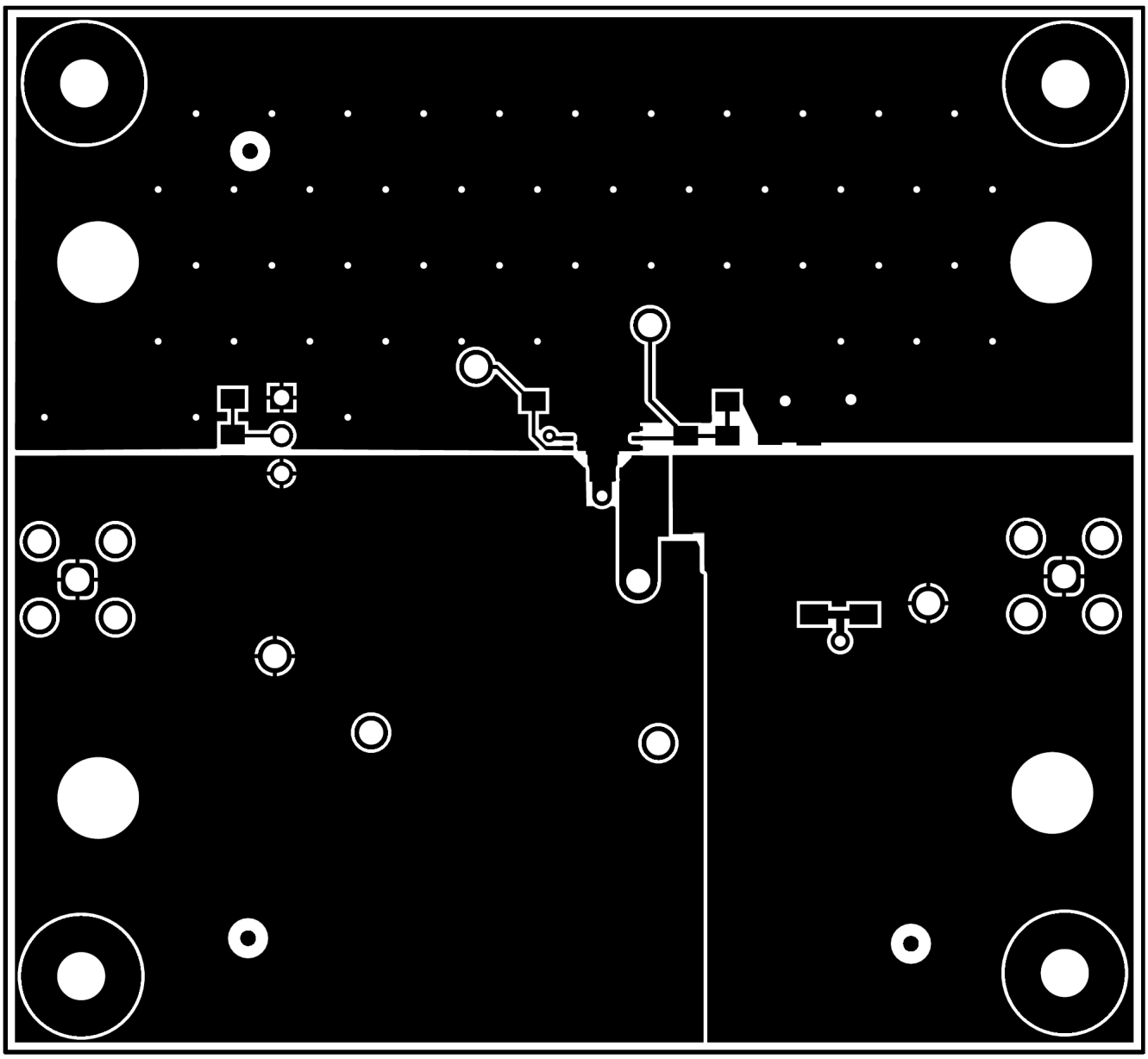

**Figure 6-3. Top Signal Layer**

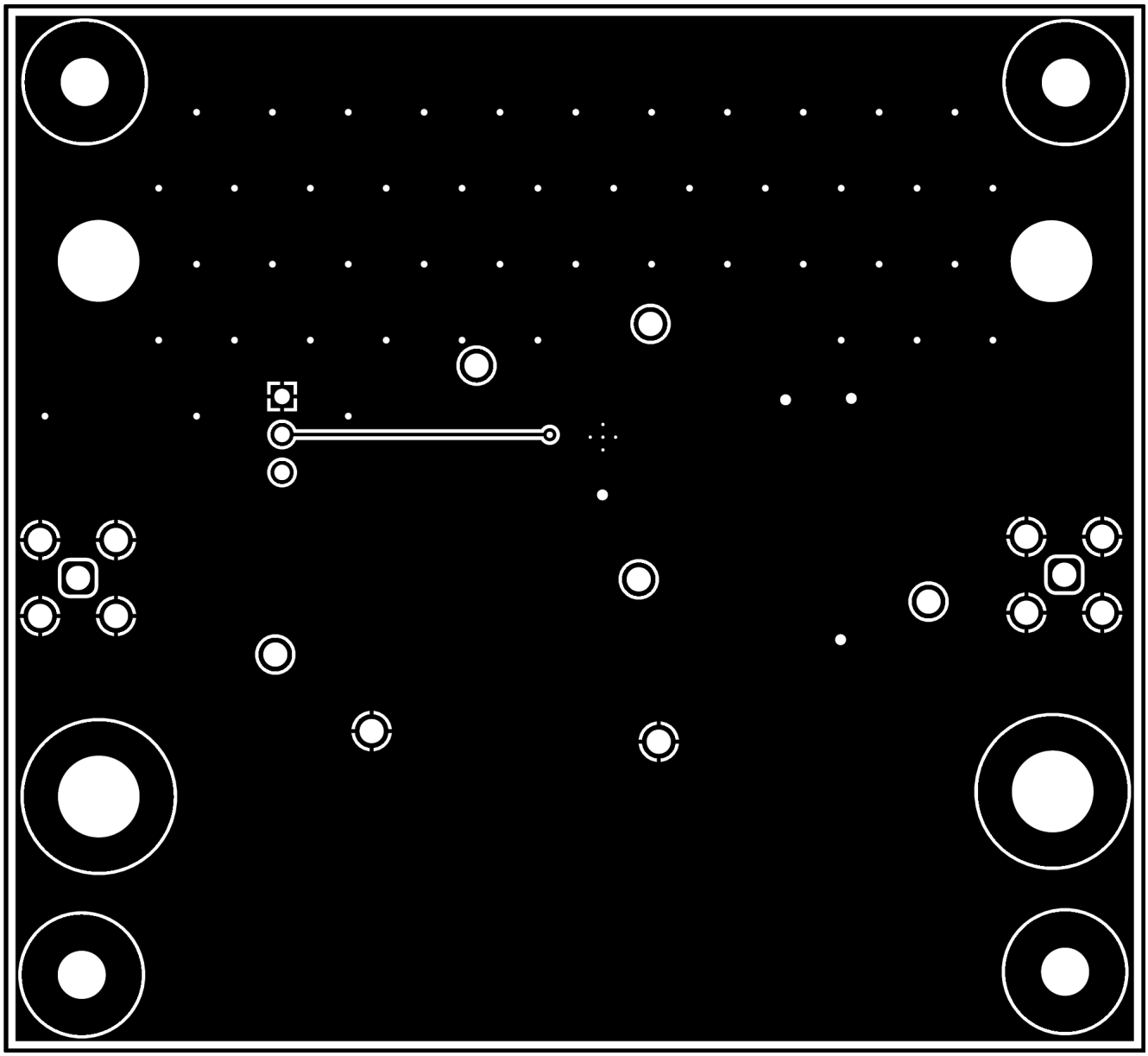

**Figure 6-4. Bottom Signal Layer**

# 7 Schematic and Bill of Materials

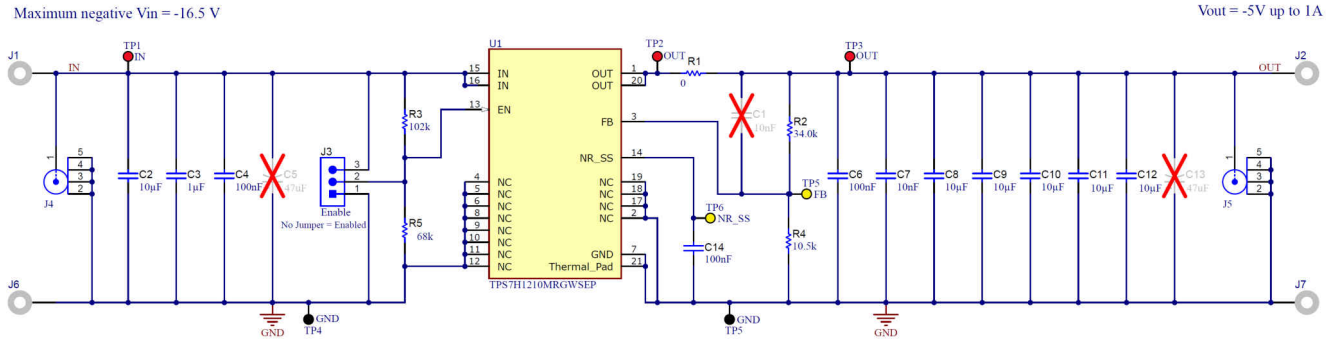


**Figure 7-1. TPS7H1210EVM (LP055B) Schematic**

The TPS7H1210EVM schematic has a placeholder for use of a feed forward capacitance C1. Caution is encouraged when using a feed-forward ($C_{FF}$) with the TPS7H1210-SEP device. While a feed-forward capacitor can provide some improvements in PSRR at certain frequencies, it also has additional risks. Specifically, a feed-forward capacitor can cause the FB pin to go to positive during shutdown, thus damaging the device. See *Pros and Cons of Using a Feed-Forward Capacitor with a Low Dropout Regulator* application report for additional information.

**Table 7-1. TPS7H1210EVM (LP055B) Bill of Materials**

| Designator | Qty | Value | Description | Package-Ref | PartNumber | Manufacturer |
|---|---|---|---|---|---|---|
| !PCB1 | 1 | | Printed Circuit Board | | LP055 | Any |
| C2, C8, C9, C10, C11, C12 | 6 | 10uF | CAP, CERM, 10 µF, 50 V,+/- 10%, X7R, AEC-Q200 Grade 1, 1206 | 1206 | CGA5L1X7R1H106K160AE | TDK |
| C3 | 1 | 1uF | CAP, CERM, 1 uF, 50 V, +/- 10%, X7R, 0805 | 805 | C0805C105K5RACTU | Kemet |
| C4, C6, C14 | 3 | 0.1uF | CAP, CERM, 0.1 uF, 50 V, +/- 5%, X7R, 0805 | 805 | C0805C104J5RACTU | Kemet |
| C7 | 1 | 0.01uF | CAP, CERM, 0.01 uF, 50 V, +/- 20%, X7R, 0805 | 805 | C0805C103M5RACTU | Kemet |
| H1, H2, H3, H4 | 4 | | Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead | Screw | NY PMS 440 0025 PH | B&F Fastener Supply |
| H5, H6, H7, H8 | 4 | | Standoff, Hex, 0.5"L #4-40 Nylon | Standoff | 1902C | Keystone |
| J1, J2, J6, J7 | 4 | | Standard Banana Jack, Uninsulated, 8.9mm | Keystone575-8 | 575-8 | Keystone |
| J3 | 1 | | Header, 100mil, 3x1, Tin, TH | Header, 3 PIN, 100mil, Tin | PEC03SAAN | Sullins Connector Solutions |
| J4, J5 | 2 | | SMA, 50 Ohm, Gold, TH | SMA, TH | 32K101-400L5 | Rosenberger |
| R1 | 1 | 0 | RES, 0, 1%, 0.5 W, AEC-Q200 Grade 0, 1210 | 1210 | CRCW12100000Z0EA | Vishay-Dale |
| R2 | 1 | 34.0k | RES, 34.0 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805 | 805 | ERJ-6ENF3402V | Panasonic |
| R3 | 1 | 102k | RES, 102 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805 | 805 | ERJ-6ENF1023V | Panasonic |
| R4 | 1 | 10.5k | RES, 10.5 k, 1%, 0.125 W, AEC-Q200 Grade 0, 0805 | 805 | ERJ-6ENF1052V | Panasonic |
| R5 | 1 | 68k | RES, 68 k, 5%, 0.125 W, AEC-Q200 Grade 0, 0805 | 805 | ERJ-6GEYJ683V | Panasonic |
| TP1, TP2, TP3 | 3 | | Test Point, Multipurpose, Red, TH | Red Multipurpose Testpoint | 5010 | Keystone |

**Table 7-1. TPS7H1210EVM (LP055B) Bill of Materials (continued)**

| Designator | Qty | Value | Description | Package-Ref | PartNumber | Manufacturer |
|---|---|---|---|---|---|---|
| TP4, TP5 | 2 | | Test Point, Multipurpose, Black, TH | Black Multipurpose Testpoint | 5011 | Keystone |
| TP5, TP6 | 2 | | Test Point, Multipurpose, Yellow, TH | Yellow Multipurpose Testpoint | 5014 | Keystone |
| U1 | 1 | | 16.5-V, 1-A, Negative Linear Regulator in Space Enhanced Plastic | VQFN20 | TPS7H1210MRGWSEP | Texas Instruments |
| C1 | 0 | 0.01uF | CAP, CERM, 0.01 uF, 50 V, +/- 20%, X7R, 0805 | 805 | C0805C103M5RACTU | Kemet |
| C5, C13 | 0 | 47uF | CAP, TA, 47 uF, 35 V, +/- 20%, 0.9 ohm, AEC-Q200 Grade 1, SMD | 7343-43 | TAJE476M035RNJ | AVX |
| FID1, FID2, FID3 | 0 | | Fiducial mark. There is nothing to buy or mount. | N/A | N/A | N/A |

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