High-Performance Analog Products

Analog Applications Journal

Second Quarter, 2009

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A linear regulator often requires significant inrush current at start-up to charge output capacitors and supply current to the load. Without inrush or soft-start control, the input current is typically clamped to the regulator's current limit and can cause input-voltage droop. This article presents several examples of regulators with soft-start capabilities that provide predictable inrush current at start-up as an integral part of the design.

Designing a linear Li-Ion battery charger with power-path control. 12

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An ADC's requirement for a low-level differential input can be a problem when the input signal is at a high level such as ±10 V. This article presents the use of a fully differential operational amplifier (FDA) to match a balanced, differential bipolar input signal to the ADC input requirements. Circuit analysis is performed to aid understanding of the key design points, and a design methodology is presented for calculating the required component values. Spreadsheet calculation tools are provided along with example TINA-TI™ SPICE models to show how to implement the design methodology.

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Introduction

Analog Applications Journal is a collection of analog application articles designed to give readers a basic understanding of TI products and to provide simple but practical examples for typical applications. Written not only for design engineers but also for engineering managers, technicians, system designers and marketing and sales personnel, the book emphasizes general application concepts over lengthy mathematical analyses.

These applications are not intended as "how-to" instructions for specific circuits but as examples of how devices could be used to solve specific design requirements. Readers will find tutorial information as well as practical engineering solutions on components from the following categories:

- Data Acquisition
- Power Management
- Interface (Data Transmission)
- Amplifiers: Op Amps

Where applicable, readers will also find software routines and program structures. Finally, *Analog Applications Journal* includes helpful hints and rules of thumb to guide readers in preparing for their design.

How the voltage reference affects ADC performance, Part 1

By Bonnie Baker, *Senior Applications Engineer,*
and Miro Oljaca, *Senior Applications Engineer*

Introduction

When designing a mixed-signal system, many designers have a tendency to examine and optimize each component separately. This myopic approach can go only so far if the goal is to have a working design at the end of the day. Given the array of different components in a system, designers must have a complete understanding of not only the individual components but also their impact on the overall system performance. When a design has an analog-to-digital converter (ADC), it is critical to understand how this device interacts with the voltage reference and voltage-reference buffer.

This article is the first of a three-part series. Parts 2 and 3 will appear in future issues of the *Analog Applications Journal*. Part 1 looks at the fundamental operation of an ADC independently, exactly as many designers do, and then at the performance characteristics that have an impact on the accuracy and repeatability of the system. Part 2 will delve into the voltage-reference device, once again examining its fundamental operation and then the details of its impact on the performance of the ADC. Part 3 will investigate the impact of the voltage-reference buffer and the capacitors that follow it, and will discuss how to ensure that the amplifier is stable. Assumptions and conclusions will be compared to measurement results. The interplay between the driving amplifier, voltage reference, and converter will be briefly analyzed, followed by an investigation of the sources of error in the ADC's conversion results.

The fundamentals of ADCs

Figure 1 shows the voltage-reference system for the successive-approximation-register (SAR) ADC that will be examined in this three-part series. As the name suggests, the ADC converts an analog voltage to a digital code. The overall system accuracy and repeatability depend on how effectively the converter executes this process. The accuracy of this conversion can be defined with static specifications, and the repeatability with dynamic specifications. Generally, the ADC static specifications are offset-voltage error, gain error, and transition noise. The ADC dynamic specifications are signal-to-noise ratio (SNR), total harmonic distortion (THD), and spurious-free dynamic range (SFDR).

Static performance

Figure 2 shows an ideal and an actual (or non-ideal) transfer function of a 3-bit ADC. The actual transfer function has an offset-voltage error and a gain error. In the example application circuit, only the ADC gain error, transition noise, and SNR are of concern.

Figure 1. Voltage-reference system for SAR ADC

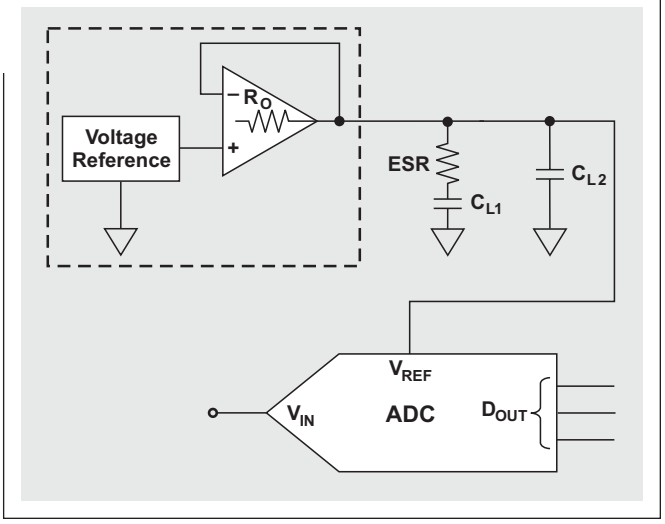


Figure 2. Ideal and actual ADC transfer functions with offset and gain errors

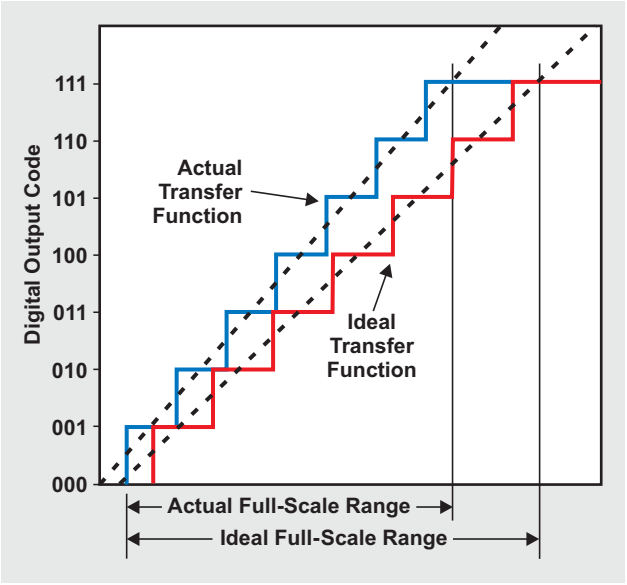
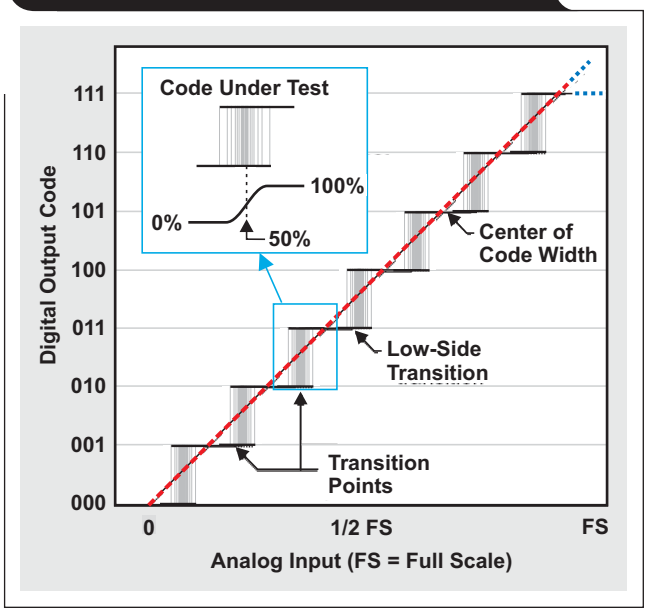


Figure 3. Transition noise with a 3-bit ADC



Equation 1 describes the typical transfer function of the ideal (error-free) ADC:

$$\text{Code} = V_{IN} \times \frac{2^n}{V_{REF}}, \quad \textbf{(1)}$$

where "Code" is the ADC output code in decimal form, V_{IN} is the analog input voltage (in volts), n is the resolution of the ADC (or number of output-code bits), and V_{REF} is the analog value of the voltage reference (in volts). This equation demonstrates that the ADC output code is directly proportional to the analog input voltage and inversely proportional to the voltage reference. Equation 1 also shows that the output code depends on the number of bits (the converter resolution).

The DC errors of non-ideal ADCs are offset-voltage error and gain error. If the offset-voltage error is introduced into the transfer function, Equation 1 can be rewritten as

$$\text{Code} = \left(V_{IN} - V_{OS_ADC}\right) \times \frac{2^n}{V_{REF}}, \quad \textbf{(2)}$$

where V_{OS_ADC} is the input offset voltage of the ADC. Gain error is equal to the difference between the ideal slope from zero to full scale and the actual slope from zero to full scale. The notation for gain error is a decimal or percentage. If the impact of only the gain error (no offset-voltage error) on an ADC is considered, Equation 1 can be rewritten as

$$\text{Code} = V_{IN} \times \frac{2^n}{V_{REF}\left(1 - GE_{ADC}\right)}, \quad \textbf{(3)}$$

where GE_{ADC} is the gain error in decimal form, expressed as

$$GE_{ADC} = \frac{\text{Actual Gain} - \text{Ideal Gain}}{\text{Actual Gain}}.$$

From Equation 3 it can be seen that the gain-error factor adds to the initial accuracy of V_{REF}. The output code is inversely proportional to the combination of the voltage reference plus the gain error. The DC error caused by noise from the voltage-reference chip inversely impacts the gain accuracy of the ADC. Part 2 of this series will specifically show the impact of the voltage reference's errors.

Equations 2 and 3 can be combined to show the final transfer function:

$$\text{Code} = \left(V_{IN} - V_{OS_ADC}\right) \times \frac{2^n}{V_{REF}\left(1 - GE_{ADC}\right)} \quad \textbf{(4)}$$

To analyze ADC transition noise, the code transition points in the ADC's transfer curve can be examined. These are the points where the digital output switches from one code to the next as a result of a changing analog input voltage. The transition point from code to code is not a single threshold but a small region of uncertainty. Figure 3 shows the uncertainty at these transitions that results from internal converter noise. The region of uncertainty is defined by measuring repetitive code transitions from code to code.

An ADC's transition noise has a direct effect on the signal-to-noise ratio (SNR) of the converter. Since it is important to understand this phenomenon, Part 2 of this series will look more closely at voltage-reference noise characteristics.

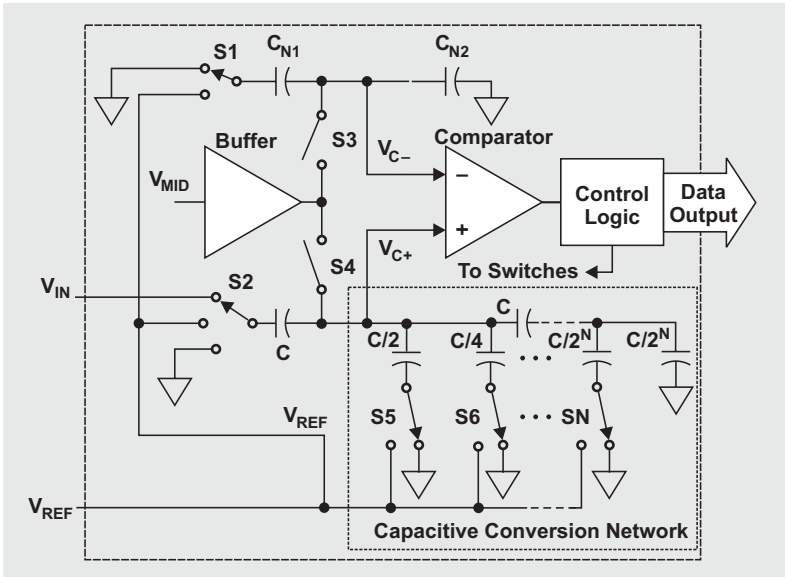
Dynamic performance

The total system noise from the circuit in Figure 1 is a combination of the inherent ADC noise, the noise from the analog input-buffer circuitry, and the reference input-voltage noise. Figure 4 shows a simplified internal circuit of a SAR ADC.

To determine the dynamic performance of an ADC, a fast Fourier transform (FFT) plot of the converter's output data can be used. An FFT plot can be calculated from a consistent clocked series of converter outputs. The FFT plot provides the SNR, the noise-floor level, and the spurious-free dynamic range (SFDR). In the example application circuit, only the SNR specification is of interest. Figure 5 provides an FFT plot of these specifications.

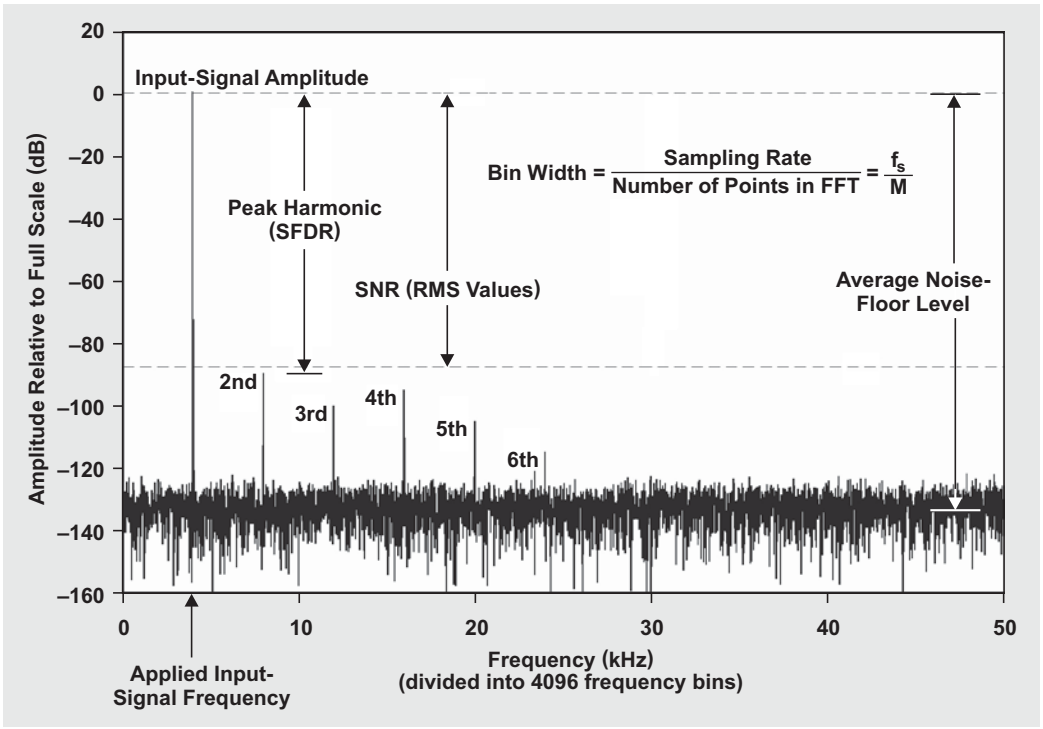
A useful way of determining noise in an ADC circuit is to examine the SNR (see Figure 5). The SNR is the ratio of the root mean square (RMS) of the signal power to the RMS of the noise power. The SNR of the FFT calculation is a combination of several noise sources, which may include the ADC quantization error and the ADC internal noise. Externally, the voltage reference and the reference driving amplifier contribute to the overall system noise. The theoretical limit of the SNR is equal to 6.02n + 1.76 dB, where n is the number of ADC bits.

Figure 4. Simplified topology of a SAR ADC



The total harmonic distortion (THD) quantifies the amount of distortion in the system. THD is the ratio of the root sum square (RSS) of the powers of the harmonic components (spurs) to the input-signal power. For example, in Figure 5, the harmonic components are labeled "2nd" through "6th." An RSS calculation is also known as the

Figure 5. FFT plot with 8192 data samples from a 16-bit converter



square root of the sum of the squares of several values. Spurs resulting from the nonlinearity of the ADC appear at whole-number multiples of the input signal's frequency (the fundamental frequency). Most manufacturers use the first six to nine harmonic components in their THD calculations.

If the ADC creates spikes in the FFT plot, it is probable that the converter has some integral nonlinearity errors. Additionally, spurs can come from the input signal through the signal source or from the reference driving amplifier. If the driving amplifier is the culprit, the amplifier may have crossover distortion; or it may be marginally stable, slew-rate-limited, bandwidth-limited, or unable to drive the ADC. Injected noise from other places in the circuit, such as digital-clock sources or the frequency of the mains, can also contribute spurs to the FFT result.

The combination of the converter's SNR and THD can be used to determine the signal to noise and distortion (SINAD) of the device. Many engineers refer to SINAD as "THD plus noise" or "total distortion." SINAD is an RSS calculation of the SNR and THD; i.e., it is the ratio of the fundamental input signal's RMS amplitude to the RMS sum of all other spectral components below half the sampling frequency (excluding DC). While the SAR converter's theoretical minimum for SINAD is equal to the ideal SNR, or 6.02n + 1.76 dB, the working SINAD is

$$\text{SINAD (dB)} = -20\log\sqrt{10^{-\text{SNR}/10} + 10^{\text{THD}/10}}. \qquad \textbf{(5)}$$

SINAD is an important figure of merit because it provides the effective number of bits (ENOB) with a simple calculation:

$$\text{ENOB} = \frac{\text{SINAD} - 1.76\text{ dB}}{6.02} \qquad \textbf{(6)}$$

In an FFT representation of converter data, the average noise floor (see Figure 5) is an RSS combination of all the bins within the FFT plot, excluding the input signal and signal harmonics. The number of samples versus the number of ADC bits can be chosen so that the noise floor is below any spurs of interest. With these considerations, the theoretical average FFT noise floor (in decibels) is

$$\text{FFT Noise Floor} = 6.02\text{n} + 10\ \log\left(\frac{3\text{M}}{\pi \times \text{ENBW}}\right),$$

where M is the number of data points in the FFT, and ENBW is the equivalent noise bandwidth of the FFT window function. A reasonable number of samples for the FFT of a 12-bit converter is 4096, which will result in a theoretical noise floor of –107 dB.

Conclusion

The ADC specifications that impact the application circuit in Figure 1 are gain error, transition noise, and SNR. Part 2 will examine the voltage reference's DC accuracy and noise contribution to the system performance.

References

For more information related to this article, you can download an Acrobat® Reader® file at www-s.ti.com/sc/techlit/*litnumber* and replace "*litnumber*" with the **TI Lit. #** for the materials listed below.

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2. Miroslav Oljaca and Justin McEldowney, "Using a SAR Analog-to-Digital Converter for Current Measurement in Motor Control Applications," Application Report	sbaa081
3. Rick Downs and Miro Oljaca. Designing SAR ADC drive circuitry, Parts I – III. *EN-Genius Network: analogZONE: acquisitionZONE* [Online]. Available: http://www.analogzone.com/acqt*0000*.pdf (Replace "*0000*" with "0221" for Part I, "1003" for Part II, or "0312" for Part III.)	—
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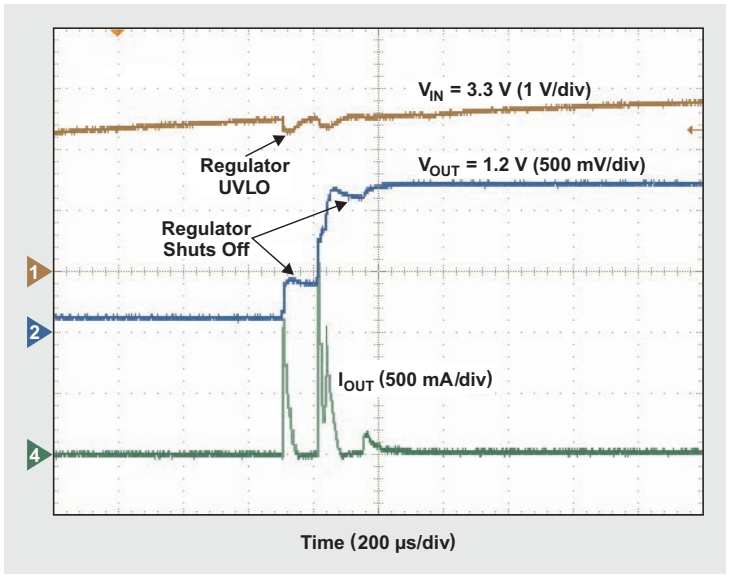
Taming linear-regulator inrush currents

By Jeff Falin
Senior Applications Engineer

Many older linear regulators and some regulators specifically designed for fast start-up require significant inrush current at start-up to charge their output capacitors and to provide current to their resistive loads. The relationship $I_{Inrush} = C_{OUT} \times V_{OUT}/t_{Rise}$ predicts the regulator's required input current at start-up for a given rise time, t_{Rise}, where C_{OUT} is the regulator's output capacitance. With no inrush-control (commonly called "soft-start") circuitry, I_{Inrush} is clamped to the regulator's current limit, which is typically significantly higher than the regulator's rated current. If the input power supply is current-limited or connected by long inductive traces, the voltage at the regulator's input will droop, possibly below that of the regulator's undervoltage lockout (UVLO) circuit. Figure 1 illustrates how this causes the regulator to "stair step" or ratchet its way up to regulation, shutting down momentarily while the input capacitor recharges, then starting up again.

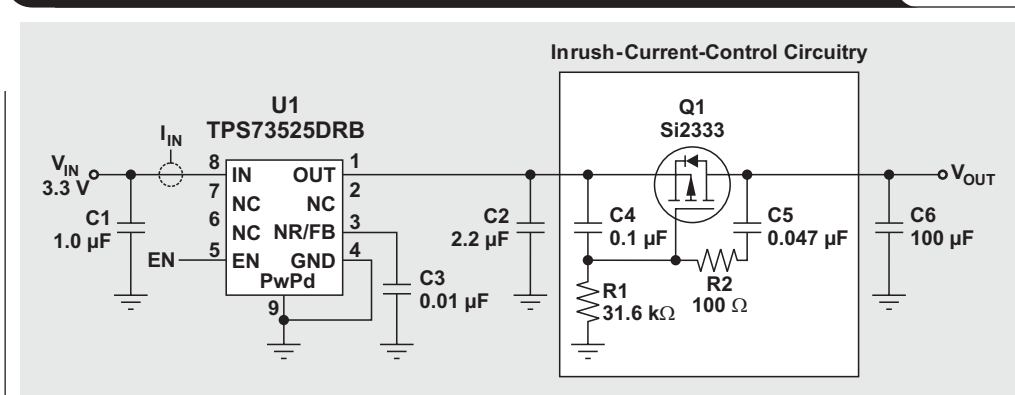
Figure 1. Older regulator with 2.5-V UVLO ratcheting up to regulation with no load



In the past, start-up problems were common for linear regulators and can still occur when the output capacitance seen by the regulator is large. End-equipment designers need to take into account how linear regulators handle inrush current, especially if the selected regulator has no inrush-current control other than clamping to its current limit.

Additional circuitry can be configured to manage inrush current for any regulator or converter. Simply by adding a FET and some passive elements following the regulator's or converter's output voltage, the designer can shape the FET's turn-on characteristic and the output-voltage waveform. For example, a designer has minimal control over the inrush current of linear regulators designed for fast start-up, like the Texas Instruments (TI) TPS734xx/5xx, which have a high power-supply ripple rejection (PSRR), low noise, and an ultralow I_q. Figure 2 shows how adding a FET and some passive circuitry to the TPS73525 provides greater control over the inrush current. I_{IN} is measured between the regulator input pin and the input capacitor because both the capacitor and the input power supply will supply the inrush current.

Figure 2. FET following the TPS73525 to provide inrush-current control



Note that in Figure 3 the amplitude and duration of the initial current spike are significantly reduced compared to those in Figure 4 because the output sees only the 2.2-µF capacitor instead of the 100-µF capacitor. Surprisingly, capacitor C5, providing additional FET gate-to-drain capacitance, and resistor R1 set the soft-start time. Reference 1 explains in detail how the additional circuit works, how to choose the FET, and how to size the passive elements.

Some regulators use a topology that has inherent inrush-current control. For example, the TI TPS732xx/4xx/6xx family of linear regulators has an internal charge pump that is needed to drive the gate of the n-channel pass element. At start-up, the charge pump needs a finite amount of time—several hundred microseconds—to charge the internal servo capacitor, which in turn charges the n-FET's gate capacitance. Figure 5 shows the TPS73633 output voltage and inrush current at start-up with C_{OUT} = 1 µF and 10 µF.

Even though these linear regulators have an 800-mA maximum current limit, the inrush current never exceeds 150 mA, after a brief spike to 300 mA, even with a 10-µF output capacitor.

From the relationship $I_{Inrush} = C_{OUT} \times V_{OUT}/t_{Rise}$, and by comparing the output voltage rise times in Figures 4 and 5, one can see that there is an inverse relationship between the output-voltage ramp time and the inrush current. Therefore, in recent years, IC manufacturers have developed linear regulators with user-controllable V_{OUT} ramp time (soft start), not only to manage inrush current but also to meet the power-rail ramp-time requirements of certain DSPs and FPGAs. The simplest integrated soft-start method, used by the TI TPS74x01 family of regulators, is

Figure 3. TPS73525 starting up into 100 µF without FET

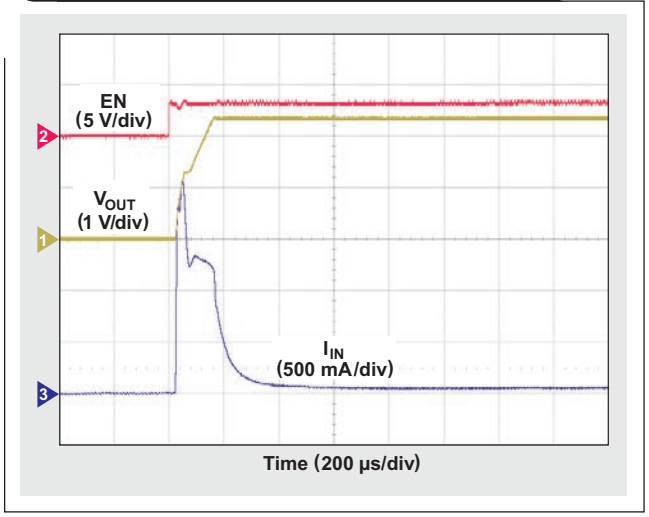


Figure 4. TPS73525 starting up into 100 µF with inrush-current-control FET

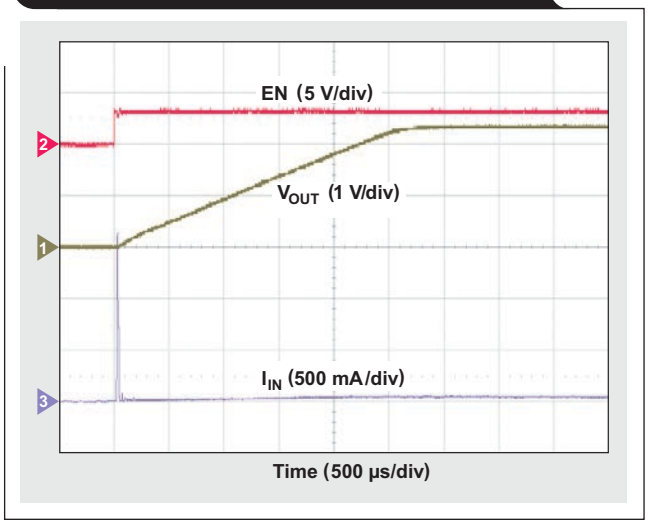


Figure 5. TPS73633 starting up with C_{OUT} = 1 µF and 10 µF

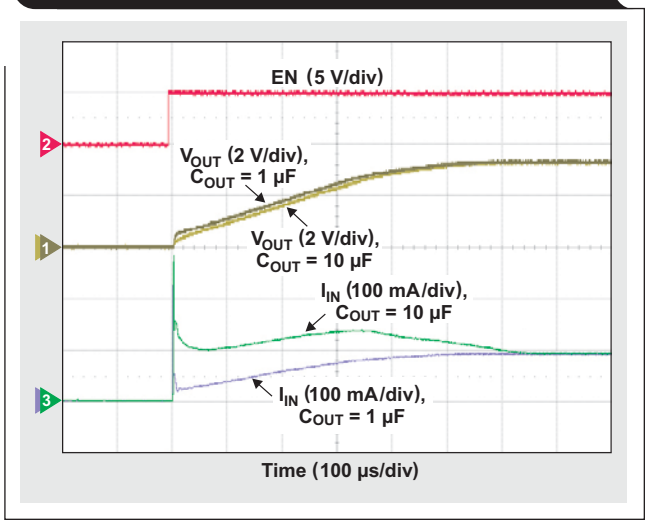


Figure 6. TPS74901 soft starting with C_{SS} = 560 pF and 2200 pF, and C_{OUT} = 10 µF

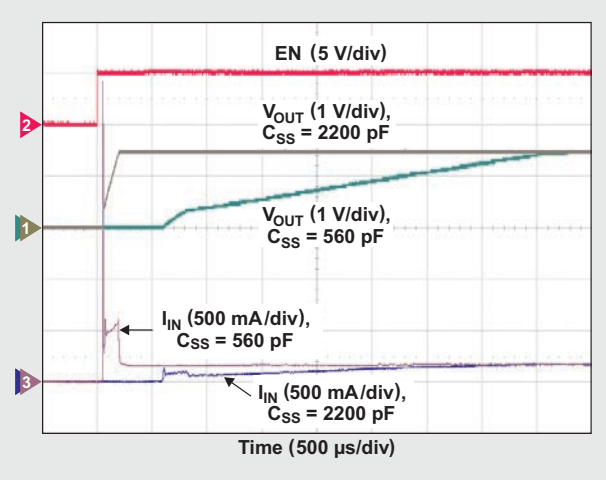
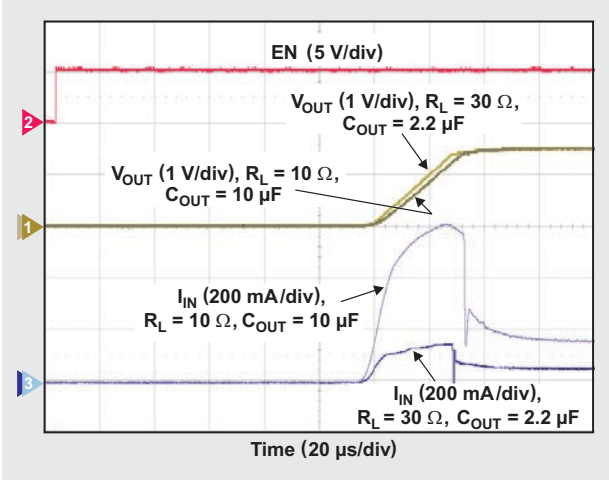


Figure 7. TPS72015 starting up at different loads (R_L)



to slowly ramp the error amplifier's internal reference voltage following an enable signal. The IC uses an external capacitor (C_{SS}) on the soft-start pin and an internal constant-current source (I_{SS}) to linearly charge this capacitor, which is initially tied to the regulator's error amplifier. Once the capacitor is charged to the same value as the internal reference voltage, V_{REF}, the IC switches the error-amplifier connection to the internal reference. Therefore, without affecting regulation, the designer can set the soft-start time as predicted by a simple equation, $t_{SS} = V_{REF} \times C_{SS}/I_{SS}$, by adjusting the capacitor value. Figure 6 shows the TPS74901 output voltage and current at start-up, with two different soft-start capacitors and C_{OUT} = 10 µF.

This soft-start method is very common and works as predicted for start-up loads that are primarily capacitive and not resistive. When the start-up load has resistive loading, the method still works, but the ramp (soft-start) time is a bit longer than predicted by the t_{SS} equation.

TI's low-I_q, dual-rail, 350-mA TPS720xx linear regulator addresses simultaneous capacitive and resistive loads with a novel, internal architecture that limits inrush current. Instead of being clamped to an overcurrent-limit value as with older regulators, the current drawn from the input to the output is limited to a lower value,

$$I_{Inrush_Limit} = I_{R_L} + C_{OUT}\ (\mu F) \times 0.0455\ (V/\mu s),$$

where I_{R_L} is the start-up resistive loading. Figure 7 shows the TPS72015 starting up at different fixed resistive loads with C_{OUT} = 2.2 µF and 10 µF. The soft-start circuitry scales the soft-start current proportionally with C_{OUT} so that the start-up time is virtually independent of C_{OUT}.

Conclusion

Historically, design engineers chose linear regulators for their low cost, simplicity, low noise, and high PSRR. Rarely did engineers consider a regulator's ability to control inrush current at start-up until after the choice was made. This oversight sometimes rendered the input power supply unable to supply enough start-up current, especially if the regulator had a large output capacitance. To continue going forward, designers had to use external circuitry to provide inrush-current control. Today, however, they can choose from a new generation of linear regulators with integrated soft start/inrush-current control. Taking soft start into consideration early in the design phase provides a problem-free system with controlled, predictable inrush current at start-up.

References

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Document Title **TI Lit. #**

1. Jeff Falin, "Monotonic, Inrush Current Limited Start-Up for Linear Regulators," Application Report. slva156

Related Web sites

power.ti.com
www.ti.com/sc/device/*partnumber*
Replace *partnumber* with TPS72015, TPS73525, TPS73633, or TPS74901

Designing a linear Li-Ion battery charger with power-path control

By Charles Mauney
Senior Systems/Applications Engineer,
Battery Management and Charging Solutions

In theory, a linear battery charger with a separate power path for the system is a fairly simple design concept and can be built with an LDO adjusted to 4.2 V; a current-limit resistor; three p-channel FETs to switch the system load between the input power and the battery source; and some bias parts. In reality, there is much more to a good design than the basic topology. This article will discuss dynamic power-path management (DPPM) and explore safety features that turn a basic topology into a complete design.

The DPPM topology is shown in Figure 1 and has two power-source pins, V_{IN} and V_{BAT}. The charger can be programmed for either a USB input or an adapter input. The design concept is to always power the system if power is available, either from V_{IN} or V_{BAT}, unless the system is programmed to shut down. The input FET regulates the output voltage and will also limit the input current to the programmed level if the load is excessive. The battery FET has control loops associated with charging the battery and allowing the battery to power the system. The input controls and battery controls act independently and are discussed in more detail later.

Figure 2 shows a charger solution with a discrete power path. The LDO provides the regulated output voltage, and the input-current-limit resistor limits the maximum current that can be delivered to the battery. D1, R1, R4, and Q1 monitor the input voltage and turn on Q2 and Q3 if input source power is present, connecting the input to the system load. If input source power is not present, Q5 and Q4 are biased on so the battery will provide power to the system load. This state will hereinafter be referred to as "battery-supplement mode."

Figure 1. Power-path topology of battery charger

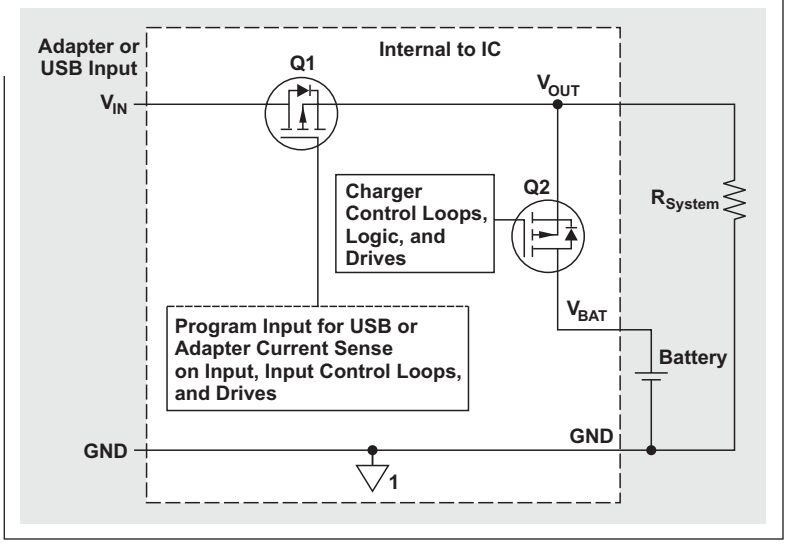
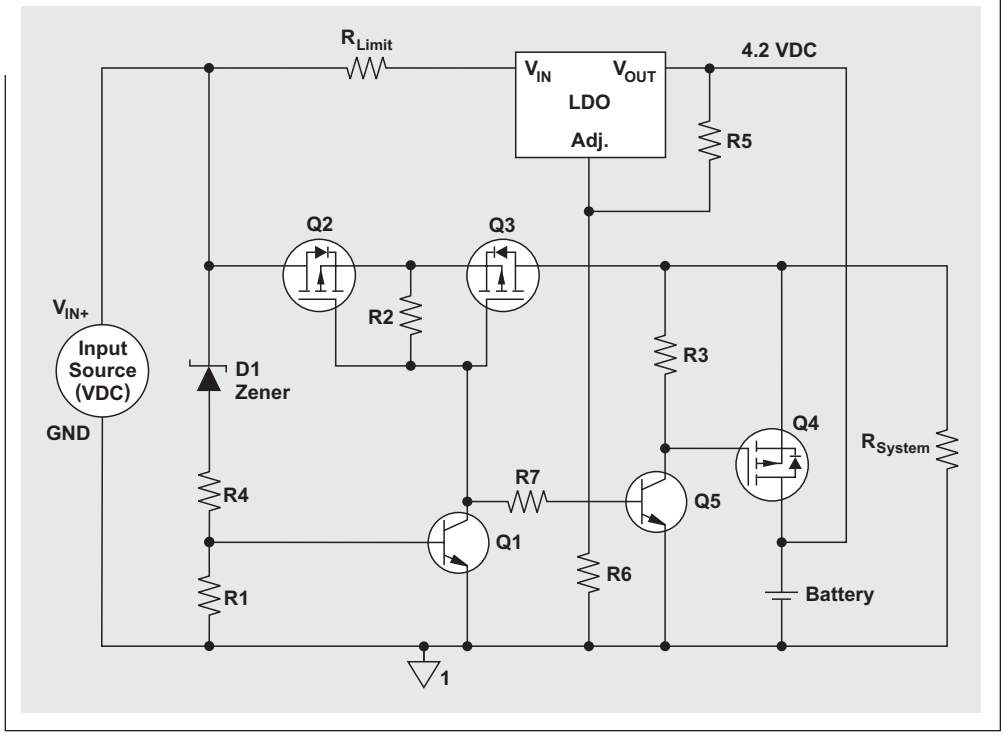
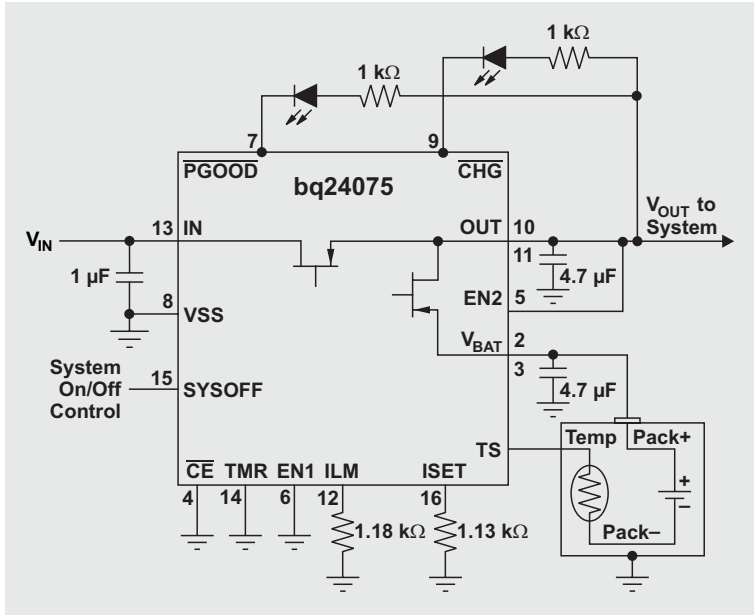


Figure 2. Discrete charger with battery-supplement mode



This charger solution is simple and discrete but has many limitations and few safety features. Adding any safety feature will quickly drive up the solution cost but often may offset the liability cost of an unprotected design. LDOs are typically not highly accurate regulators, especially with external programmable resistors. If the regulation was set lower to ensure that the maximum battery voltage was not exceeded, the typical voltage and capacity would be lower. The crude current-limit resistor would allow more current at lower battery voltages and would not provide a conditioning current to help recover depleted cells or to prevent cell damage from excessive charging.

Figure 3. Typical integrated application with bq24075 charger



Typical integrated application

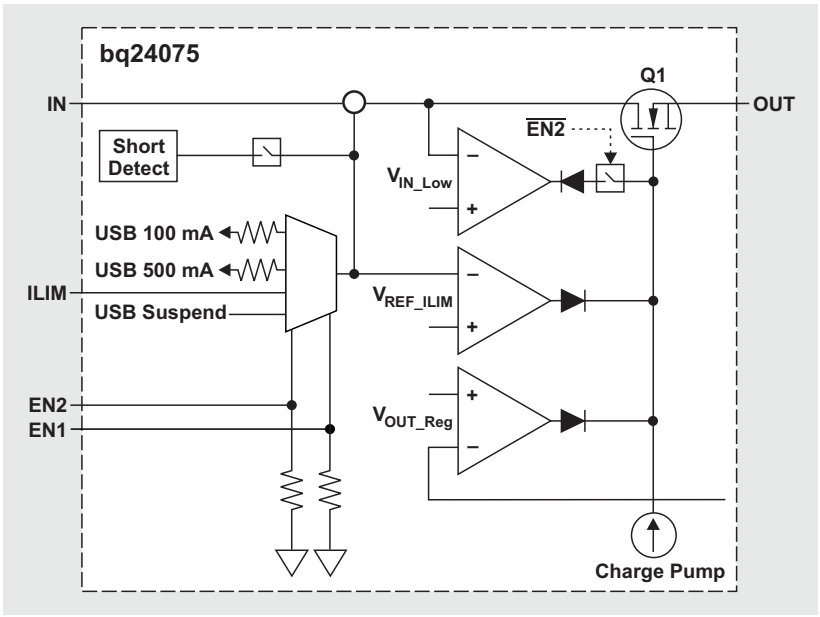
Figure 3 shows the Texas Instruments (TI) bq24075, a charger with a highly integrated power path in a 3 × 3-mm, 16-pin QFN package. The only external components required are two external programming resistors and three capacitors for the power sources.

Programmed input-source protection

The input-current limit is programmed with the EN1/2 pins to one of four states: 100 mA, 500 mA, ILIM, or Suspend, as shown in Figure 4. A resistor can be used to program ILIM at any level up to the device's maximum input current. When current-limited, the input FET restricts the current to the OUT pin, causing the system voltage to drop to the DPPM threshold or to the battery voltage where the charge current will be reduced. Assuming that the protection was designed for the applied source, this feature solves the problem of the system overloading the adapter or the USB source, which could potentially damage the source or device. More power-management details are presented later under "DPPM protection of output voltage."

If a current-limited source such as a weak or wrong adapter or USB is used, the adapter and system voltages

Figure 4. Input-FET control loops



will drop, causing the IC to enter DPPM mode or battery-supplement mode. Basing DPPM on the output voltage solves most loading issues by reducing the charge current, giving priority to the system load, and allowing operation with a weak power source or minor AC brownouts. Other input-current-management solutions without DPPM would not detect the weak source or reduce the charging current, and the system would crash.

The V_{IN_Low} input loop provides additional protection for a weak source when in USB 100/500-mA mode. This loop monitors the voltage on the USB input pin; and, if it drops to ~4.5 V, Q2 enters its linear range to keep the USB input voltage from dropping any further, as shown in Figure 5. This voltage loop is independent of the input-current-limit loop. This feature adds protection for the USB host in the event that it cannot deliver the load current because of a weak source or failed communication. In Figure 5, I_{OUT} starts with no load and, at ~250 mA, the current limit of the weak source causes the source voltage to fall to 4.5 V, where the V_{IN_Low} loop kicks in and the system output voltage drops about 100 mV to the DPPM threshold. The charge current is reduced as the load is increased to maintain the input at 4.5 V. As the load is reduced, the system returns to normal operation.

DPPM protection of output voltage

The output voltage powering the system will drop if the system load current and the battery charge current exceed the available input current. The input current can be restricted by the source, the V_{IN_Low} loop, or the input-current-limit setting of the IC. If the output voltage drops to the DPPM threshold, the charge current will be reduced to keep the voltage from further decay. This allows the use of a less expensive adapter because the charging current is reduced during peak loads.

If the system current exceeds the available input current, the output voltage will drop to the battery voltage and enter battery-supplement mode, in which the battery FET turns on and supplements the input current going to the system. This allows use of the battery to supplement large current pulses to the system, which the charger is not capable of supplying. Figures 6 through 8 show the waveforms of the TI bq24072/3/4/5 where the output voltage drops first into DPPM mode and then into battery-supplement mode.

Figure 6 shows the waveforms of the bq24072 with V_{OUT} initially regulated to about 225 mV above the battery voltage. Upon reaching the input-current limit after the first load step, the IC enters DPPM mode, which reduces the charge current to keep the output voltage from dropping below the DPPM threshold. After the second load step, the system load is greater than the input limit. The output voltage drops to just below the battery voltage, and the battery FET turns on and supplements the input current to the system load. Note that the voltage transitions between modes are very small and are best for applications that are sensitive to voltage changes.

Figure 5. V_{IN_Low} USB protection with source-current limit at 250 mA

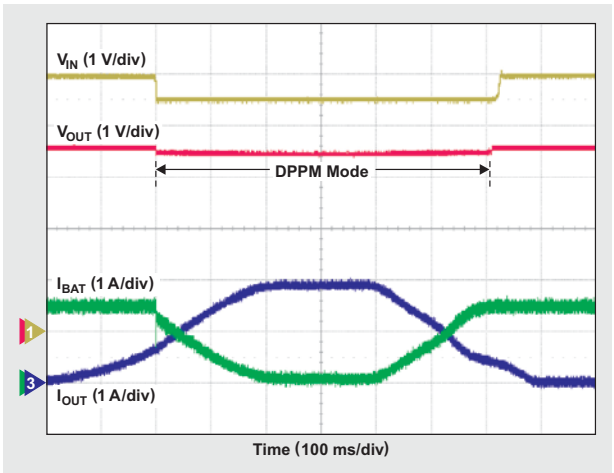
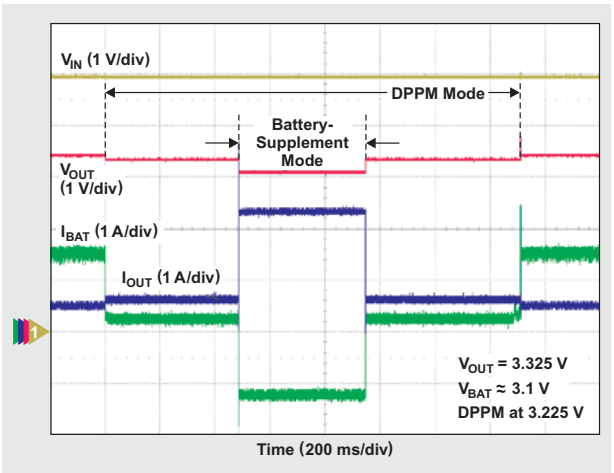


Figure 6. bq24072 DPPM and battery-supplement modes with $V_{BAT} \approx 3.1$ V



The waveforms of the bq24073/4 in Figure 7 were generated under the same conditions as for the bq24072 in Figure 6, except that the bq24073/4 regulates V_{OUT} at 4.4 V and the DPPM threshold at 4.3 V. Upon entering battery-supplement mode, the output voltage drops to just below the battery voltage; so the lower the battery voltage is, the larger the drop. For an application sensitive to system voltage drops, the system load should not exceed the available input current in order to stay out of battery-supplement mode. An alternative is to use the bq24072.

The bq24075 waveforms in Figure 8 were generated under the same conditions as for the bq24072 in Figure 6, except that the bq24075 regulates V_{OUT} at 5.5 V and the DPPM threshold at 4.3 V. The transition between modes is larger and dependent on the input voltage and battery voltage. If the input voltage is less than 5.5 V, then the regulator is switched fully on to deliver what voltage is available.

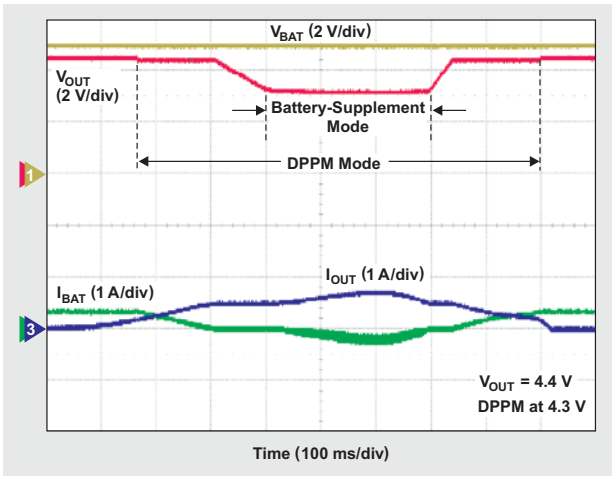
Protection from shorting system V_{OUT}

Shorting the V_{OUT} pin can cause excessive current from the battery or the V_{IN} power source. Battery short-circuit protection disables the battery FET if the voltage drop from V_{BAT} to V_{OUT} is greater than 250 mV for a duration longer than the specified deglitch time. The battery FET is turned on periodically to check whether the short is still present, and this hiccup mode will continue until the short is removed. This prevents damage to the IC and solves reliability issues.

For V_{IN} protection, the input FET limits the input current to 100 mA when the output voltage is less than 1 V. Once the excessive load is removed, the output will charge above 1 V and start delivering the programmed input current. This feature reduces the power dissipation during the output short, which also improves reliability. Figure 9 shows the waveforms of an output short and the IC's recovery.

Figure 9 shows the waveforms that occur when the bq24072's output is shorted, causing the battery FET and input FET to turn off. The input source supplies about 90 mA to the output via the input control loop; and, approximately every 64 ms, the battery FET is turned on for 250 µs to check whether the short is still present.

Figure 7. bq24073/4 DPPM and battery-supplement modes with V_{OUT} = 4.4 V



Picking the right charger IC

The bq24072/3/4/5 ICs all charge a single-cell Li-Ion battery properly, but they have various values for the overvoltage-protection (OVP) threshold, the V_{OUT} regulation, and the DPPM threshold (see Table 1). Each IC also has an

Figure 8. bq24075 DPPM and battery-supplement modes with V_{OUT} = 5.5 V

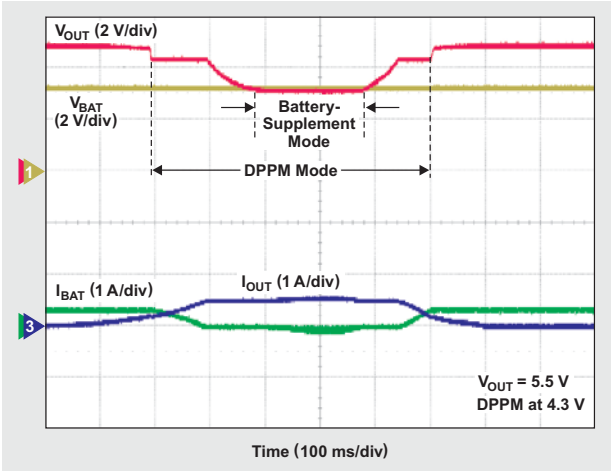


Figure 9. Output short-circuit protection

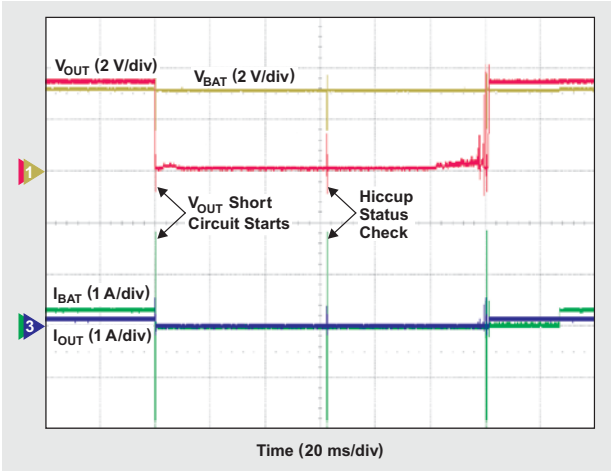


Table 1. Differences between bq24072/3/4/5 ICs

DEVICE	V_{OVP}	V_{OUT}	V_{DPPM}	OPTIONAL FUNCTION
bq24072	6.6 V	V_{BAT} + 225 mV	$V_{O(REG)}$ – 100 mV	TD
bq24073	6.6 V	4.4 V	$V_{O(REG)}$ – 100 mV	TD
bq24074	10.5 V	4.4 V	$V_{O(REG)}$ – 100 mV	ITERM
bq24075	6.6 V	5.5 V	4.3 V	SYSOFF

optional control function such as termination disable (TD), programmable termination current (ITERM), or system off (SYSOFF). The 10.5-V OVP is for a nonregulated 5-V adapter where the unloaded source is above 6.6 V. To minimize power dissipation, during fast charge the optimum input voltage should be between 4.5 and 5.5 V.

The bar chart in Figure 10 shows graphically how the charger output voltage changes from one operational mode to another for each charger. If the system is sensitive to changes in the output voltage and the peak system load exceeds the input current, the bq24072 minimizes these changes since it regulates the output voltage to within 225 mV of the battery voltage. The bq24073/4 regulates the output voltage to 4.4 V and the DPPM threshold to 4.3 V. Depending on the battery voltage, the voltage drop can be large when the charger enters battery-supplement mode. The bq24075 regulates the output voltage to 5.5 V for inputs greater than 5.5 V and passes through lower voltages. If the charger output current plus the charge current exceed the input current, the output voltage will drop much more than 100 mV, as shown in Figure 10. A further increase in output current may put the device in battery-supplement mode, where another large drop will occur.

Figure 11 shows the efficiency of the power topology. Efficiency for a linear topology is

$$\eta = \frac{V_{IN} - V_{OUT}}{V_{IN}} \times 100.$$

Each charger mode has an efficiency factor. For the bq24072/3/4/5, the efficiency during battery-supplement mode is the same given the same input voltage and battery voltage.

The bq24072 has the least change in output voltage between modes, but the efficiency drops as the battery discharges. The bq24073/4 is more efficient in normal and DPPM modes but may have a larger internal voltage drop upon entering battery-supplement mode. The bq24075 has high efficiency in normal mode and good efficiency in DPPM mode, but it may have a large change in output voltage after switching from normal to DPPM to battery-supplement mode.

Figure 10. Output voltage with changes in operational mode and part number (V_{IN} = 5 V)

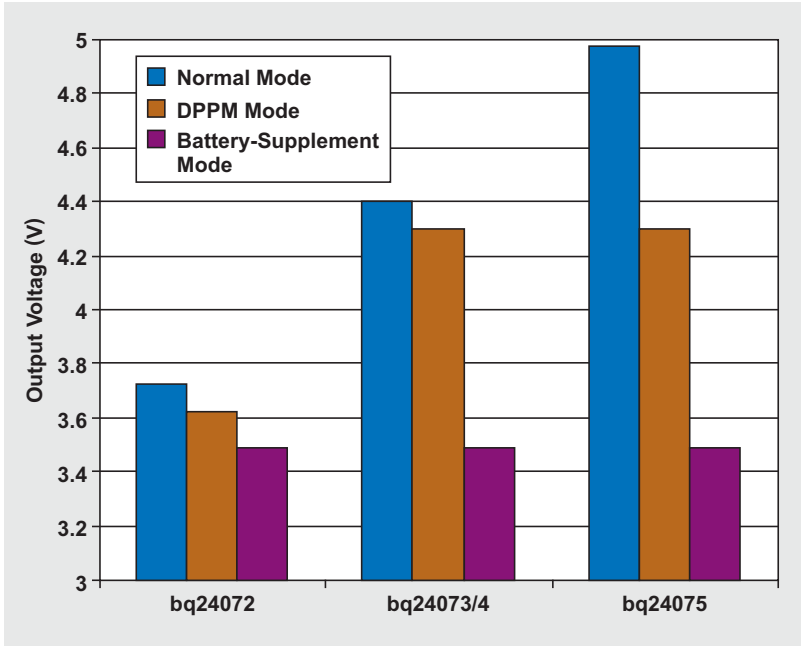
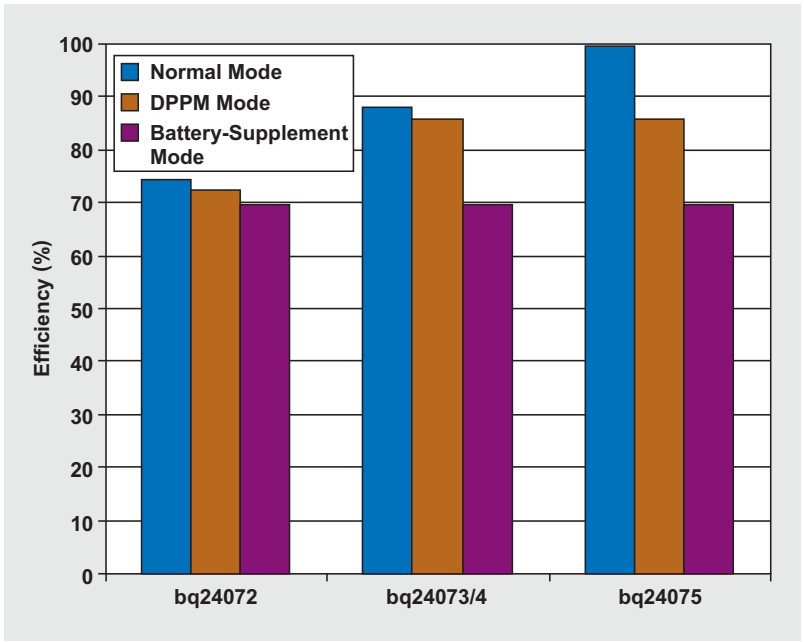


Figure 11. System efficiency with changes in operational mode and part number (V_{IN} = 5 V. For V_{OUT}, see Figure 10.)



The decision for the designer is whether the charger should be sensitive to system voltage changes, have lower efficiency, or both. If the charger is sensitive to voltage changes, will the system operations cause changes between the modes with large voltage steps? Because of the low power drain from the adapter or USB source, efficiency is not typically a cost concern, but it can be a heat-dissipation issue in the device.

Simple, single-cell, integrated Li-Ion chargers

For designs where power-path control is not necessary, the TI bq2401x, bq2402x, and bq2406x families of single-cell Li-Ion chargers perform complete charging with all the necessary safety features.

The bq2406x family incorporates many of the same features found in the bq24072/3/4/5 family, but without the power-path management. The bq2406x performs standard three-phase charging—battery conditioning, constant current, and voltage regulation—followed by termination. The safety features include input OVP, a precharge safety timer, a fast-charge safety timer, and IC thermal regulation. The OVP circuit disables the input pass FET if the input voltage exceeds the OVP threshold. This helps to protect against wrong or damaged power sources. The safety timers, once expired, will disable charging. Typically, if the design is done properly, a good battery will exit precharge or reach termination long before the safety timers declare a fault. Typically intended for operation in extremely hot environments where the IC junction temperature reaches 125°C, the thermal-regulation loop reduces the charge level to prevent further heating of the charger IC. Further details on these features can be found in the data sheet.

Conclusion

An inexpensive discrete charger can be implemented that performs the charging and manages basic power-path connections but does not address any of the safety and reliability issues that may occur. A brief description has been given of the safety features of a simple charger, followed by a more detailed description of DPPM. The bq24072/3/4/5 chargers provide three levels of input-current-limiting protection that can be programmed to protect the specified source. The USB V_{IN_Low} loop provides additional protection by detecting weak USB sources and restricting the input current. The output DPPM loop reduces the charging current at the first sign of a drop in the system voltage and enters battery-supplement mode if the system load exceeds what the adapter can handle. This article has also discussed how the IC protects against a system short circuit and then recovers. Finally, for each part number in the bq24072/3/4/5 family, changes in output voltage and efficiency that occur with changes in operational mode were compared.

The bq24072/3/4/5 family of Li-Ion battery chargers is a fully integrated solution that performs Li-Ion charging and DPPM and reduces application size. It solves many issues with power sources by allowing use of less expensive adapters, managing loading, giving priority to the system, increasing reliability, and incorporating many safety features for a lower total system price.

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Replace *partnumber* with bq24010, bq24020, bq24060, bq24072, bq24073, bq24074, or bq24075

Selecting the right charge-management solution

By Masoud Beheshti
Director/Product Line Manager

Introduction

Today's designers of portable devices have choices of many types of battery chemistries, charger topologies, and charge-management solutions. Selecting the right solution should be simple, but in most cases it is a bit complicated. The designer needs to strike a balance between performance, cost, form factor, and other key requirements. This article provides an overview of several portable-power solutions.

The three C's of charge management

Charge management is a critical function in any portable design utilizing rechargeable batteries. Sound design techniques ensure that requirements for the following three considerations are met (see Table 1):

1. *Cell safety*—This is not limited to a simple requirement like, for example, meeting the voltage-regulation tolerance of ±1% during the final phase of charge for a Li-Ion battery. Safety functions also include safety timers, cell-temperature monitoring, and a preconditioning mode to safely handle deeply discharged cells.
2. *Cell capacity*—Any charge-management solution needs to ensure that the batteries are charged to full capacity in every cycle. Early charge termination results in reduced run time and is not desirable in today's power-hungry portable devices.
3. *Cell cycle life*—Adhering to the recommended charge algorithm is an important step towards ensuring that the end user gets the maximum number of charge cycles from each pack. Qualifying each charge with the cell temperature and voltage, preconditioning deeply discharged cells, and avoiding late or improper charge termination are some of the steps necessary for maximizing cycle life.

Managing battery-chemistry requirements

System designers today have the option to select from a variety of battery chemistries. The selection is typically based on a number of criteria, including energy density; size and form factor; cost; and usage pattern and cycle life. Although there has been a strong trend towards Li-Ion and Li-Pol chemistries in recent years, the NiCd and NiMH chemistries are still viable options for a variety of consumer applications.

Table 1. The three C's of charge management

CHARGE FEATURE	CELL SAFETY	CELL CAPACITY	CELL CYCLE LIFE
Accurate voltage and/or current regulation	✔	✔	
Charge qualification (voltage and temperature)	✔		✔
Temperature monitoring	✔	✔	✔
Preconditioning	✔	✔	✔
End-of-charge termination	✔	✔	✔
Charge timer	✔		
Charge-status reporting	✔	✔	
Detection of battery insertion and removal	✔		
Minimal battery drainage		✔	
Short-circuit current limit	✔		
Automatic recharge		✔	

Regardless of the choice of chemistry, it is critical to adhere to the appropriate charge-management techniques for each chemistry. These techniques ensure that batteries are charged to their maximum capacities in every cycle without compromising safety or cycle life.

NiCd/NiMH

Before a fast-charge cycle starts, NiCd and NiMH batteries must be qualified and possibly conditioned. Fast charge is prohibited if the battery voltage or temperature is outside the allowed limits. For safety, any charging of a "hot" battery (typically above 45°C) is suspended until the battery cools to the normal operating-temperature range. To condition a "cold" battery (typically below 10°C) or an over-discharged battery (typically below 1 V per cell), a gentle trickle current is applied.

Fast charge begins when the battery temperature and voltage are valid. NiMH batteries are typically charged with a constant current of 1C or less. Certain NiCd batteries can be charged at rates of up to 4C. Proper charge termination is required to prevent harmful overcharge.

For nickel-based rechargeable batteries, fast-charge termination can be based on either voltage or temperature.

As shown in Figure 1, a typical voltage-termination method is peak-voltage detection (PVD), where fast charging is terminated within a range of 0 to –4 mV per cell of the peak cell voltage. The temperature method monitors the rate of battery temperature rise, ΔT/Δt, to detect full charge. The typical ΔT/Δt rate is 1°C/minute.

Li-Ion/Li-Pol

Similar to NiCd and NiMH batteries, Li-Ion and Li-Pol batteries must be qualified and possibly conditioned before fast charge. A qualification and conditioning method similar to the one described earlier is used.

As shown in Figure 2, following qualification and preconditioning, a lithium-based battery is first charged with a current of 1C or less until it reaches its charge-voltage limit. This stage of charge typically replenishes up to 70% of the capacity. The battery is then charged with a constant voltage of typically 4.2 V. To maximize safety and the available capacity, the charge voltage must be regulated to at least ±1%. During this stage of charge, the charging current drawn by the battery tapers down. The charge is typically terminated once the current level falls below 10 to 15% of the initial charging current at a 1C charging rate.

Figure 1. Charge profile for NiCd/NiMH batteries

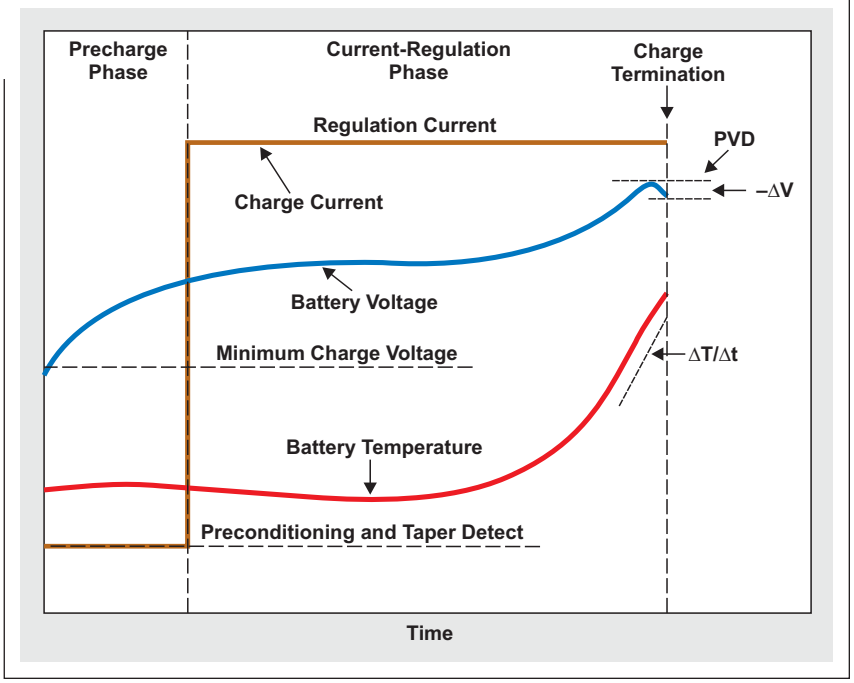
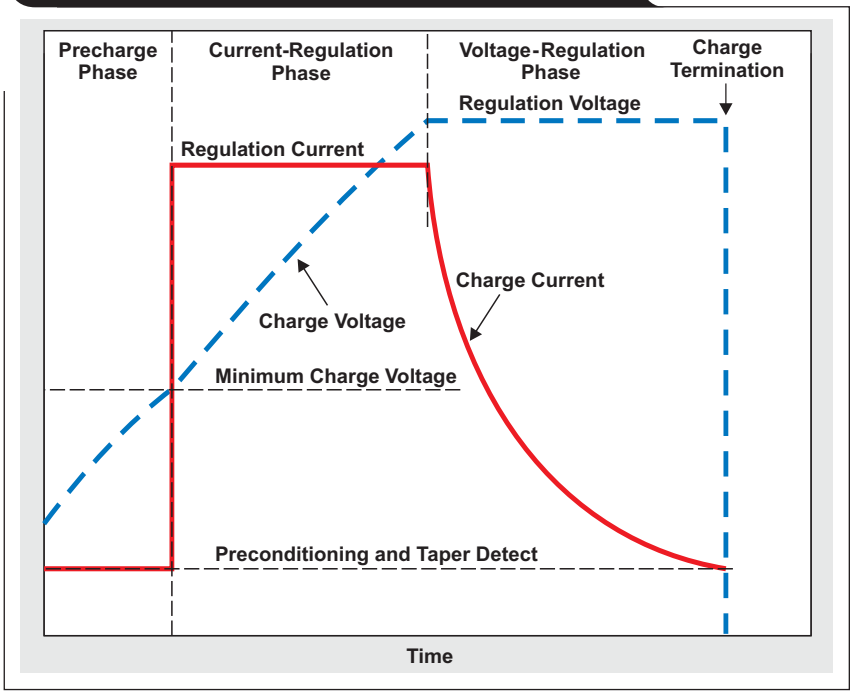


Figure 2. Charge profile for Li-Ion/Li-Pol batteries



Linear versus switch-mode charging topology

Linear and switch-mode topologies are commonly used for controlling the charging current and voltage in applications using rechargeable batteries. Each topology provides unique advantages for its intended applications.

The linear topology is well suited for low cell counts and charging currents. It offers the designer several advantages: low implementation cost, design simplicity, and "quiet" operation due to the absence of high-frequency switching. The linear topology also introduces some power dissipation into the system, in this case mostly during the current-regulation phase of the charge cycle. This is a drawback if the designer has no means to manage the thermal issues in the design.

The switch-mode topology is well suited for higher cell counts and charging currents. Its main advantage is increased efficiency. Unlike linear regulators, the power switch or switches are operated in the saturation region, which substantially reduces the overall losses. The main sources of power loss in a buck converter include the switching losses (in the power switches) and the DC losses in the filter inductor. Depending on the design parameters, it is not uncommon to see efficiencies of well over 95% in these applications.

Inductive charging

Inductive (wireless) power has been around for a long time and has found applications in many areas. In the industrial area, for instance, induction heating has provided a practical and efficient way to melt large amounts of metals in a manufacturing environment. In the consumer area, inductive power has been used successfully to charge toothbrushes and other small personal-care products. However, when it comes to charging the new generation of portable appliances such as cellular phones, portable media players, and *Bluetooth*® headsets, the use of wireless power is in its infancy.

The wireless chargers commonly used in the consumer market for devices such as toothbrushes are not optimized for efficiency or speed. These chargers "trickle charge" at a low rate, and the form factor is customized to accept only the intended end equipment. However, the demands for portable power are changing; and most consumers now own a multitude of portable devices, each with its own power cable and, in many cases, proprietary connectors. Consumers are beginning to look for the same convenience in charging their portable devices as is offered by wireless data transfer. This concept, although simple, presents a number of barriers for design solution and acceptance:

- Unlike the battery for a toothbrush, batteries for the new portable devices need to be charged at a standard fast-charge rate, reaching 70% of capacity in about an hour. The solution must therefore be very power-efficient.
- The battery for each portable device is a different size and has a different charge rate (i.e., power rating), so the concept of "one size fits all" does not apply. The wireless charger needs to have the intelligence to recognize these variations and adjust itself accordingly.
- Consumer safety is very important, so the wireless charger needs not only to differentiate between a coin and a cell phone but also to make certain that no hazardous situations are created under any operating condition.
- Ultimately, what consumers will pay for is convenience, so the wireless charger needs to be substantially easier to use than the easiest corded charger available.

There are a variety of solutions being developed to address these concerns. A great example is eCoupled™ technology developed by Fulton Innovation. This technology includes an inductively coupled power-supply circuit that dynamically seeks resonance, adapting its operation to match the needs of each device it supplies (see Figure 3). By communicating with each device individually in real time, eCoupled technology not only determines power needs but also takes into account the age of a battery or device and its charging life cycles. This supplies the optimal amount of power to the device and keeps it operating at peak efficiency.

Figure 3. Concept of inductively coupled power supply

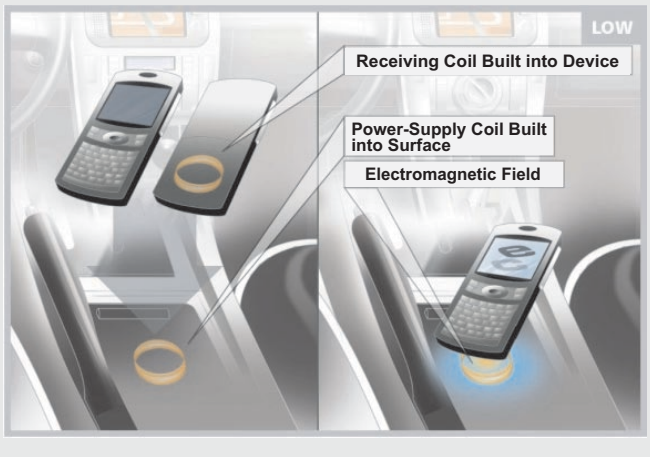
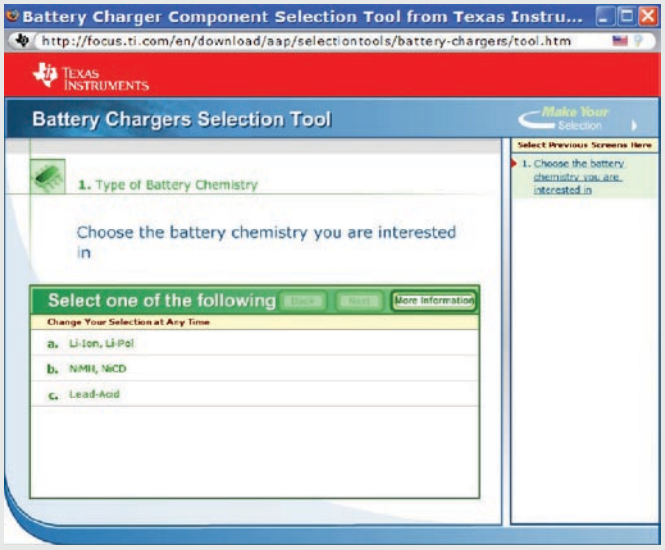


Figure 4. TI Battery Chargers Quick Search tool



Selecting the charger

Texas Instruments offers a variety of tools to make the process of selecting the right charger easier for designers. Figure 4 shows the "Battery Chargers Quick Search" tool available at power.ti.com (Scroll down to "Analog eLab™ Design Support" to view links under "Design, Simulation, and Selection Tools.")

Related Web site

power.ti.com

Designing with digital isolators

By Thomas Kugelstadt
Senior Applications Engineer

Introduction

The purpose of this article is to help engineers use the Texas Instruments (TI) ISO72xx family of digital isolators to design galvanically isolated systems in the shortest time possible. The article explains the basic operating principle of the TI isolator, suggests where to place it within a system design, and recommends guidelines for an electromagnetic-compatible (EMC) circuit-board design.

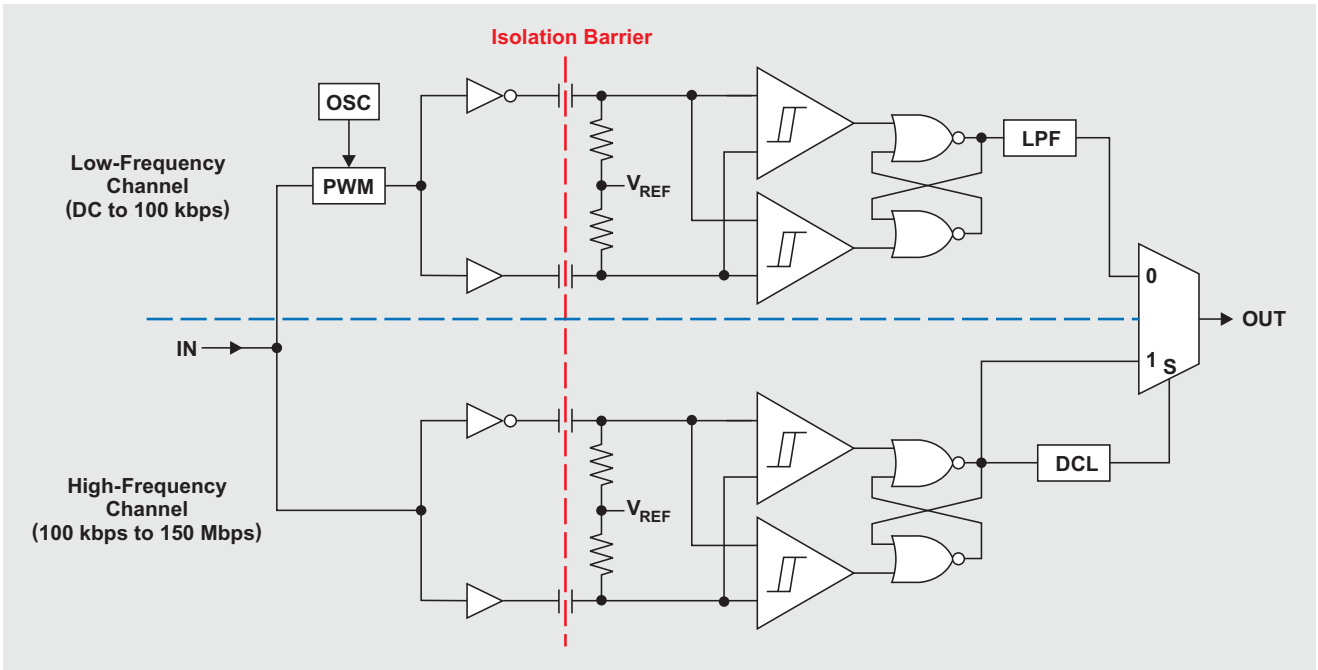
Operating principle

The isolator in Figure 1 is based on a capacitive-isolation-barrier technique. The device consists of two data channels —a high-frequency channel with a bandwidth ranging from 100 kbps up to 150 Mbps, and a low-frequency channel covering the range from 100 kbps down to DC.

In principle, a single-ended input signal entering the high-frequency channel is split into a differential signal via the inverter gate at the input. The subsequent capacitor-resistor networks differentiate the signal into transients, which are then converted into differential pulses by two comparators. The comparator outputs drive a NOR-gate flip-flop whose output feeds an output multiplexer. A decision logic (DCL) at the driving output of the flip-flop measures the durations between signal transients. If the duration between two consecutive transients exceeds a certain time limit, as in the case of a low-frequency signal, the DCL forces the output multiplexer to switch from the high- to the low-frequency channel.

Because low-frequency input signals require the internal capacitors to assume prohibitively large values, a pulse-width modulator (PWM) is used to modulate these signals with the carrier frequency of an internal oscillator (OSC), thus creating a frequency high enough to pass the capacitive barrier. As the input is modulated, a low-pass filter (LPF) is needed to remove the high-frequency carrier from the actual data before it is passed on to the output multiplexer.

Figure 1. Block diagram of a digital capacitive isolator



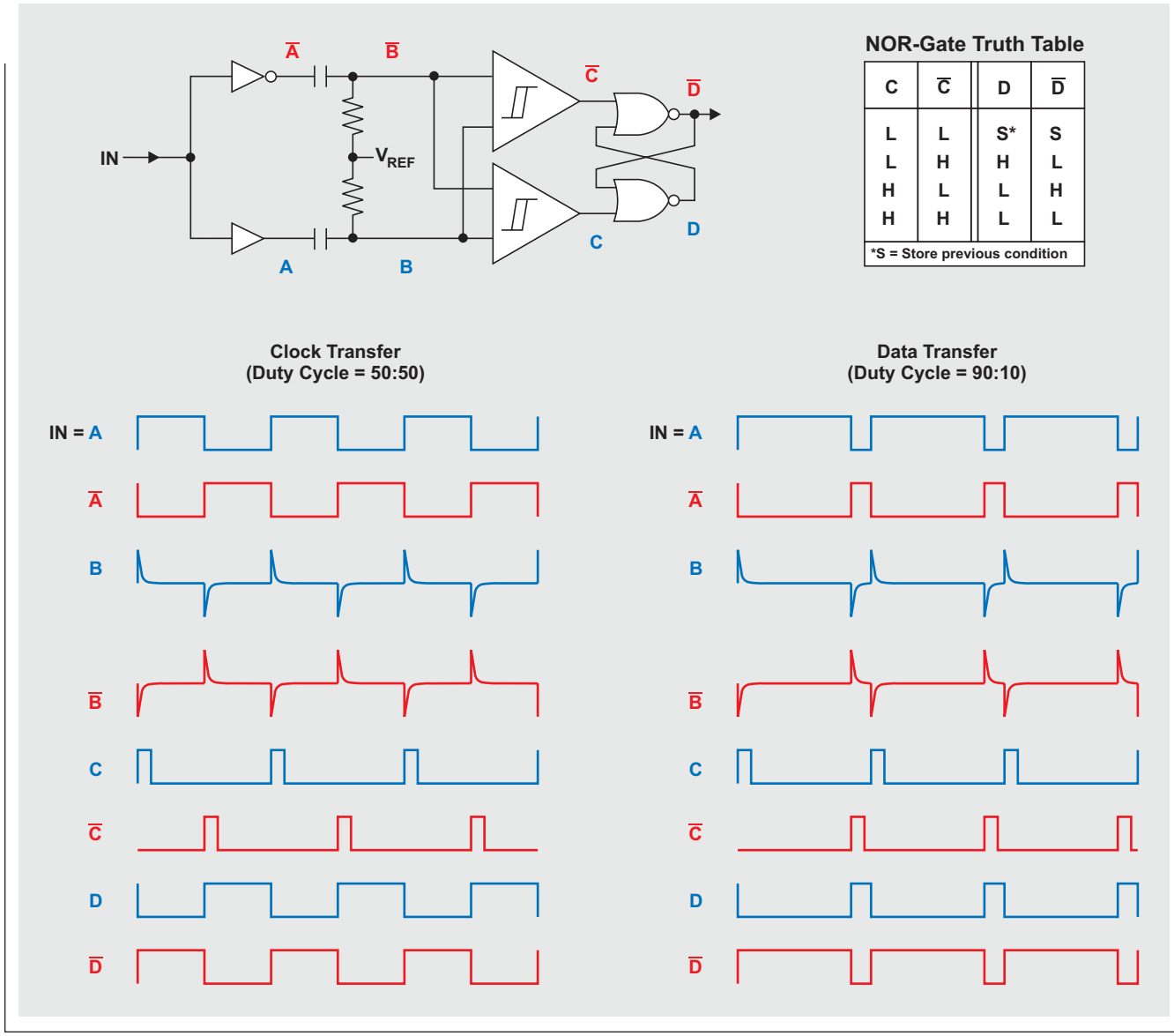
High-frequency-channel operation

Figure 2 presents the high-frequency channel and the waveforms at specific points of the signal chain. The single-ended input signal is split into the differential signal components, A and $\overline{A}$. Each signal component is then differentiated into the transients, B and $\overline{B}$. The subsequent comparators compare the differential transients to one another. As long as the positive input of a comparator has a higher potential than its negative input, the comparator output will present a logical high, thus converting an input transient into a short output pulse.

The output pulses set and reset a NOR-gate flip-flop. From the "NOR-Gate Truth Table" in Figure 2 we see that the NOR-gate configuration presents an inverting flip-flop, meaning that a high at input C sets output $\overline{D}$ to high, and a high at $\overline{C}$ sets D to high. Because the comparator output pulses are of short duration, there will be times when both outputs are low. During this time the flip-flop stores its previous output condition. Since the signal at $\overline{D}$ is identical to the input signal in shape and phase, $\overline{D}$ becomes the output of the high-frequency channel and is connected to the output multiplexer.

While input signals with symmetrical duty cycles cause equidistant pulses at the comparator outputs, asymmetrical signals (shown in the "Data Transfer" timing diagram in Figure 2) move the comparator pulses closer to each other to maintain the shape and phase relationships of the input signal.

Figure 2. Timing in high-frequency-channel operation



NOR-Gate Truth Table

C	$\overline{C}$	D	$\overline{D}$
L	L	S*	S
L	H	H	L
H	L	L	H
H	H	L	L

*S = Store previous condition

Low-frequency-channel operation

As shown in Figure 3, a PWM modulates slow input signals with a high-frequency carrier such that, at location A, a high-level input yields a 90:10 duty cycle, and a low-level input yields a 10:90 duty cycle. From there on, signal processing is identical to the asymmetrical signal processing in the high-frequency channel. The only exception is that the high-frequency content of $\overline{D}$, the low-frequency channel, is filtered by an R-C LPF before being passed on to the output multiplexer, E.

Isolator technology and requirements

The successful proof of the single isolator's ability to transmit wideband data (from DC to above 150 Mbps) inspired TI to fabricate unidirectional and bidirectional devices in dual-, triple-, and quad-channel versions that accommodate the most common digital interfaces encountered in industrial applications (see Figure 4). All TI digital isolators utilize single-ended, 3-V/5-V CMOS-logic switching technology. Their nominal supply-voltage range is specified

Figure 3. Timing in low-frequency-channel operation

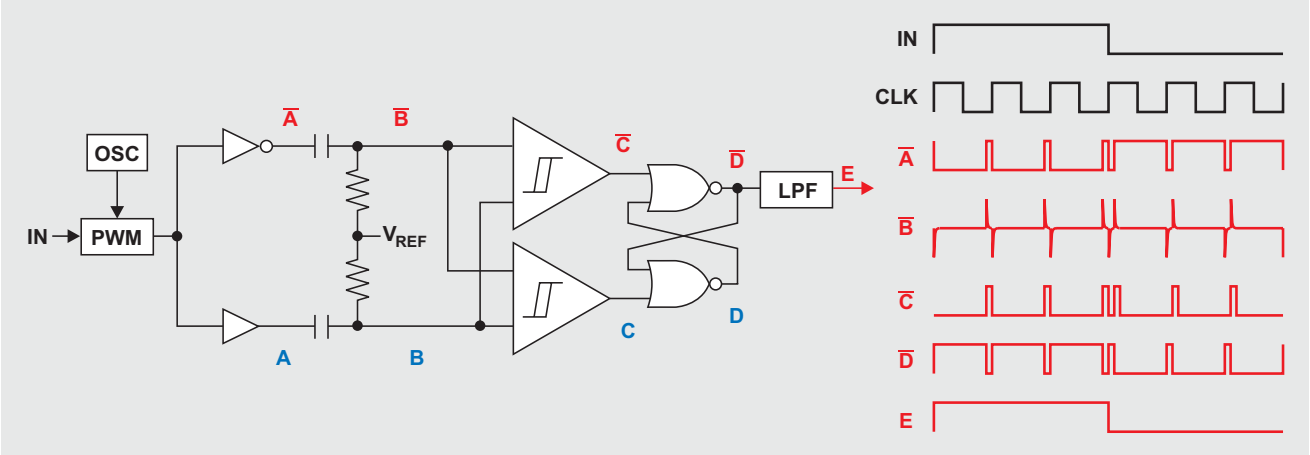
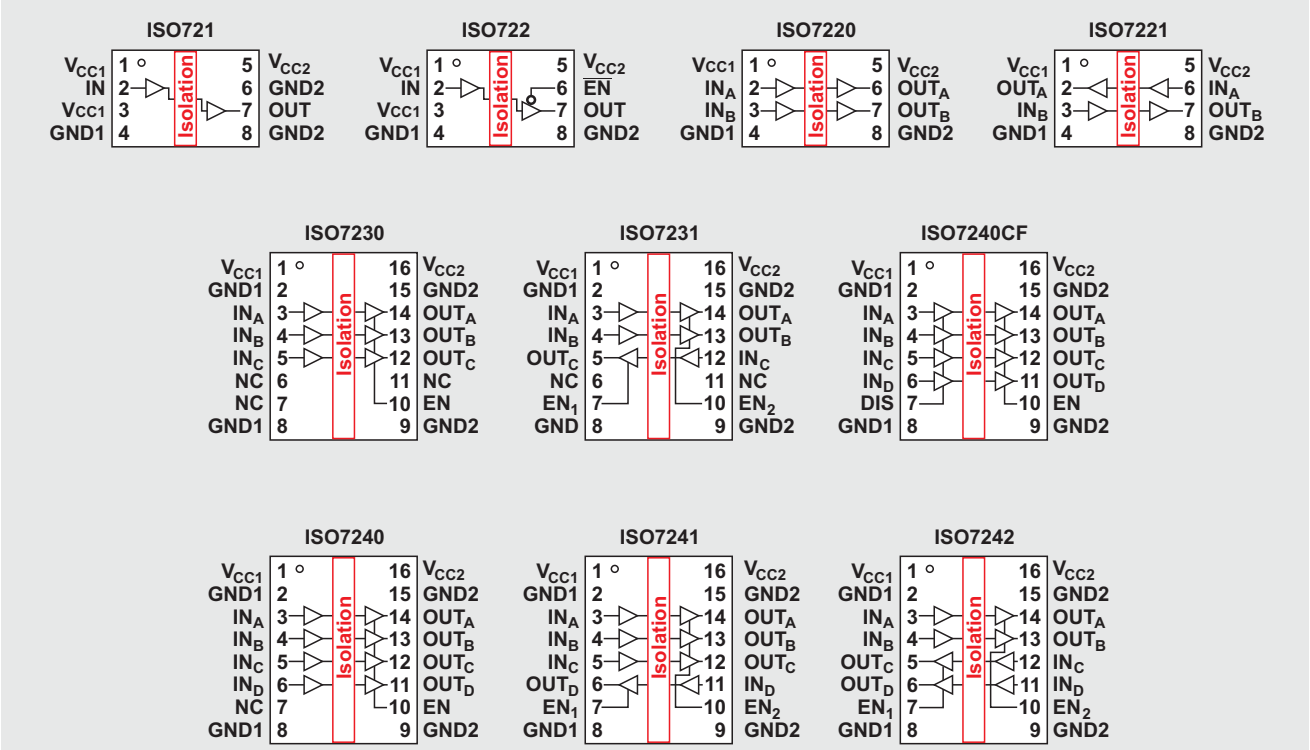


Figure 4. TI family of stand-alone digital isolators



from 3.3 V to 5 V for both supplies, V_{CC1} and V_{CC2}, and allows any combination of these values.

It is important for the designer to keep in mind that digital isolators, due to their single-ended design structure, do not conform to any specific interface standard and are intended only for isolating single-ended, 3-V/5-V digital signal lines.

Figures 5 to 7 give examples of isolated interfaces for SPI, RS-232, and RS-485 applications. Note that the isolator is always placed between the data controller (i.e., the microcontroller or UART) and a data converter or line transceiver, regardless of the interface type or standard.

Figure 5 presents the simplest isolator application. Here the entire circuit constitutes a single-ended, low-voltage system in which a digital isolator connects the SPI interface of a controller with the SPI interface of a data converter. The most commonly applied TI isolators in SPI interfaces are ISO7231 and ISO7241, often designated as 3- and 4-channel SPI isolators.

The full-blown, isolated RS-232 interface in Figure 6 requires two quad isolators because six control signals are required in addition to the actual data lines, RX and TX. Although the entire system is single-ended, the high-voltage requirements of the symmetrical, ±13-V bus supply make it necessary to galvanically isolate the data link between the UART and the low-voltage side of the bus transceiver.

Figure 5. Isolated SPI interface

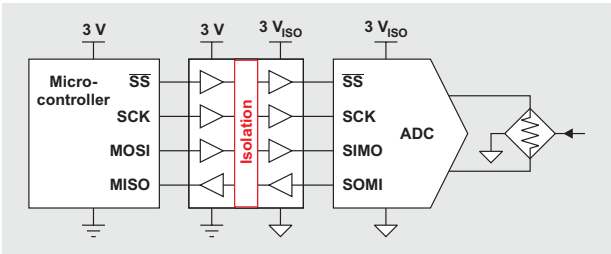
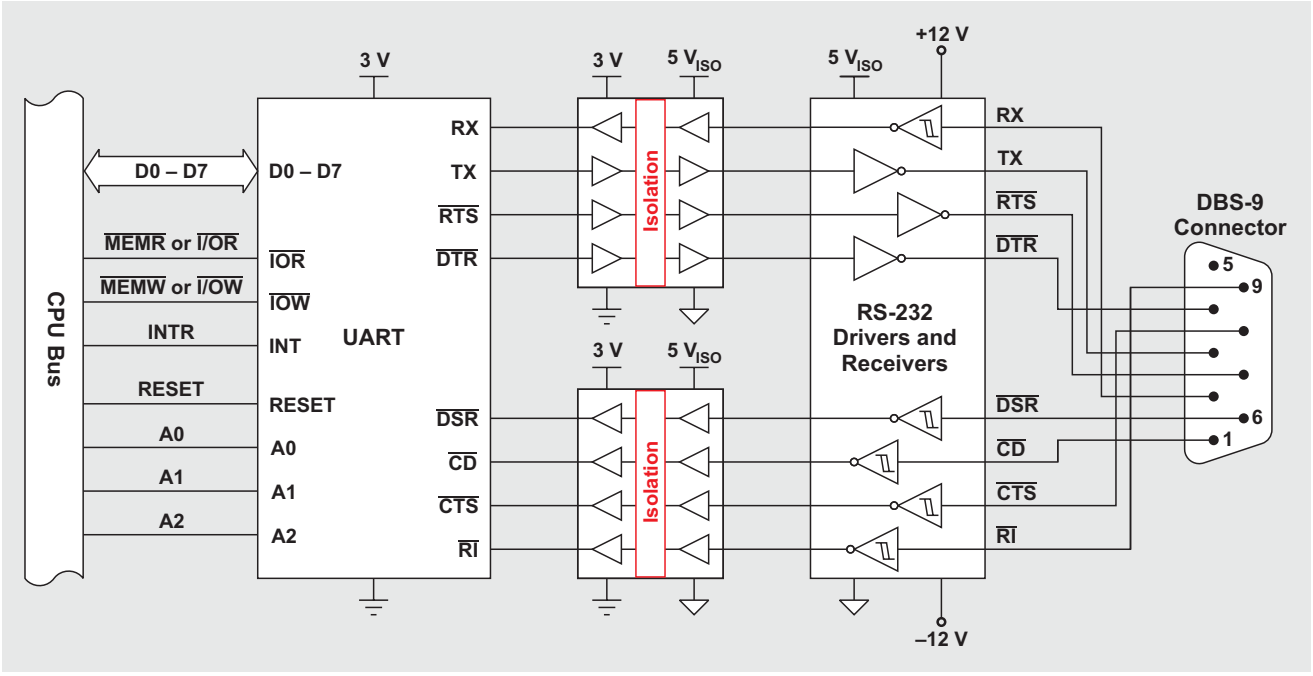


Figure 6. Isolated RS-232 interface



As in the previous example, the isolation of the RS-485 interface in Figure 7a occurs between the controller and the bus transceiver. Despite the entire interface circuit being a low-voltage system, the differential nature of the transmission bus requires prior isolation on the single-ended side. Due to the simplicity of this interface, it was possible to integrate the isolator function into the RS-485 transceiver circuit as shown in Figure 7b, thus providing an application-specific isolator device featuring low cost and a low component count.

To simplify the selection of an appropriate isolator for a specific application, Table 1 provides a comprehensive overview of TI digital isolators. Of the five different speed grades for isolators—A, B, C, CF, and M—all but the M version possess internal low-pass noise filters at the data inputs and are therefore recommended for use in noisy environments. The high-speed version, M, requires external input filtering when used in noisy environments. This is accomplished by connecting a filter capacitor from an

Figure 7. Isolated RS-485 interface

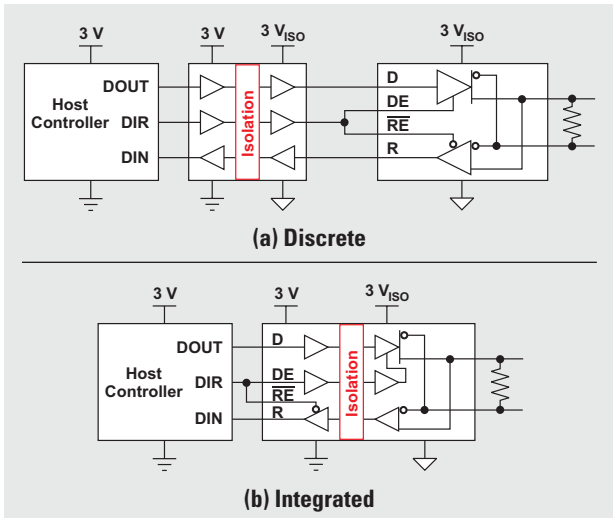


Table 1. Overview of TI stand-alone and application-specific isolators

ISOLATOR TYPE	DEVICE	SPEED GRADE	INPUT THRESHOLD	MAX. DATA RATE* (Mbps)	MAX. PROP. DELAY* (ns)	MAX. CH/CH OUTPUT SKEW* (ns)	TYPICAL OUTPUT RISE TIME* (ns)
Single	ISO721/722		TTL	100	24	—	1
		M	CMOS	150	16	—	1
Dual	ISO7220/7221	A	TTL	1	475	15	1
		B		5	70	3	1
		C		25	42	1	1
		M	CMOS	150	16	1	1
Triple	ISO7230/7231	A	TTL	1	95	2	2
		C		25	42	2	2
		M	CMOS	150	23	1	2
Quad	ISO7240/7241/7242	A	TTL	1	95	2	2
		C		25	42	2	2
		M	CMOS	150	23	1	2
	ISO7240	CF	TTL	25	42	2	2
RS-485 Half-Duplex	ISO3082		TTL	0.2	1.3 (XTR) 125 (RCV)	—	900 (XTR) 1 (RCV)
	ISO15		TTL	1	340 (XTR) 100 (RCV)	—	185 (XTR) 2 (RCV)
	ISO3088		TTL	20	45 (XTR) 125 (RCV)	—	7 (XTR) 1 (RCV)
RS-485 Full-Duplex	ISO3080		TTL	0.2	1.3 (XTR) 125 (RCV)	—	900 (XTR) 1 (RCV)
	ISO35		TTL	1	340 (XTR) 100 (RCV)	—	185 (XTR) 2 (RCV)
	ISO3086		TTL	20	45 (XTR) 125 (RCV)	—	7 (XTR) 1 (RCV)
PROFIBUS Half-Duplex	ISO1176		—	40	40 (XTR) 55 (RCV)	1	3 (XTR) 2 (RCV)

*Switching characteristics with $V_{CC1} = V_{CC2} = 5$ V.

input to the respective device ground. The capacitor value is calculated as

$$C_F = \frac{1}{2\pi \times f_{max} \times R_{SS}},$$

where f_{max} is the maximum signal frequency and R_{SS} is the output impedance of the signal source.

PCB design guidelines

PCB material

Standard Flame Retardant 4 (FR-4) epoxy glass should be used as PCB material for digital circuit boards operating below 150 Mbps (or with rise and fall times longer than 1 ns) and with trace lengths of up to 10 inches. FR-4 meets the requirements of Underwriters Laboratories UL 94 V-0 and is preferred over cheaper alternatives due to its lower dielectric losses at high frequencies; low moisture absorption; greater strength and stiffness; and self-extinguishing burning characteristics.

Layer stack

A minimum of four layers is required to accomplish a PCB design with low electromagnetic interference (EMI) (see Figure 8). Layers should be stacked in the following order, from top to bottom:

- *High-speed traces*—Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator, transmitter, and receiver circuits of the data link.
- *Ground plane*—Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission-line interconnects and provides an excellent low-inductance path for the return current flow.
- *Power plane*—Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in^2.
- *Low-speed traces*—Routing the slower-speed control signals on the bottom layer allows for greater flexibility, as these signal links usually have a margin to tolerate discontinuities such as vias.

If an additional supply-voltage plane or signal layer is needed, a second power/ground-plane system can be added to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also, the power and ground planes of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

Creepage distance

Creepage distance is the shortest path between two conductive parts, measured along the surface of the insulation. An adequate creepage distance protects against tracking, a process that produces a partially conducting path of localized deterioration on the surface of an insulating material as a result of the electric discharges on or close to that surface. Tracking damage to the insulating material normally occurs because of one or more of the following reasons: humidity in the atmosphere, the presence of contamination such as that from corrosive chemicals, and the altitude at which equipment is operated.

The degree of tracking that occurs depends on the comparative tracking index (CTI) of the material and the degree of pollution in the environment. Used for electrical insulating materials, the CTI provides a numerical value of the voltage that will cause failure due to tracking during standard testing. Reference 1 provides a fuller explanation of tracking and CTI.

With higher isolation-voltage levels, it is more important than ever to have a robust PCB design that not only reduces EMI emissions but also reduces creepage problems. In addition to wide isolator packaging, techniques such as cutting grooves can be used to attain a desired creepage distance (see Figure 9).

For a groove wider than 1 mm, the only depth requirement is that the existing creepage distance plus the width of the groove and twice the depth of the groove must equal or exceed the required creepage distance. The groove should not weaken the substrate to a point that it fails to meet mechanical test requirements.

Also, on all layers, the space under the isolator should be kept free of traces, vias, and pads to maintain maximum creepage distance (see Figure 8).

Figure 8. Recommended layer stack

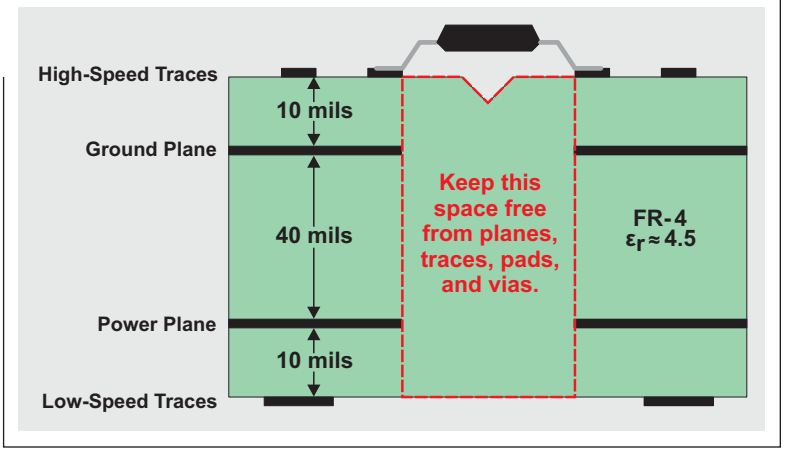
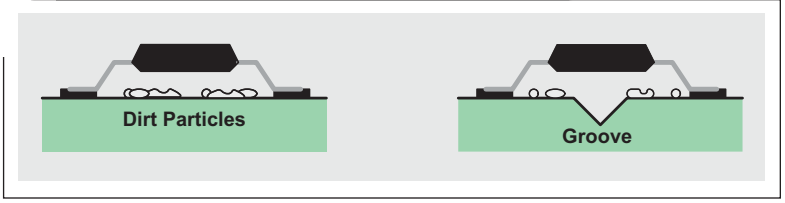


Figure 9. Groove cutting extends effective creepage distance



Controlled-impedance transmission lines

A controlled-impedance transmission line is a trace whose characteristic impedance, Z_0, is tightly controlled by the trace geometries. In general, these traces match the differential impedance of the transmission medium, such as cables and line terminators, to minimize signal reflections. Around digital isolators, controlled-impedance traces must match the isolator's output impedance, $Z_0 \approx r_O$, which is known as source-impedance matching (see Figure 10).

To determine Z_0, the dynamic output impedance of the isolator, $r_O = \Delta V_{OUT}/\Delta I_{OUT}$, needs to be established. For that purpose, the output characteristic in Figure 11 (based on the ISO7240 data sheet) is approximated by two linear segments. One indicates that $r_O \approx 260\ \Omega$ at low voltages; the other indicates that $r_O \approx 70\ \Omega$ for the majority of the curve—and thus for the transition region of the output.

The required trace geometries, such as trace thickness (t) and width (w), the height of the trace (h) above an adjacent ground layer, and the PCB dielectric (ε_r), are partially dictated by the copper-plating capabilities of the board manufacturing process and the dielectric of the chosen board material. Typical values are 1 and 2 oz of copper plating, resulting in trace thicknesses (t) of 1.37 and 2.74 mils, respectively. The dielectric value (ε_r) for FR-4 epoxy glass varies between 2.8 and 4.5 for microstrips and is 4.5 for stripline traces.

With t and ε_r given, the designer has the freedom to define Z_0 through the trace width (w) and height (h). For PCB designs, however, the most critical dimensions are not the absolute values of w and h but their ratio, w/h. Easing the designer's task, Figure 12 plots the characteristic trace impedance as a function of the width-to-height ratio (w/h) for a trace thickness of 2.74 mils (2-oz copper plating), an FR-4 dielectric of 4.5, and a trace height (h) of 10 mils above the ground plane.

From Figure 12 we see that a 70-Ω design requires a w/h ratio of about 0.8. As described later under "Reference planes," designing a low-EMI board requires close electric coupling between the signal trace and ground plane, which is accomplished by ensuring that h = 10 mils. The corresponding trace width would therefore be 8 mils. This width must be maintained across the entire trace length; otherwise, variations in trace width will cause discontinuities in the characteristic impedance, leading to increased reflections and EMI.

Figure 10. Source-impedance matching: $Z_0 \approx r_O$

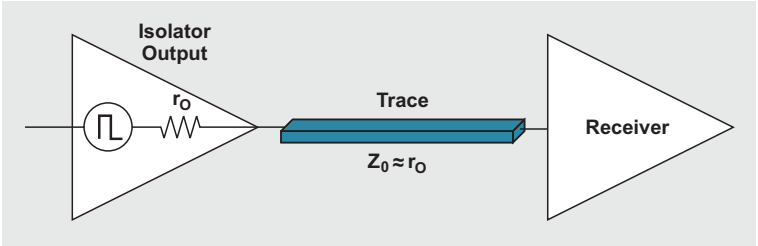


Figure 11. Isolator output characteristic

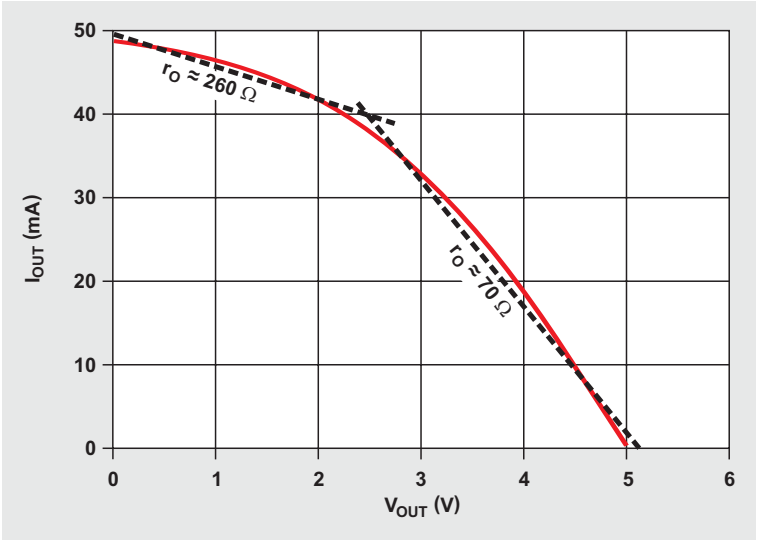


Figure 12. Characteristic impedance as a function of w/h

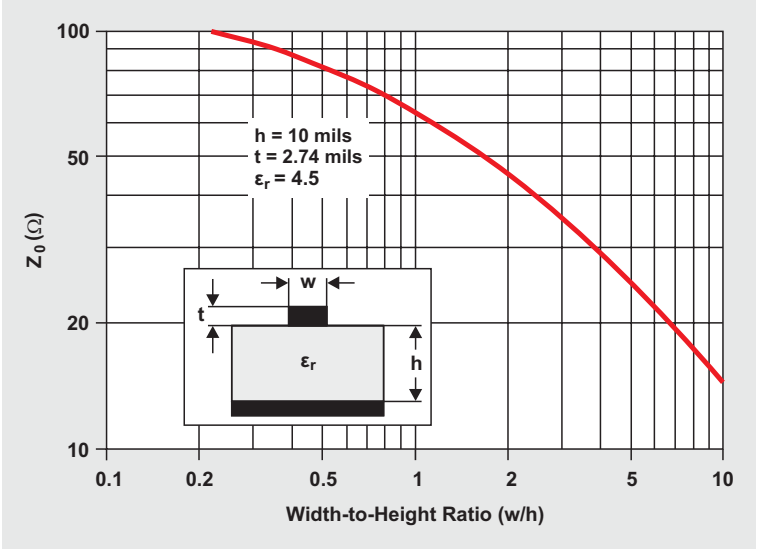
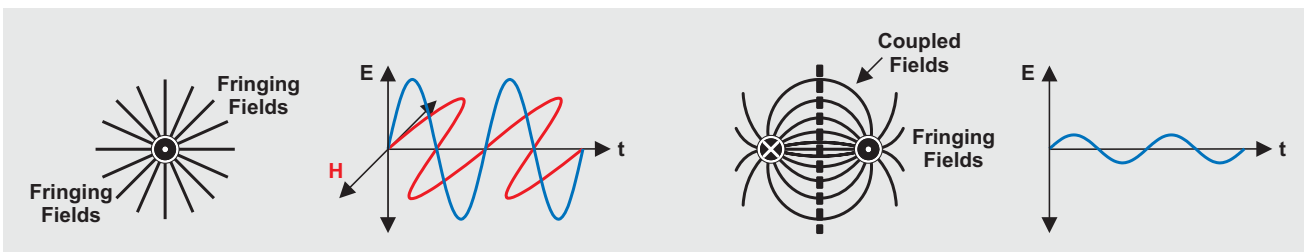


Table 2. Microstrip equations* for when 0.2 < w/h < 1

$\varepsilon_{Eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2} \times \left[\frac{1}{\sqrt{1 + \frac{12h}{w}}} + 0.04 \times \left(1 - \frac{w}{h}\right)^2 - \frac{t}{2.3 \times \sqrt{wh}} \right]$	ε_{Eff} = effective dielectric, taking into account: • dielectric of air • dielectric of PCB material • height above ground • nominal trace width
$w_{Eff} = w + \frac{1.25t}{\pi} \times \left[1 + \ln\left(\frac{2h}{t}\right)\right]$	w_{Eff} = effective trace width, taking into account: • nominal trace width • trace thickness • height above ground
$Z_0 = \frac{60 \times \ln\left(\frac{8h}{w_{Eff}} + \frac{w_{Eff}}{4h}\right)}{\sqrt{\varepsilon_{Eff}}}$	Z_0 = characteristic impedance, taking into account: • effective trace width • height above ground • effective dielectric

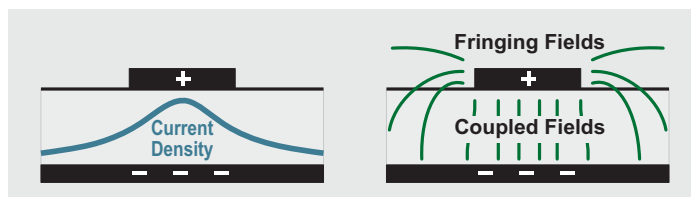
*Keep all dimensions in inches, mils (1 inch = 1000 mils), or millimeters (1 inch = 25.4 mm).

Figure 13. Reducing field fringing through close electric coupling between conductors



Note that this design example is only one of many possible ways to achieve the desired Z_0. Different trace thicknesses due to higher or lower copper plating can be used, as can a different PCB material, but these will require the w/h ratio to change. The rather complex mathematical equations for calculating the characteristic impedance, Z_0, while taking into account the trace thickness, width, and dielectric, are presented in Table 2.

Figure 14. Ground plane acting as a single return trace



Reference planes

The power and ground planes of a high-speed PCB design usually must satisfy a variety of requirements. At DC and low frequencies, they must deliver stable reference voltages, such as V_{CC} and ground, to the supply terminals of integrated circuits. At high frequencies, reference planes, and ground planes in particular, serve numerous purposes. For the design of controlled-impedance transmission systems, the ground plane must provide strong electric coupling with the signal traces of an adjacent signal layer.

Consider a single, AC-carrying conductor with its associated electric and magnetic fields, shown in Figure 13. Loose or no electric coupling allows the transversal electromagnetic (TEM) wave, created by the current flow, to freely radiate into the outside environment, causing severe EMI. Now imagine a second conductor in close proximity, carrying a current of equal amplitude but opposite polarity. In this case the conductors' opposing magnetic fields cancel, while their electric fields tightly couple. The TEM waves of the two conductors, now being robbed of their magnetic fields, cannot radiate into the environment. Only the far smaller fringing fields might be able to couple outside, thus yielding significantly lower EMI.

Figure 14 shows the same effect occurring between a ground plane and a closely coupled signal trace. High-frequency currents follow the path of least inductance, not the path of least impedance. Because the return path of least inductance lies directly under a signal trace, returning signal currents tend to follow this path. The confined flow of return current creates a region of high current density in the ground plane, right below the signal trace. This ground-plane region then acts as a single return trace, allowing the magnetic fields to cancel while providing tight electric coupling to the signal trace above.

To provide a continuous, low-impedance path for return currents, reference planes (power and ground planes) must be solid copper sheets and free of voids and crevices (see Figure 15). For reference planes, it is important that the clearance sections of vias do not interfere with the path of the return current. In the case of an obstacle, the return current will find its way around it. However, when this happens, the current's electromagnetic fields will most likely interfere with the fields of other signal traces, introducing crosstalk. Moreover, this obstacle will adversely affect the impedance of the traces passing over it, leading to discontinuities and increased EMI.

Figure 15. Return-current paths in solid versus slotted ground planes

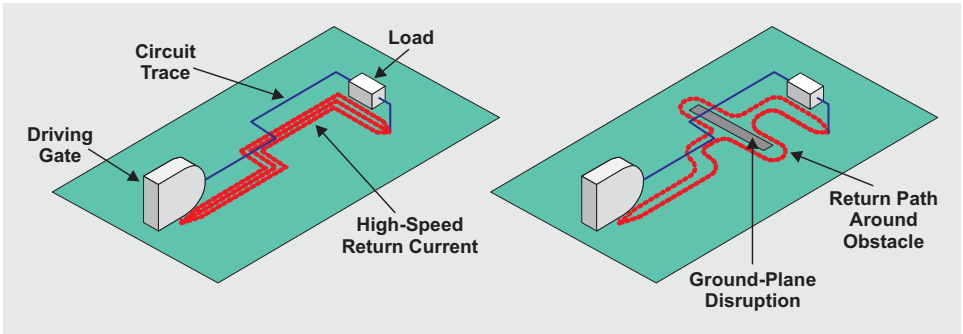


Figure 16. Separate traces to minimize crosstalk

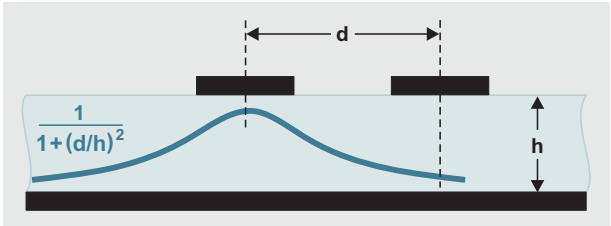
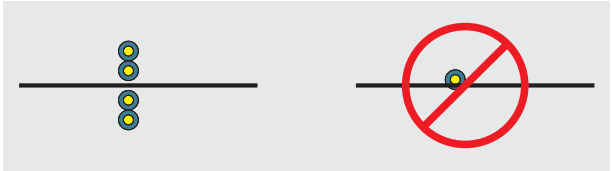


Figure 17. Use 45° bends instead of 90° bends

Figure 18. Avoiding via clearance sections



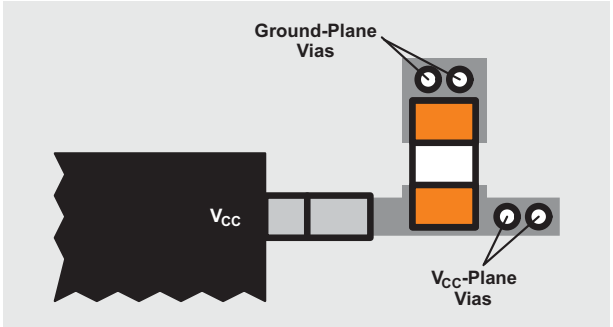
Routing

Guidelines for routing PCB traces and placing components are necessary to maintain signal integrity, avoid noise pickup, and lower EMI. Although there seem to be an endless number of precautions to be taken, only a few main layout recommendations are provided here:

1. Separate signal traces by three times the trace-to-ground height (d = 3h) to reduce crosstalk to 10% (see Figure 16). Because the return-current density under a signal trace diminishes via the function $1/[1 + (d/h)^2]$, it will be sufficiently small at a point where d > 3h to avoid causing significant crosstalk in an adjacent trace.
2. Use 45° bends (chamfered corners) instead of right-angle (90°) bends (see Figure 17). Right-angle bends increase the effective trace width and thus the trace impedance. This creates additional impedance mismatch, which might lead to higher reflections.
3. For permanent operation in a noisy environment, connect the Enable inputs of an isolator through a via to the appropriate reference plane; that is, connect high-Enable inputs to the V_{CC} plane and low-Enable inputs to the ground plane.
4. When routing traces next to a via or between an array of vias, make sure that the via clearance section does not interrupt the path of the return current on the ground plane below (see Figure 18). If a via clearance section lies in the return path, the return current will find a path of least inductance around it. By doing so, it might cross below other signal traces, thus generating crosstalk and increasing EMI.
5. Avoid routing signal traces over different layers, as this causes the inductance of the signal path to increase.
6. If, however, such routing is unavoidable, accompany each signal-trace via with a return-trace via. In this case, use the smallest via size possible to minimize the increase in inductance.
7. Use solid power and ground planes for impedance control and minimum power noise.
8. Use short trace lengths between the isolator and surrounding circuits to avoid noise pickup. Digital isolators are usually accompanied by isolated DC-to-DC converters that supply power across the isolation barrier. Because single-ended transmission signaling is sensitive to noise pickup, the switching frequencies of nearby DC-to-DC converters can easily be picked up by long signal traces.

9. Place bulk (i.e., 10-µF) capacitors close to power sources such as voltage regulators or where the power is supplied to the PCB.
10. Place smaller (0.1-µF or 0.01-µF) bypass capacitors close to the device to be bypassed. This can be accomplished by connecting the power side of the capacitor directly to the device's supply terminal and through two vias to the V_{CC} plane (see Figure 19). Connect the ground side of the capacitor through two vias to the ground plane.

Figure 19. Connect bypass capacitor directly to V_{CC} terminal



Vias

The term "via" commonly refers to a plated hole in a PCB. While some applications require through-hole vias to be wide enough to accommodate the leads of through-hole components, designs for high-speed boards mainly use vias to route signal traces to different layers, connect SMT components to the required reference plane, and connect reference planes of the same potential to each other.

Layers connecting to a via do so by making direct contact with a pad surrounding the via (the "via pad"). Layers that must not connect are separated by a clearance ring. Every via has a capacitance to ground that can be approximated with the following equation:

$$C = \frac{1.41 \times \varepsilon_r \times T \times D_1}{D_2 - D_1},$$

where D_2 is the diameter of a clearance hole in a ground plane (in inches), D_1 is the diameter of a pad-surround via (in inches), T is the thickness of the PCB (in inches), ε_r is the dielectric constant of the PCB, and C is the parasitic via capacitance (in picofarads). Because the capacitance increases proportionally with size, trace vias in high-speed boards should be as small as possible to avoid signal degradation caused by heavy capacitive loading.

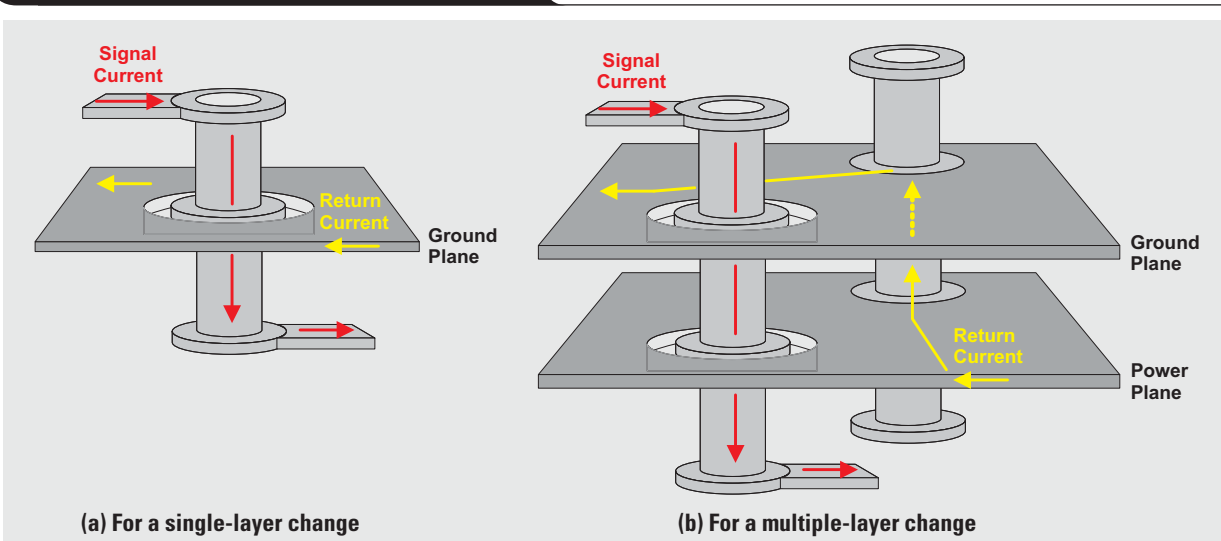
When decoupling capacitors are connected to a ground plane, or when ground planes are connected to each other, the via's inductance becomes more important than its capacitance. The magnitude of this inductance is approximated by

$$L = 5.08h \times \left[\ln\left(\frac{4h}{d}\right) + 1 \right],$$

where L is the via inductance (in nanohenries), h is the via length (in inches), and d is the via diameter (in inches). Because this equation involves a logarithm, changing the via diameter does little to influence the inductance. A big change may be effected by changing the via length or by using multiple vias in parallel. Therefore, the designer should connect decoupling capacitors to ground by using two paralleled vias per device terminal. For low-inductance connections between ground planes, multiple vias should be used in regular intervals across the board.

It is highly recommended that high-speed traces not change layers; but, if they must, the designer should ensure a continuous return-current path. Figure 20 shows the flow of the return current for a single-layer change and a multiple-layer change.

Figure 20. Continuous return-current paths

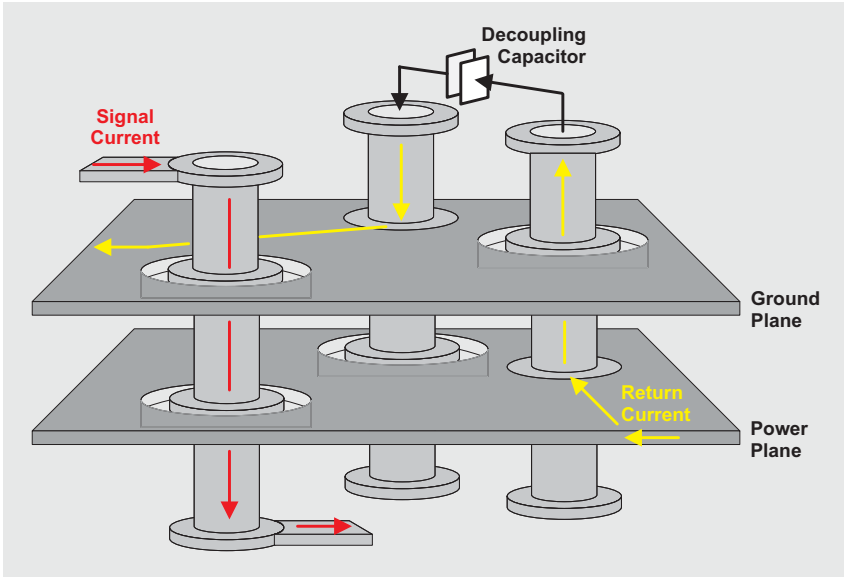


The ability for the current flow to change from the bottom to the top of the ground plane is provided by a metallic laminate of the inner clearance ring. Thus, when a signal passes through a via and continues on the opposite side of the same plane, a return-current discontinuity does not exist.

A signal trace that changes from one layer to another by crossing multiple reference planes complicates the design of the return-current path. In the case of two ground planes, a ground-to-ground via must be placed near the signal via to ensure a continuous return-current path (see Figure 20b).

If the reference planes are of different voltage potentials, such as the power and ground planes in Figure 21, the design of the return path becomes messy, requiring a third via and a decoupling capacitor. The return-current flow begins at the bottom of the power plane, where it is closest to the signal current. It then flows through the power via, across the decoupling capacitor into the ground via, and returns on top of the ground plane.

Figure 21. Return-current path for reference planes with different voltage potentials



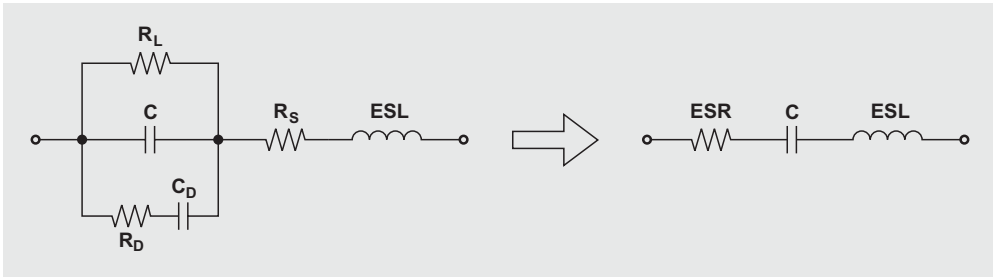
Return-current paths comprising multiple vias and decoupling capacitors possess high inductance, thus compromising signal integrity and increasing EMI. If possible, the designer should avoid changing layers during high-speed trace routing, as it usually worsens board performance, complicates design, and increases manufacturing cost.

Decoupling capacitors

Decoupling capacitors provide a local source of charge for ICs requiring a significant amount of supply current in response to internal switching. Insufficient decoupling causes a lack of supply current, resulting in signal-integrity problems and data errors. The capacitors must provide low impedance for a specific frequency range. To accomplish that, a common approach is to distribute an array of decoupling capacitors evenly across the board. In addition to maintaining signal integrity, decoupling capacitors serve as EMI filters, preventing high-frequency RF signals from propagating throughout the PCB.

Connecting a capacitor between the power and ground planes actually loads the power supply with a series resonant circuit whose frequency-dependent R-L-C components represent the equivalent circuit of a real capacitor. Figure 22 shows the parasitic components of an initial equivalent circuit and their conversion into a series resonant circuit. The leakage resistance, R_L, represents the loss through leakage current at low frequencies. R_D and C_D respectively indicate the losses due to molecular polarization and dielectric absorption. R_S depicts the resistance in the leads and plates of the capacitor. The three resistive losses are combined into one equivalent series resistance (ESR). The equivalent series inductance (ESL) combines the inductance of the capacitor plates and internal leads.

Figure 22. Capacitor losses modeled by a series resonant circuit



Note that the capacitor-connecting vias, although low in impedance, contribute a significant amount to the series inductance. Therefore, via inductance should be reduced by using two vias per capacitor terminal.

Figure 23 shows the progression of capacitor impedance, Z, versus frequency for a 10-nF capacitor. At frequencies far below the self-resonant frequency (SRF), the capacitive reactance is dominant. Closer to the SRF, the inductive reactance gains influence, trying to neutralize the capacitive component. At the SRF the capacitive and inductive reactance cancel each other, and only the ESR is effective. Note that the ESR is frequency-dependent and, in contrast to popular belief, does not reach its minimum at the SRF. However, the impedance, Z, does.

Paralleling capacitors in a distributed decoupling network works because the total capacitance increases to $C_{TOT} = C \times n$, where n is the number of decoupling capacitors used. With $X_C = 1/\omega C$, the capacitor impedance is reduced to $X_{C_{TOT}} = 1/n\omega C$ for frequencies below SRF. The same holds true for the inductance. Here $L_{TOT} = L/n$; and, because $X_L = \omega L$, the impedance decreases to $X_{L_{TOT}} = \omega L/n$ for n capacitors at frequencies above SRF.

Designing a solid decoupling network must include lower frequencies down to DC, which requires the implementation of large bypass capacitors. Therefore, to provide sufficient low impedance at low frequencies, 1-µF to 10-µF tantalums should be placed at the output of voltage regulators and at the point where power is supplied to the PCB. For the higher-frequency range, several 0.1-µF or 0.01-µF ceramics should be placed next to every high-speed switching IC.

Conclusion

Without claiming to be complete, this article covers the main aspects of PCB design with digital isolators. Following the recommendations presented will help designers accomplish an electromagnetic-compatible board design in the shortest time possible. Further information is available in the ISO72xx data sheets and EVM manuals.

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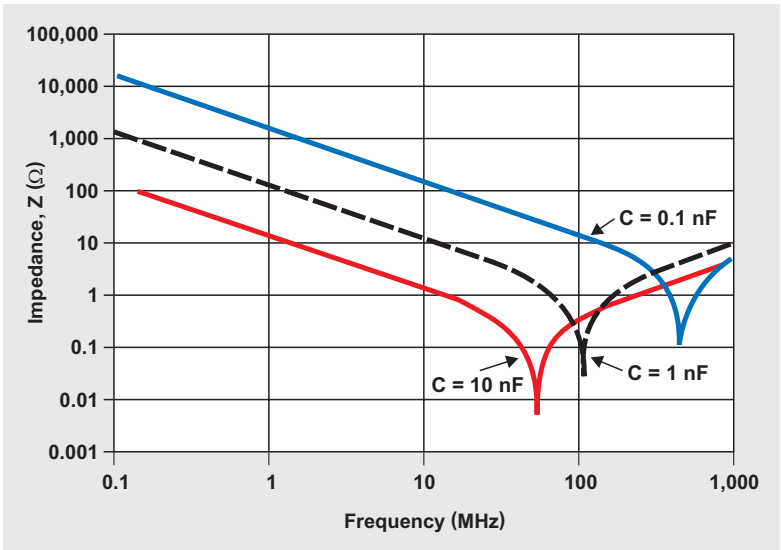
Figure 23. Capacitor impedance versus frequency



Using fully differential op amps as attenuators, Part 1: Differential bipolar input signals

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Introduction

Conditioning high-voltage input signals to drive ADCs from high-voltage sources can be challenging. How can a higher-voltage signal like ±10 V be attenuated and level-shifted to match the significantly lower differential and common-mode-voltage input required by the ADC? In this article, Part 1 of a three-part series, we consider a balanced, differential bipolar input signal and propose an architecture utilizing a fully differential operational amplifier (FDA) to accomplish the task.

We consider this type of circuit first because it most clearly shows how to approach the design, keep a balanced circuit, and not introduce unwanted offsets. Parts 2 and 3 will appear in future issues of the *Analog Applications Journal*. Part 2 will show how to adapt the circuit to a single-ended bipolar input. Part 3 will show the more generic case of a single-ended unipolar input with arbitrary common-mode voltage. The level of complexity will increase with each step, but ordering the presentation in this manner should help the reader better understand why values are chosen for the final circuit the way they are.

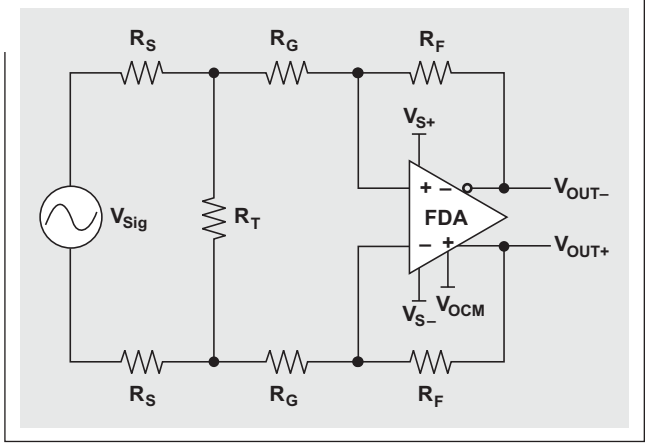
Differential bipolar input

The fundamentals of FDA operation are presented in Reference 1. Since the principles and terminology presented there will be used throughout this article, please see Reference 1 for definitions and derivations.

FDAs can easily be used to attenuate large signals, convert single-ended signals to differential signals, and level-shift voltages to match the input requirements of lower-voltage ADCs. The trick is to implement them in a way that will perform these tasks while keeping the amplifier stable.

FDAs have been compared to two standard, inverting, single-ended output op amps configured in a differential architecture. While this has some validity, one important difference is that a unity-gain, stable op amp is compensated for a noise gain* of 1, while a unity-gain, stable FDA is typically compensated for a noise gain of 2. The implication of this in the context of implementing an attenuator circuit is that the gain resistors can no longer be chosen simply to provide the attenuation. Two approaches are identified in this article; one implements an input attenuator with resistor values chosen to provide a noise gain of 2, and the other implements the attenuator using the gain-setting resistors with added components to get a noise gain of 2.

Figure 1. Attenuator circuit for differential bipolar input



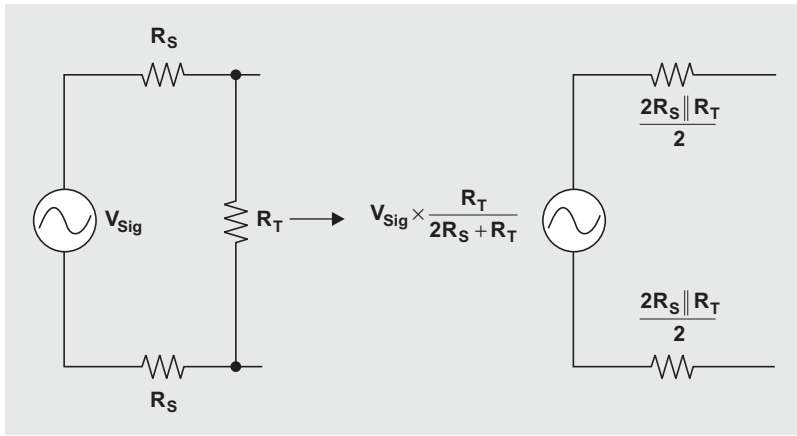
Using an input attenuator

The proposed input-attenuator circuit for a balanced, differential bipolar input signal is shown in Figure 1, whose parameters are defined as follows:

- V_{S+} and V_{S-} are the power supplies to the amplifier.
- V_{Sig} is the input-signal source.
- R_S and R_T are the resistors that provide attenuation of the signal from the source. Their parallel combination also affects the noise gain of the amplifier.
- R_G and R_F are the main gain-setting resistors for the amplifier.

*Noise gain is used to define the stability criteria of an op amp and is calculated as the gain from the input terminal of the op amp to the output. Generally, one speaks of op amp stability in terms of the minimum noise gain required, where larger values are fine, but lower values may lead to instability or oscillation.

Figure 2. Thevenin-equivalent input source and attenuator



For analysis, it is convenient to assume that the FDA is an ideal amplifier with no offset and has infinite gain. The first step in analyzing the circuit in Figure 1 is to simplify it by using only its attenuator portion and the Thevenin equivalent of the input source. This is shown in Figure 2. With the circuit in this form, it is easier to see that its overall gain can be calculated by the formula

$$\frac{V_{OUT\pm}}{V_{Sig}} = \frac{R_T}{2R_S + R_T} \times \frac{R_F}{R_G + \frac{2R_S \| R_T}{2}}. \quad (1)$$

The noise gain of the FDA can be set to 2 by making the second half of Equation 1 equal to 1:

$$R_G + \frac{2R_S \| R_T}{2} = R_F \quad (2)$$

With this constraint, the overall gain equation reduces to

$$\frac{V_{OUT\pm}}{V_{Sig}} = \frac{R_T}{2R_S + R_T}. \quad (3)$$

There are two degrees of freedom for choosing components in the gain equation—an infinite number of combinations of R_S and R_T that will give the desired input attenuation, and an infinite number of R_F and R_G values to set the gain.

The differential input impedance of this amplifier circuit is given by $Z_{IN} = 2R_S + R_T \| 2R_G$. Depending on the attenuation needed, the input impedance is approximately $2R_S$.

It is recommended that R_F be kept to a range of values for the best performance. Too large a resistance will add excessive noise and will possibly interact with parasitic board capacitance to reduce the bandwidth of the amplifier; and too low a resistance will load the output, causing increased distortion. Design is best accomplished by first choosing R_S close to the desired input impedance, then choosing R_F within the recommended range for the device. For example, the THS4521 performs best with R_F at about 1 kΩ. Next, the value of R_T required to give the desired attenuation is calculated. Then R_G is calculated for the desired gain. These equations are easily solved when set up in a spreadsheet. To see an example Excel® worksheet, go to http://www.ti.com/lit/zip/slyt336 and click Open to view the WinZip® directory online (or click Save to download the WinZip file for offline use). Then open the file FDA_Attenuator_Examples_Diff_Bipolar_Input.xls, and select the Diff Bipolar FDA Input Atten worksheet tab.

Design Example 1

As a design example, let's say we have a 20-V_{PP} differential bipolar (±10-V) signal, and we need a 2-kΩ differential input impedance. We want to use the ADS8321 SAR ADC with a 5-V_{PP} differential input and a 2.5-V common-mode voltage. We choose R_S = 1 kΩ and R_F = 1 kΩ. Rearranging Equation 3 and using substitution, we can calculate

$$R_T = \frac{2R_S}{\frac{V_{Sig}}{V_{OUT\pm}} - 1} = \frac{2\ k\Omega}{4-1} = 666.7\ \Omega.$$

The nearest standard 1% value, 665 Ω, should be used. Then, rearranging Equation 2 and using substitution, we can calculate

$$R_G = R_F - \frac{2R_S \| R_T}{2} = 1\ k\Omega - \frac{2\ k\Omega \| 665\ \Omega}{2} = 750\ \Omega,$$

which is a standard 1% value. These values will provide the needed attenuation function and will keep the FDA stable. The V_{OCM} input on the FDA is then used to set the output common-mode voltage to 2.5 V.

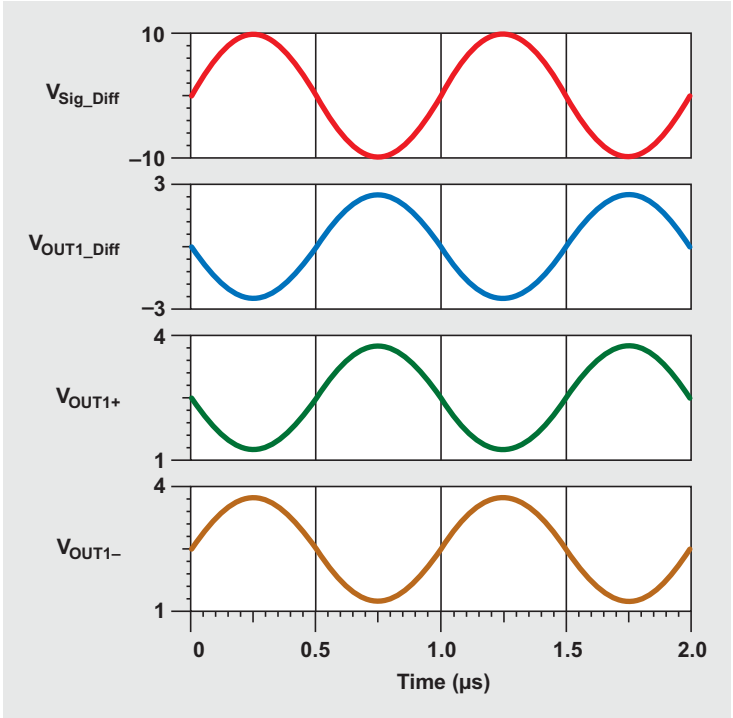
The input impedance is

$$Z_{IN} = 2R_S + R_T \| 2R_G = 2\ k\Omega + 665\ \Omega \| 1.5\ k\Omega = 2461\ \Omega,$$

which is higher than desired. If the input impedance really needs to be closer to 2 kΩ, we can iterate with a lower value. In this case, using R_S = 806 Ω and R_F = 1 kΩ will yield Z_{IN} = 2014 Ω, which comes as close as is possible when standard 1% values are used.

SPICE simulation is a great way to validate the design. To see a TINA-TI™ simulation of the circuit in Example 1,

Figure 3. TINA-TI simulation waveforms of differential bipolar input in Example 1



go to http://www.ti.com/lit/zip/slyt336 and click Open to view the WinZip directory online (or click Save to download the WinZip file for offline use). If you have the TINA-TI software installed, you can open the file FDA_Attenuator_Examples_Diff_Bipolar_Input.TSC to view the example (the top circuit labeled "Example 1"). To download and install the free TINA-TI software, visit www.ti.com/tina-ti and click the Download button.

The simulation waveforms in Figure 3 show that the circuit simulates as expected. V_{Sig1_Diff} is the 20-V_{PP} input; V_{OUT1_Diff} is the differential output of the amplifier circuit; and V_{OUT1+} and V_{OUT1-} are the individual outputs of the amplifier.

Using an FDA's R_F and R_G as an attenuator

The proposed circuit using gain-setting resistors to obtain a balanced, differential bipolar input signal is shown in Figure 4. In this circuit, the FDA is used as an attenuator in a manner similar to using an inverting op amp. The gain (or attenuation) is set by R_F and R_G:

$$\frac{V_{OUT\pm}}{V_{Sig}} = \frac{R_F}{R_G}$$

R_T is used to set the noise gain to 2 for stability:

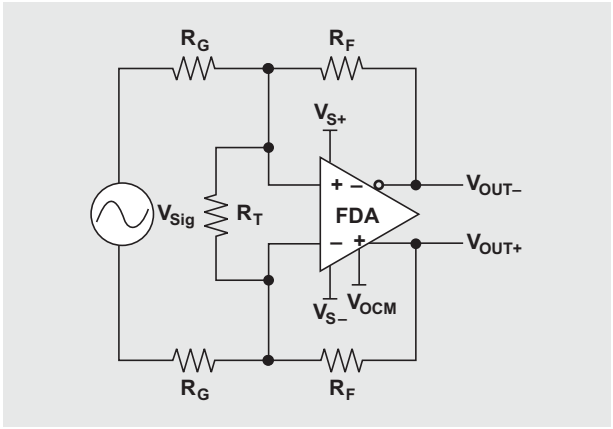
$$R_F = R_G \| \frac{R_T}{2}$$

The equation for input impedance is $Z_{IN} = 2R_G$.

Design Example 2

Using the same approach as for Example 1, with R_F = 1 kΩ, we calculate R_G = 4 kΩ (the nearest standard 1% value is 4.02 kΩ) and R_T = 2.67 kΩ (a standard 1% value). This makes Z_{IN} = 8.04 kΩ. The simulation results are the same as before, but with this approach the only freedom of choice given the design requirements is the value of R_F.

Figure 4. Using FDA's R_F and R_G as attenuator for differential bipolar input



To see an example Excel worksheet, go to http://www.ti.com/lit/zip/slyt336 and click Open to view the WinZip® directory online (or click Save to download the WinZip file for offline use). Then open the file FDA_Attenuator_Examples_Diff_Bipolar_Input.xls, and select the Diff Bipolar FDA Rf_Rg Atten worksheet tab. To see a TINA-TI simulation of the circuit in Example 2, go to http://www.ti.com/lit/zip/slyt336 and click Open to view the WinZip directory online (or click Save to download the WinZip file for offline use). If you have the TINA-TI software installed, you can open the file FDA_Attenuator_Examples_Diff_Bipolar_Input.TSC to view the example (the bottom circuit labeled "Example 2"). Note that this circuit provides the same results as for the circuit in Example 1. To download and install the free TINA-TI software, visit www.ti.com/tina-ti and click the Download button.

Conclusion

We have analyzed two approaches to using an FDA to attenuate and level-shift high-amplitude, differential bipolar signals to the input range of lower-voltage input ADCs. The first approach uses an input attenuator with values chosen to provide the required attenuation and to keep the noise gain of the FDA equal to 2 for stability. The second approach uses the gain-setting resistors of the FDA in much the same way as using an inverting op amp, then a resistor is bootstrapped across the inputs to provide a noise gain of 2. The two approaches yield the same voltage translation that is needed to accomplish the interface task. Other performance metrics were not analyzed here, but the two approaches have substantially the same noise, bandwidth, and other AC and DC performance characteristics as long as the value of R_F is the same.

The input-attenuator approach shown in Example 1 is more complex but allows the input impedance to be adjusted independently of the gain-setting resistors used around the FDA. At least to a certain degree, lower values can easily be achieved if desired, but there is a maximum allowable R_S where larger values require the R_G resistor to be a negative value. For example, setting R_S = 4 kΩ results in R_G = 0 Ω. The spreadsheet tool provided will generate "#NUM!" errors for this input as it tries to calculate the nearest standard value, which then replicates throughout the rest of the cells that require a value for R_G; but this value will work.

It should be noted that a circuit similar to the one in Example 1, with a maximum R_S value and R_G = 0 Ω, results in the same circuit as the one in Example 2 that uses the gain-setting resistors as the attenuator. It should also be noted that the source impedance will affect the input gain or attenuation of either circuit and should be included in the value of R_S, especially if it is significant.

The approach in Example 2 is easier, but the input impedance is set as a multiplication of the feedback resistor and attenuation: $Z_{IN} = 2 \times R_F \times \text{Attenuation}$. This does allow some design flexibility by varying the value of R_F, but the impact on noise, bandwidth, distortion, and other performance characteristics should be considered.

Reference

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1. Jim Karki, "Fully-Differential Amplifiers," Application Report. sloa054

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