

AN-1864 Phase Synchronization with Multiple Devices and Frequencies

ABSTRACT

This application note discusses how phase synchronization can be achieved when multiple chips are involved and also when the frequencies are not the same.

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1 Introduction

In some applications, there is a need to generate multiple signals of different frequencies with a closely controlled phase relationship. One such application is scanners for medical imaging that use many signals of different frequencies. As the signals pass through the body, they are distorted in phase, and these distortions in phase can be used to create an image. If a single chip can generate all the needed frequencies, then it is typically easier to achieve a controlled phase alignment. However, if the application requires more clock outputs than a single chip can generate, then it is necessary to cascade chips in order to get enough outputs.

2 Phase Synchronization

Most devices are clocked on the rising edges of signals and therefore it makes the most sense to focus just on these rising edges. Using this context, two or more signals of the same frequency are considered to be in phase if their rising edges occur at the same time. If these frequencies are multiples of each other, then they are said to be synchronized in phase if they all have a rising edge occurring whenever the lowest frequency signal has a rising edge.

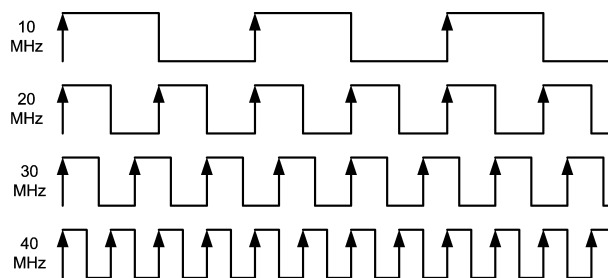


Figure 1. Signals Synchronous in Phase

Figure 1 shows a 10, 20, 30, and 40 MHz signals that are synchronous in phase. Since all of these frequencies are multiples of 10 MHz, they are aligned on the edge of this lowest frequency signal. If the 10 MHz signal was not included, one could see how the 20, 30, and 40 MHz signal could be aligned in phase by imagining a 10 MHz signal being there. Figure 2 illustrates the application of this concept with 12.288 MHz and 30.72 MHz signals that are synchronous in phase. In this example, an imaginary signal of 6.144 MHz has all of the rising edges of the 12.288 and 30.72 MHz signals occurring with its rising edges. 6.144 MHz is the highest frequency that divides both 12.288 and 30.72 MHz and is therefore the greatest common divisor (GCD) of 12.288 and 30.72 MHz. Another frequency that is of interest is the lowest frequency one that has a rising edge corresponding to all of the other signals. In this example, this frequency is 61.44 MHz, which is the lowest frequency that is a multiple of both 12.288 and 30.72 MHz. Mathematically, 61.44 MHz is the least common multiple (LCM) of 12.288 and 30.72 MHz. The concepts of GCD and LCM are discussed in more detail in AN-1865 and allow one to expand this concept to any group of frequencies that are rational ratios of each other.

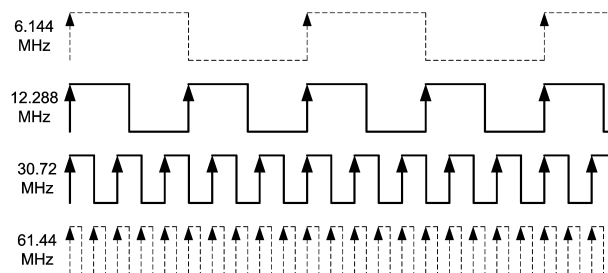


Figure 2. Understanding the LCM and GCD Frequencies

3 Multi-Chip Phase Synchronization

Ambiguous Phase Produced by Division

The delays caused by unequal trace lengths or using chips without division are typically deterministic. However, if division is involved, then random phase relationships can be introduced. When a frequency is divided by a factor of D , there are D possible phase states. Consider the following example in which a signal is divided down by 4 as shown in Figure 3.

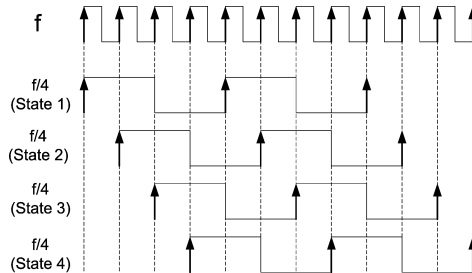


Figure 3. Ambiguous Phase Produced by Division

In this example, there are four possible states which are all phase synchronized to the original signal, but not to each other. It is this ambiguous phase produced by division that can cause synchronization issues when there are multiple copies of a divided frequency generated by different chips if special care is not taken.

LMK01000 and LMK03000 Family of Devices

NOTE: "LMK01000" and "LMK03000" referred to throughout this document, should be reflective of the LMK01000 and LMK03000 family of devices and not limited to the two specific models.

At some point, it becomes necessary to introduce specific families of devices in order to be able to create good examples and get into some of the real details involved. The LMK01000 family of precision devices allows the user to take an input signal and create up to 8 outputs that can be divided and skewed from the original CLKin signal. The delays can be programmed in steps of 150 ps and may also be bypassed.

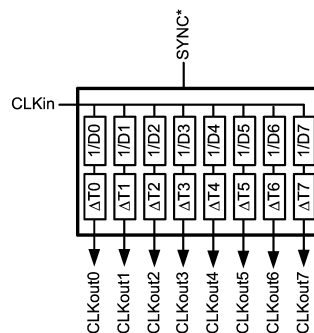


Figure 4. LMK010xx Architecture

The LMK03000 family of timing devices takes the CLKin signal and multiplies it up to a higher frequency using a PLL and VCO. This VCO frequency is divided down by the VCO divider to create the bus frequency. This bus frequency is in to create the clock outputs. Because this VCO divider is in the feedback path of the PLL loop, it has a deterministic phase relationship with the CLKin signal. This bus frequency can be further divided down and skewed if desired as well. The delay from CLKin to CLKout for the LMK03000 is only deterministic if the bus frequency is not divided down. If it is divided down, then there is the random phase error produced by division, that has already been discussed.

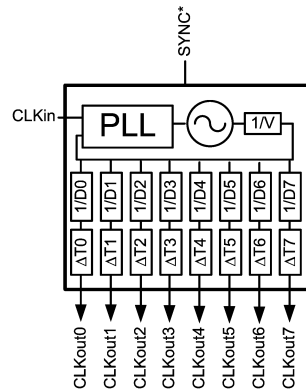


Figure 5. LMK030xx Architecture

The LMK01000 and LMK03000 family of devices have many different options for output types, number of outputs, VCO frequency, and performance grades. For the purposes of simplifying the discussion, these details will not be included unless they are germane to the discussion. One important feature these parts do have is the SYNC* pin, which allows the outputs to be synchronized on a single chip. When this pin is brought from low to high, the outputs will start operating in phase alignment upon the fifth rising edge of the input bus. For the LMK01000, the input bus is simply the CLKin signal. For the LMK03000, this input bus is the VCO frequency after it goes through the VCO divider.

Where only one device chip is used, it is easy to achieve synchronized outputs. However, the challenge comes when more than one device is involved and the timing of the SYNC* pin is unknown. If this pin is pulled from low to high very close to the event of a rising edge of the clock input signal, then there could be two possible phases as shown in Figure 6. Although matching traces will decrease the likelihood of this event occurring, it is impossible to match them exactly accounting for process variations, nonuniform dielectric constants, nonuniform thermal expansion, and various other factors.

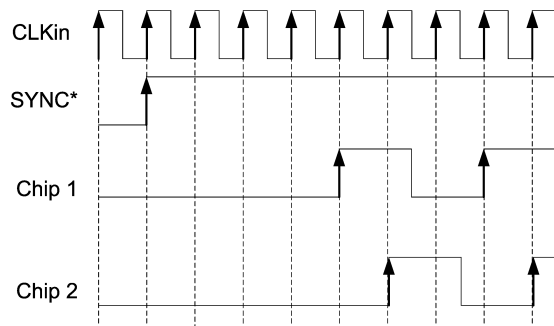


Figure 6. Ambiguous Phase Misalignment

Deterministic Delays

In addition to random phase errors, one also needs to consider the delays through these chips. Using the LMK01000 and LMK03000 as an example, these can be estimated as shown in Table 1. For the LMK03000, the delay from CLKin to CLKout is only deterministic for channel outputs set to bypass mode; otherwise, there will be a random phase error because it is ambiguous what phase state is chosen after the VCO frequency is divided.

Table 1. Typical Delays in ps (does NOT imply any sort of guarantee)

Delay Type	Absolute Number	Variation over Temperature and Voltage	Part to Part Variation	Comments
LMK01000 (Bypass Mode)	600	+/- 40	+/- 40	+/- 150 variation vs. Frequency
LMK03000(Bypass Mode)	1320	+/- 50	+/- 40	+/- 150 variation vs. Frequency
Bypass to Delay	390	+/- 40	+/- 40	This delay varies is less accurate than using the programmed delays
Enabling Divide	100	+/- 10	+/- 5	
Delay Stages	142/Stage	+/- 10	+/- 10	Stages are not all exactly the same delay, but these differences from stage to stage do not change over part, temperature, and voltage

The deterministic delays through chips and due to trace lengths are best illustrated by an example. Consider the case where frequencies of 122.88 MHz, 61.44 MHz, and 8 copies of a 30.72 MHz signal are required. This can be achieved with the LMK03000 family chip driving the LMK01000 family chip with a 30.72 MHz signal as shown in Figure 7. In this case, the delays and divides are not used on the LMK01000 device, but it this chip still provides value by buffering and converting the output to the correct type. For the LMK03000 chip, the analog delays can be used to adjust for unequal trace lengths. For the purposes of calculating delays due to trace length, a rough rule of thumb is 135 ps/inch of trace, although it varies with the trace properties. A useful reference for calculating this delay more exactly, may be found at http://www.emclabinfo.com/emc_calc/microstrip.htm.

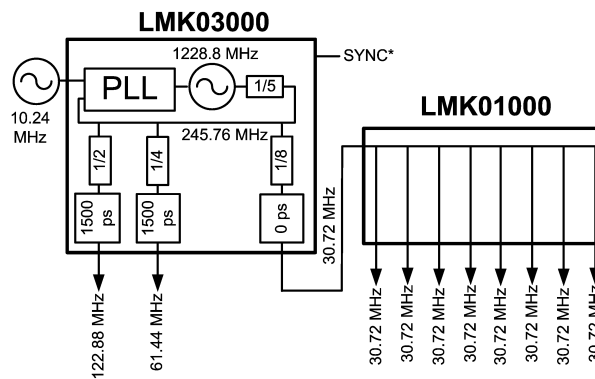


Figure 7. LMK03000 and LMK01000 Cascaded Setup

An experiment was carried out using the configuration in Figure 7. Both boards had the same CLKout trace lengths and they were attached with a 1" barrel connector.

Table 2. Delay Analysis

Source	LMK03000 Delay	LMK01000 Delay
Delay through the LMK01000 Chip		600 ps
1" Barrel Connector		135 ps
2.456" CLKout Trace to LMK01000		332 ps
3.006" CLKin trace to LMK01000		391 ps
Programmed Delay	1500 ps	0 ps
Total Delay (theoretical)	1500 ps (Actual Delay = 1420 ps)	1458 ps
LMK03000 to LMK01000 Skew (theoretical)	38 ps	
Total Delay (measured)		1470 ps
LMK03000 to LMK01000 Skew (measured)	38 ps	

In [Table 2](#) the theoretical calculation is very close, if the true delay stage value of 142 ps/stage is used. Typically, there will be some error due to variations in the LMK01000 delay and errors introduced by SMA connectors and cables. There is also the option of not enabling the LMK03000 delay that drives the LMK01000 to reduce current and noise at the expense of accuracy of the skew. In this case, this would add another 390 ps to the programmed delay.

3.1 LMK03000/LMK01000 Series Combination

In the example in [Figure 7](#), things were simplified because the LMK01000 was simply buffering the signal it was given. If the LMK01000 device also divides the input signal, then there may be potential issues caused the ambiguous phase error produced by division. To overcome this, a general strategy is to plan the frequencies such that all states produced by this ambiguous phase error are valid. To make this possible, the LMK03000 device is used to drive the LMK01000 in such a way that every frequency produced by the LMK01000 device divides evenly into every frequency of LMK03000. In other words, the Least Common Multiple of the LMK01000 frequencies must divide the Greatest Common Divisor of the frequencies from the LMK03000. The order of these chips can not be reversed because when the LMK03000 outputs are divided, the ambiguous phase error will cause the delay through this chip to not be deterministic.

One may be concerned that self-oscillation or noise could cause the second chip to get off a cycle, or that it is necessary to synchronize the first chip and then the second. However, if the frequencies are planned correctly, there is no way the second chip could be off a cycle because all phase relationships will be correct.

Consider the following example where it is desired to produce 122.88 MHz, 61.44 MHz, 30.72 MHz, and 12.288 MHz from two different chips and to have these signals synchronized in phase. This could be accomplished using an LMK03000 family device and an LMK01000 family device as shown in [Figure 8](#). Even though a single chip could be used in this case, it is easy to see if multiple copies of these frequencies were required, utilizing one chip would not be a viable solution.

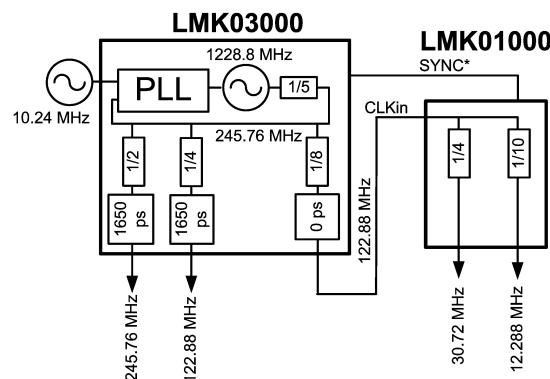


Figure 8. Using the LMK03000 and LMK01000 Together

The delay analysis is shown in [Table 3](#).

Table 3. Using the LMK03000 and LMK01000 Together

Source	LMK03000 Delay	LMK01000 Delay
Delay through the LMK01000 Chip		700 ps
1" Barrel Connector		135 ps
2.456" CLKout Trace to LMK01000		332 ps
3.006" CLKin trace to LMK01000		391 ps
Programmed Delay	1650 ps (Actual Delay = 1562 ps)	0 ps
Total Delay	1562 ps	1558 ps
Theoretical Skew		-4 ps
Actual Measured Skew		52 ps

[Figure 8](#) shows the LMK03000 providing the 122.88 MHz reference for the LMK01000. Although the theoretical frequency to drive the LMK01000 would be $LCM(30.72, 12.288) = 61.44$ MHz, this frequency can not be used because the LMK01000 does not support a divide of 5. It is also important this frequency divides evenly into all frequencies produced by the LMK03000, which is equivalent to saying that it divides GCM $(245.76, 122.88 \text{ MHz}) = 122.88$ MHz. Therefore, 122.88 MHz is the frequency used to drive the LMK01000. [Table 3](#) shows that there is reasonable agreement between the theoretical results and the measured result, although not as close as last time. One possibility is the LMK01000 had divides enabled, which typically adds about 100 ps of delay.

From [Figure 8](#), one may be interested to know how long it takes for all the clock signals to be in phase after the SYNC* pin is asserted. For the LMK03000, this is based on the bus frequency, which is the divided VCO frequency. If we assume the LMK03000 integrated VCO frequency is 1228.8 MHz and this was divided by a VCO divider of 5, then the bus frequency would be 245.76 MHz. It would therefore take 5 cycles of this signal, or 20.3 ns, for the LMK03000 outputs to start working. For the LMK01000, it would take 5 cycles of the 122.88 MHz input frequency, or 40.7 ns, to enable the outputs. The total latency time would be the sum of these two, or 71 ns. Any self-oscillation, or noise at the input of the LMK01000, does not increase this time, but rather improves it. A timing diagram is shown in [Figure 9](#).

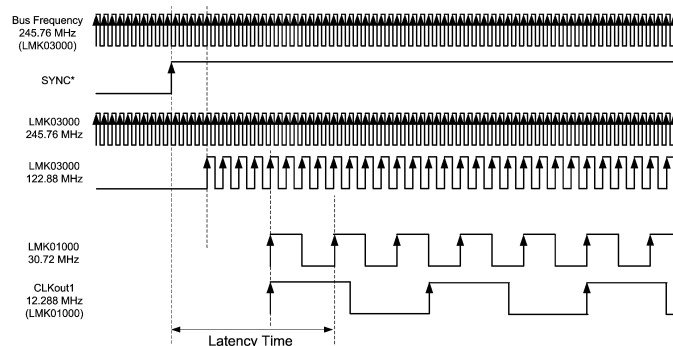


Figure 9. Timing Diagram for Figure 8

The easiest way to synchronize the LMK01000 and LMK03000 combinations is to plan the frequencies strategically. However, there are situations where this may not be sufficient. For instance, given the example shown in [Figure 9](#), consider what would happen if the user also wanted 40.76 MHz, which is $(245.76 \text{ MHz}/6)$. This could be theoretically added to the LMK01000 frequencies, except the LMK01000 does not support a divide of 3. This could be generated by the LMK03000, but then it could not be synchronized using this technique. The 30.72 and 12.288 frequencies have to be generated by the same chip, since they do not divide each other. If one was determined to generate these with both chips, it would be possible, but this would require additional circuitry and gating of the signal.

3.2 LMK03000/LMK01000 Series Combination with More than 2 Devices

It is certainly possible to cascade more than one LMK01000 device, but if there is any ambiguity caused by dividing its input signal, they must be done in a series fashion if the SYNC* signal is to be shared. In Figure 10, the following restrictions are necessary:

$LCM(h_1, h_2, \dots, h_n)$ divides $GCD(g_1, g_2, \dots, g_n)$

$LCM(g_1, g_2, \dots, g_n)$ divides $GCD(f_1, f_2, \dots, f_n)$

Although in this example, all the chips have the same number of signals, this is not a requirement.

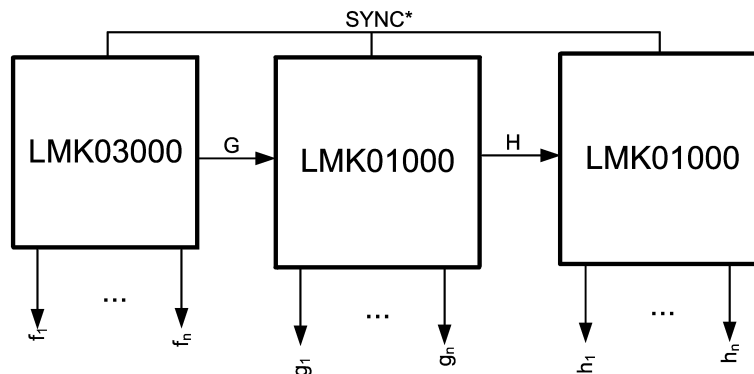


Figure 10. Using the LMK03000 Multiple LMK01000 Devices

3.3 LMK03000/LMK01000 Parallel Combination with Timed SYNC*

Although it is a lot easier to strategically plan the frequencies than add additional circuitry, there will be some instances where it is impossible. In this situation, it might make sense to gate the SYNC* pulse as shown in Figure 11. For the LMK03000, the only phase aligned frequency is the bus frequency, f_{BUS} , which is the frequency after the VCO divider, which is attained by setting the channel dividers in bypass mode. A delayed version of this bus signal is sent through a flip flop to generate a signal for the other LMK01000 family devices. This delay must ensure the SYNC* signal going to the LMK01000 occurs away from a rising edge of the bus signal presented to these chips, accounting for trace delays. The good thing about this method is there are no restrictions on frequencies of the LMK01000, provided they are all derived from the same bus frequency. This method may also be expanded to more than two LMK01000 family devices.

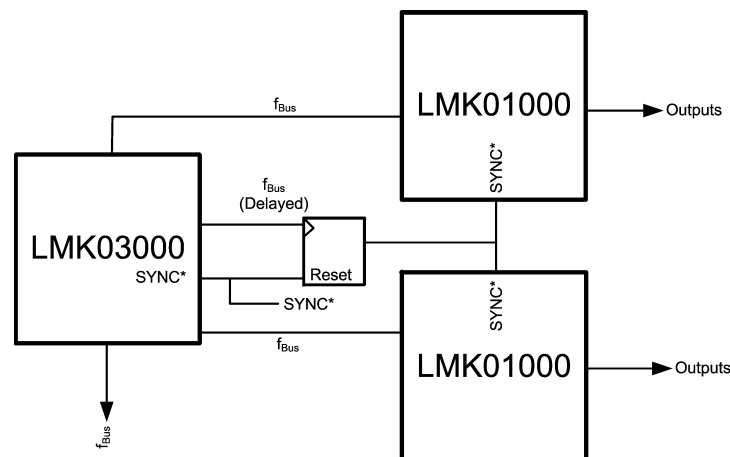


Figure 11. Using the LMK03000 and LMK01000 in a Parallel Configuration

4 Conclusion

The concepts of being synchronized in phase and how the LMK01000 can be added to the LMK03000 in order to achieve more outputs have been discussed. Special care has to be taken when a frequency is divided down because it creates multiple possible phase relationships. Many times, the right frequency plan will prevent a phase alignment issue because all states are correct. The general pattern is to put the highest frequencies on the first chip, and then lower frequencies on subsequent chips. In addition to the benefits of phase alignment, this is also typically optimal for noise performance, because the division is happening farther down the chain. Although strategic frequency planning is the preferred method of synchronization, some situations may arise where divide values or other factors make it necessary to add circuitry to create a specially timed SYNC* signal.

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