ADC081000,ADC08D1000

Interleaving ADCs for Higher Sample Rates

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Technology Edge

Interleaving ADCs for Higher Sample Rates

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Designers have often attempted to combine more than one analog-to-digital converter (ADC) in an effort to increase the effective sample rate. While the flash converter (still the fastest ADC architecture) was available before the advent of high-speed fabrication processes, the process technology limitations restricted those early flash converters to speeds on the order of 10 to 20 Msps (Megasamples per second). Today we have process speeds and architectures that permit sampling at gigahertz rates. (One example of such a product is National's ADC081000, an 8-bit, 1 Gigasample-per-second ADC).

But as process and architecture technologies have given us higher speeds, the fact that designers can have such fast products has produced a desire for even higher sample rates. To get these higher sample rates, designers have sometimes tried to use two to four ADCs and combine their outputs. Let's examine how this can work and what possible problems we might encounter.

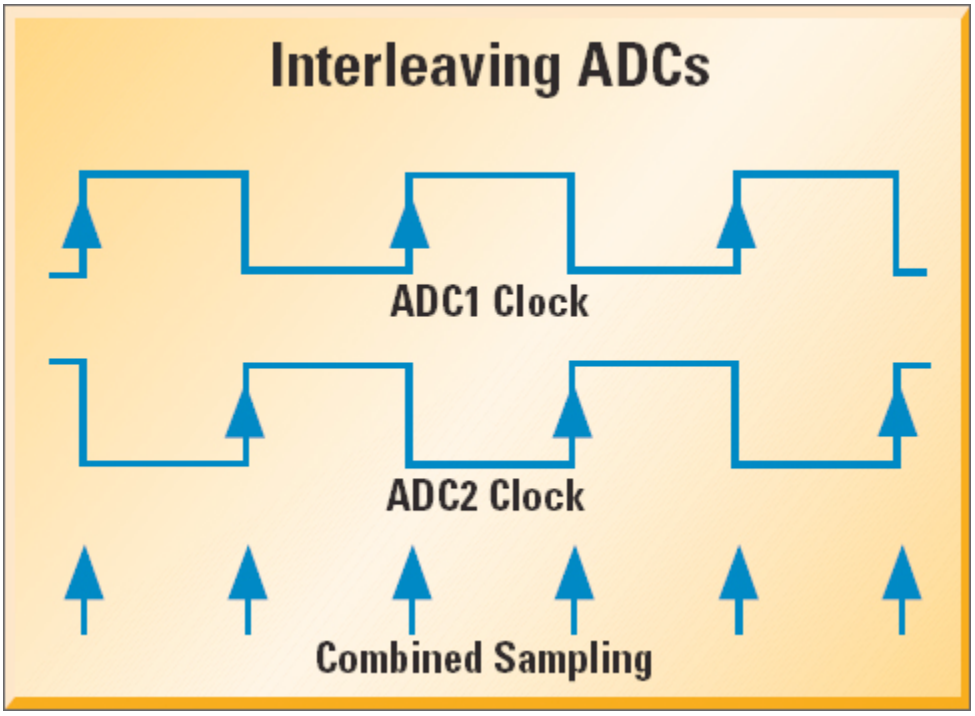
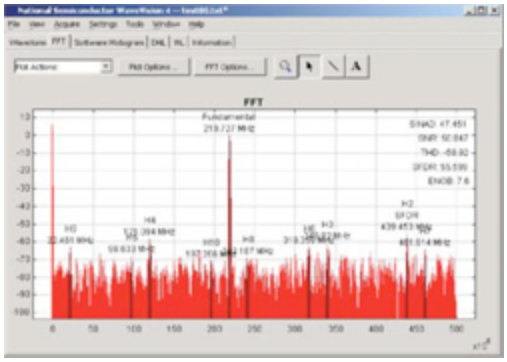


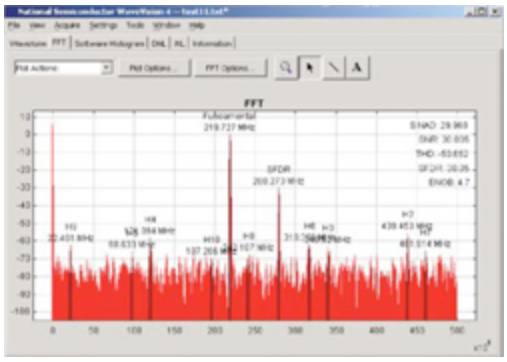
Figure 1. Interleaving two ADCs is the process of using a second ADC to fill data half way between the samples of the first ADC

High-speed ADCs generally sample the input signal on one clock edge: either the rising edge or the falling edge. This means there is one sample per clock cycle and the ADC sample rate is then the same as the ADC clock rate. To combine the output of two ADCs in a process known as interleaving, one needs to sample on both edges of the clock signal, meaning one ADC must be provided with a clock signal that is 180° out of phase with the clock signal to the other ADC. The outputs of the two ADCs are then multiplexed to provide an effective sample rate that is twice that of the sample rate of each ADC (see Figure 1). To minimize the problems of combining two ADC outputs, use two identical devices and two clock signals that are exactly 180° out of phase with each other. Deviation of these clock signals from this phase relationship will cause a spur in the combined ADC output (as seen in Figure 2b compared to Figure 2a). In this example, a spur is noted at about 280 MHz. Note that while THD is not seriously affected, SFDR degrades, which then degrades SNR (Signal to Noise

Ratio), SINAD (Signal to Noise and Distortion) and ENOB (Effective Number of Bits).



A. Interleave sampling with proper phase relationship



B. Interleave sampling with 1% (3.6 degree) phase error

Figure 2. Phase relationship of clock signals is important

This problem is exacerbated when an attempt is made to interleave three or four ADCs (as can be seen in Figure 3), where four ADCs are interleaved. Note that there are three spurs in this example. A spur is a frequency component that does not belong in the output. It may or may not be a harmonic of the input frequency.

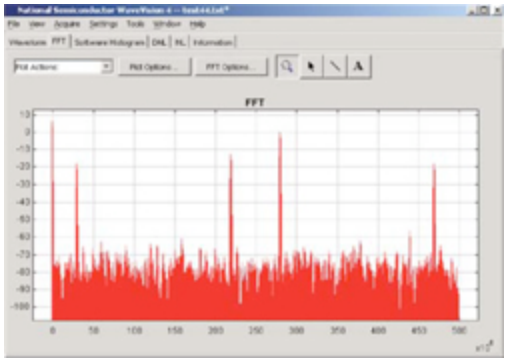


Figure 3. Interleaved sampling of four ADCs, all with different phase errors

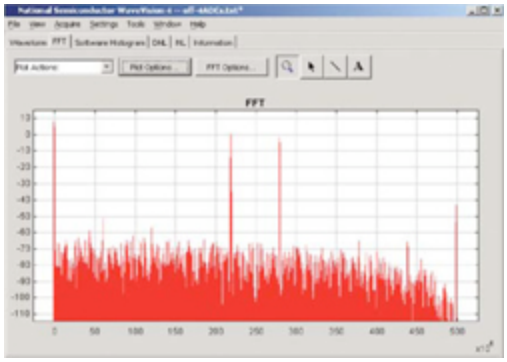


Figure 4. Different offsets of interleaved ADCs will produce a spur at one-half the net sample rate

Even when getting the phasing between the two ADCs correct, there is still the problem of matching offset and gain. Differing offsets between interleaved ADCs will produce a spur at one-half of the net sample rate (see Figure 4). If additional ADCs are interleaved, additional spurs will be produced.

Differing gains among interleaved ADCs will produce spurs at sub-multiples of the clock frequency, shifted by the input frequency (see Figure 3). Having both differing gain and differing offset errors, however, can result in performance so bad that interleaving more than two ADCs can be useless. Indeed, interleaving just two ADCs may produce such poor results that the combination is not at all useful.

Fortunately, many ADCs are available today with sample rates beyond 100 Msps, with much higher sample rates available for lower resolutions. For 8-bit applications, ADCs in the GSPS (Gigasamples per second) range are available. The ADC081000 from National Semiconductor, for example, is specified for a sample rate of 1.0 GSPS and will typically function well at 1.3 GSPS. The dual version of that device, the ADC08D1000, is also specified for 1.0 GSPS and typically performs well at 1.3 GSPS. The benefit with this family of products is its self-calibration feature where offset, gain, and linearity errors are minimized, making it much easier to interleave them without spurs, provided an accurate sampling time relationship exists between them.

The problem remains, then, of developing clock signals that are of the proper phase relationship for two or more converters. That problem, however, has been addressed with the dual ADC08D1000 in that the two converters on the single die can be interleaved to produce an overall sample rate that is twice that of the clock provided to the chip.

This is done by having one of the ADCs on the die sample on the rising edge of the clock and the other ADC on the die sample on the falling edge of the clock, doubling the sample rate to 2.0 GSPS.

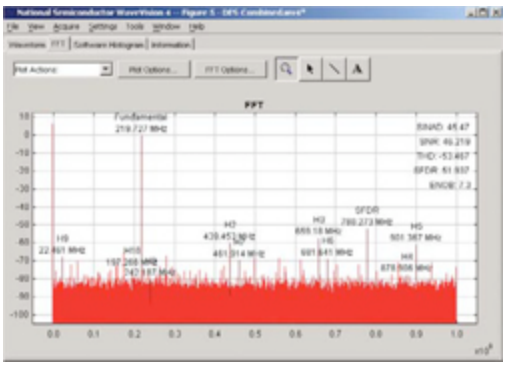


Figure 5. The two ADCs on the ADC08D1000 die can be interleaved without large spurs, doubling its nominal 1.0 GSPS sample rate

This is called Dual Edge Sampling (DES). The excellent results are shown in Figure 5, which is an FFT of ADC08D1000 in the DES mode.

The ADC08D1000 contains a phase adjustment circuit that can automatically adjust the relative phasing of the timing between the two ADCs on the die, minimizing the spurs that might otherwise be produced. With 200 MHz input frequency, the ADC08D1000 produces an ENOB of 7.5 in the normal (non-DES) mode. In the DES mode, the ENOB is 7.3. This is very impressive performance for 2.0 GSPS.

The use of interleaved ADCs presents a rather large challenge to the circuit designer, but the Dual Edge Sampling capability of the ADC08D1000 eliminates the problems associated with interleaving, producing performance that is superior to any other solution in the 2 GSPS arena.

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