Application Note

LMX1204 Multiplier Clock Distribution Drives Large Phased-Array Systems

Russell Hoppenstein *Systems Engineering and Marketing*

ABSTRACT

The LMX1204 is a high-performance clock distribution device. This device is intended to distribute a low phase-noise clock or local oscillator (LO) signal across many channels. The device also employs an integrated multiplier operating between 3.2- and 6.4-GHz output. Designers can use the multiplier feature to create a high-frequency signal from a low-frequency reference source and then distribute as needed. This approach eliminates the need for a separate radio-frequency (RF) synthesizer to generate the signal and the additional power dissipation of such a device. This note presents the phase-noise performance of the multiplier feature in the LMX1204 compared to industry test equipment to gauge the relative performance of the LMX1204. The final test uses the multiplied-up reference from a cascaded LMX1204 design to drive the external clock of the AFE7950 RF sampling transceiver and compare performance of the design to the internal phase-locked loop (PLL) plus voltage-controlled oscillator (VCO) of that device.

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Trademarks

1 Introduction

A large phased-array radar or communication system requires many channels. Components like the AFE7950 (4T6R RF sampling transceiver), the ADC12DJ5200RF (Dual, 5.2 GSPS ADC), or the ADC32RF54 (Quad, 3 GSPS ADC) are examples of data converter devices used in such systems. The devices operate at high sampling rates and integrate multiple channels per device. An entire phased-array system employs many of the devices to satisfy the total number of channels required. Each device requires a high-quality, low phase-noise clock source. Using a low phase-noise RF synthesizer at each device for the clock is possible, but that approach is cumbersome, expensive, and DC power-prohibitive for large systems. An alternative is to use a single low phase-noise source and distribute that source to all of the required devices.

The LMX1204 is a high-frequency clock distribution chip. The device distributes a low phase-noise clock signal to multiple data converters used in large array systems. Each LMX1204 distributes the input clock to four output clocks. Designers can cascade multiple devices to scale the outputs to the required number of channels. The LMX1204 provides a straight buffer option and a divider output option. There is also an integrated multiplier. The multiplier output frequency of operation is limited between 3.2 GHz and 6.4 GHz. Multiply-by-2, 3, and 4 options are available..

As an example, consider the AFE7950 RF sampling integrated transceiver device with an input clock of around 6 GHz. The digital-to-analog converter (DAC) samples at 6 GSPS and the analog-to-digital converter (ADC) divides that clock in half (internally) to sample at around 3 GSPS. The 6-GHz clock must be distributed to each device and the proper phase matching between channels must be verified. One option is to generate the clock with an RF synthesizer like the LMX2820. That clock output is distributed to the required number of elements through the LMX1204 operating in straight buffer mode.

This note investigates an alternative approach to distribute the sample clock by taking advantage of the multiplier option in the LMX1204. The approach uses a very low phase-noise reference source oscillator which is multiplied up to the desired sample clock frequency. The approach eliminates the need for a separate RF synthesizer and takes advantage of an existing high-quality (but low frequency) reference source.

1.1 Basic Clock Distribution System

The LMX1204 includes a 2 ×, 3 ×, or 4 × multiplier option. The caveat is that the output frequency must be within 3.2 GHz to 6.4 GHz. The goal is to generate a 5898.24-MHz clock from a 491.52-MHz reference. Multiplying up from 491.52 MHz directly with the LMX1204 is not possible since the first multiply stage does not satisfy the output frequency requirement. As such, a pre-multiplier stage is needed to get the input frequency within the proper range.

1.2 Pre-multiplier Stage

The pre-multiplier stage multiplies the reference frequency by 3 to get to 1474.56 MHz. This frequency is sufficient to multiply up with the LMX1204 to 5898.24 MHz. The pre-multiplier stage uses a TRF37C75 RF amplifier operating in heavy saturation to generate high harmonic content. The amplifier is followed by a bandpass filter centered on the third harmonic to pass that signal to the LMX1204. The TRF37C75 normally operates at a 5-V supply, but for this approach, the supply is reduced to 3.6 V to reduce power consumption and increase the device saturation. After filtering, this approach yields a signal at 1474.56 MHz at about 0 dBm.

2 Low-Frequency Reference

The multiplier approach assumes that there is a high-quality, low phase-noise reference signal available. This analysis uses a Wenzel oscillator operating at 491.52 MHz as a good quality, but practical reference source. The performance of the Wenzel is compared against the Rohde & Schwarz SMA100B signal generator. This signal generator is the gold standard of signal synthesis and serves as a gauge of the absolute best performance possible, albeit not practical for use in a production system. The Agilent PSG is another high-quality signal generator used as a reference. The PSG phase noise is not as good as the SMA100B, but is still one of the better test equipment generators available.

Figure 2-1 shows the phase-noise comparison of the SMA100B, the Wenzel oscillator, and the Agilent PSG operating at 491.52 MHz. Table 2-1 reports the RMS jitter performance integrated from 1-kHz offset to 40-MHz offset using the Holzworth phase-noise analyzer.

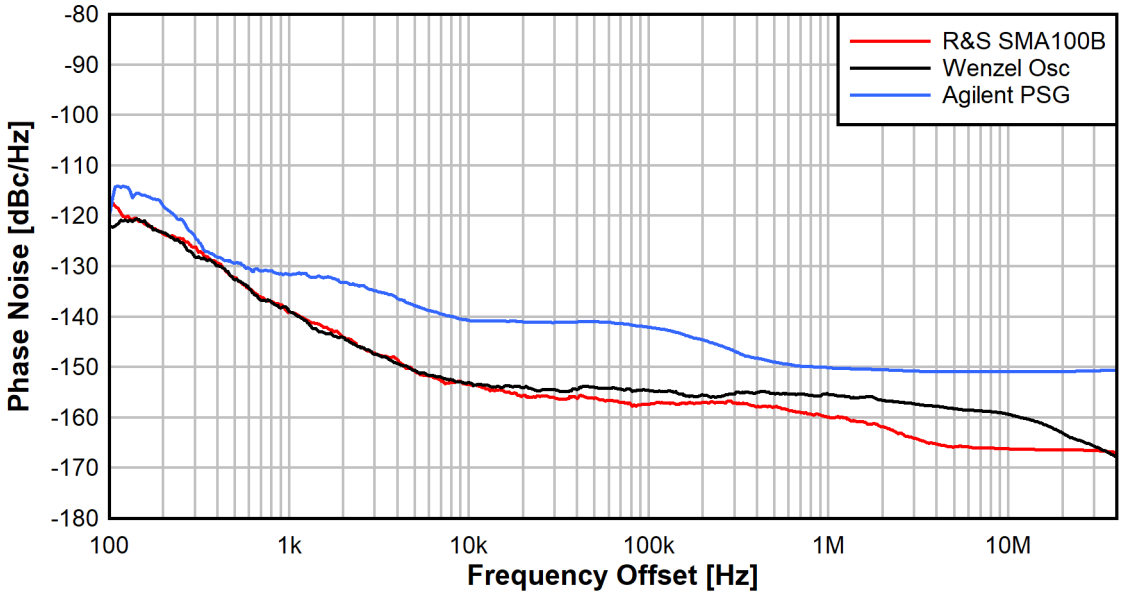

Figure 2-1. Phase-Noise Comparison at 491.52 MHz

Table 2-1. Integrated Jitter Performance at 491.52 MHz

Frequency	Source	RMS Jitter
491.52 MHz	R&S SMA100B	15.6 fs
	Wenzel Oscillator	25.5 fs
	Agilent PSG	85.3 fs

As the results show, the SMA100B performs the best. The Wenzel oscillator keeps pace with the SMA100B out to about 300-kHz offset. The SMA100B definitely out-performs the Agilent PSG.

2.1 Pre-multiplier Stage

Figure 2-2 shows a block diagram of the 3 × pre-multiplier stage using the TRF37C75 amplifier. Figure 2-3 compares the phase-noise performance of the pre-multiplier stage with that of the signal generator. Table 2-2 reports the integrated jitter performance for each configuration.

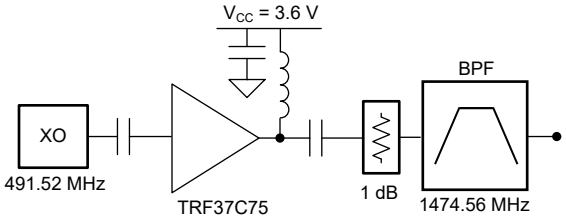

Figure 2-2. 3 × Pre-multiplier Stage

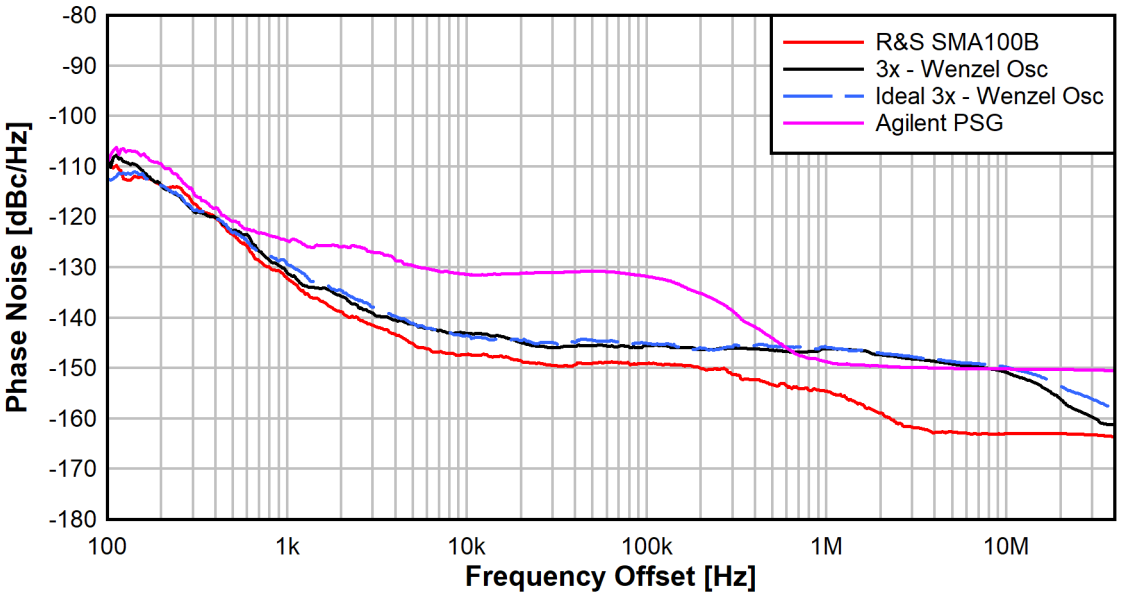

Figure 2-3. Phase-Noise Comparison of 1474.56-MHz Signal

As expected, the SMA100B provides the best output at 1474.56 MHz. The 3 × multiplied Wenzel oscillator performance is also quite good. The sweep of the SMA100B is nearly identical to the ideal response when the input performance is degraded by 20 × log (n), where n = 3 as the multiplication factor. As before, the multiplied-up Wenzel approach is significantly better than the Agilent PSG.

Table 2-2. Integrated RMS Jitter at 1474.56 MHz

Frequency	Source	RMS Jitter
1474.56 MHz	R&S SMA100B	8.1 fs
	Wenzel Oscillator - 3 ×	22.2 fs
	Agilent PSG	35.4 fs

2.2 LMX1204 Multiplier Stage

The LMX1204 device multiplies the 1474.56 MHz by 4 × to achieve the final output sampling frequency of 5898.24 MHz. Figure 2-4 shows the performance of the sample clock phase noise compared to the test equipment sources.

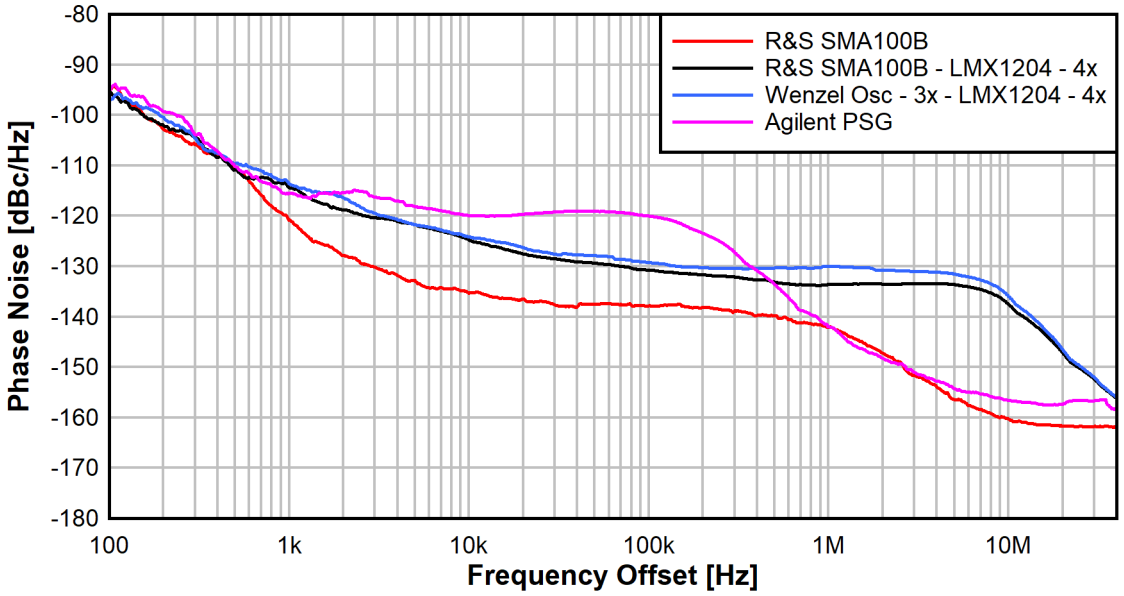

Figure 2-4. Phase-Noise Comparison of 5898.24-MHz Signal

The multiplier circuitry does introduce some phase-noise degradation, particularly evident at the higher frequency offsets beginning at around 1-MHz offset. The performance is still good and still surpasses the Agilent PSG for offsets below the 300-kHz offset. With the multiplier (and the phase-noise contribution of the multiplier) the absolute performance of the source becomes diminished; the performance using the LMX1204 multiplier with the SMA100B as the source versus the pre-multiplier as the source is nearly the same. Table 2-3 reports the integrated jitter performance.

Table 2-3. Integrated Jitter at 5898.24 MHz

Frequency	Source	RMS Jitter
5898.24 MHz	R&S SMA100B	5.4 fs
	R&S SMA100B - LMX1204 - 4x	26.4 fs
	Wenzel Osc - 3x - LMX1204 - 4x	33.6 fs
	Agilent PSG	19.4 fs

2.3 LMX1204 Multiplier vs RF Synthesizer

A natural question is whether using the multiplied-up reference is a better alternative than simply an integrated RF synthesizer like the LMX2820. Figure 2-5 shows the phase-noise comparison between the LMX1204 multiplier and the LMX2820 operating at 5898.24 MHz. The LMX2820 uses the 491.52 MHz Wenzel oscillator as the reference frequency. Table 2-4 reports the integrated jitter performance.

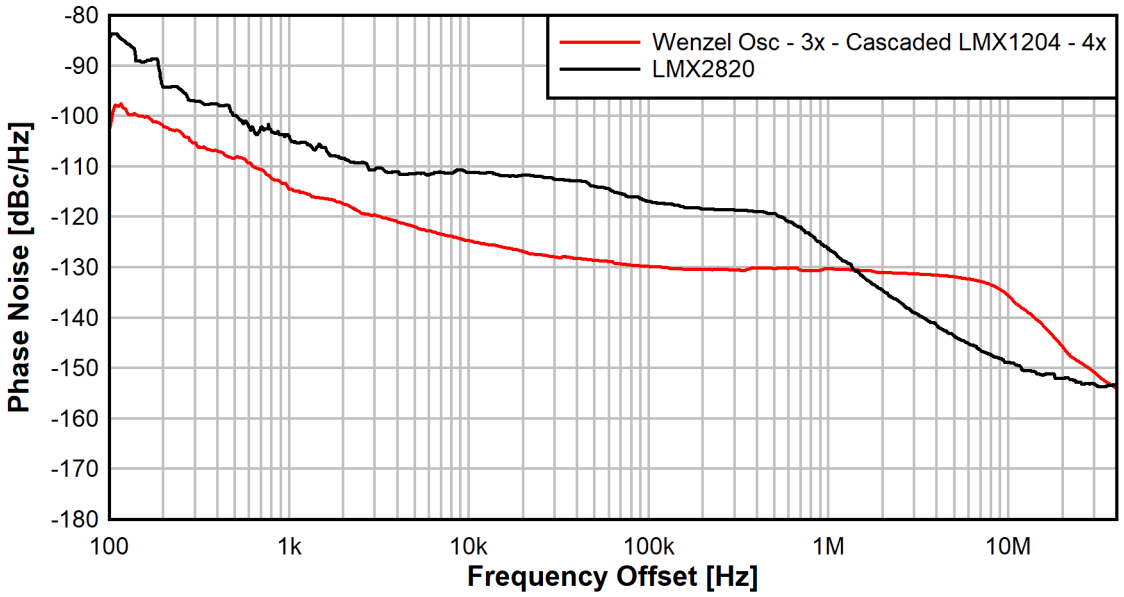

Figure 2-5. Phase-Noise Comparison Between LMX1204 Multiplier and LMX2820

Table 2-4. LMX1204-4x vs LMX2820 Jitter at 5898.24 MHz

Frequency	Source	RMS Jitter
5898.24 MHz	3 × Wenzel Oscillator + 4 × Cascaded LMX1204	33.2 fs
	LMX2820	36.0 fs

THE LMX1204 with multiplier generally performs as good or better than the LMX2820. Low frequency offset phase noise performance is better with the LMX1204 multiplier out to about 1 MHz. After which, the LMX2820 performs better. The integrated RMS jitter is slightly better with the LMX1204 multiplier. The LMX1204 approach provides the additional benefit of eliminating one active device in signal chain, the RF synthesizer, and the associated power consumption of that device. Note, the approach does forego some flexibility as there is no opportunity to adjust the frequency.

3 Real-World Application With AFE7950 RF Sampling Transceiver

The AFE7950 is a 4T6R RF sampling transceiver that is typically used in large phased array systems because of the high frequency of operation and the number of integrated channels available. The AFE7950 clock typically ranges from around 6 GHz up to around 12 GHz. The user determines the clock frequency based on the RF band and power consumption trade-offs. For output bands below 6 GHz, a clock frequency at 6 GHz is likely sufficient and reduces power consumption compared to injecting a higher clock frequency. The DAC clock is taken directly from the sample clock; the ADC clock is divided down from the sample clock and is limited to a max of 3 GHz. The AFE7950 can integrate PLL/VCO to generate the sample clock; however, providing an external clock that has better phase-noise performance is an alternative approach.

Figure 3-1 illustrates a block diagram of a 64T64R phase array system using 16 AFE7950 devices with external clock. Each AFE7950 needs a sample clock. The cascaded LMX1204 topology provides the clock distribution to all of the transceiver devices. The root LMX1204 multiplies the reference signal up to the sample clock frequency. The subsequent LMX1204 stages operate in buffer mode to distribute the signal to each AFE device. Though not depicted in the block diagram, the LMX1204 also provides clocking signals to the FPGA and SYSREF signals to all the devices.

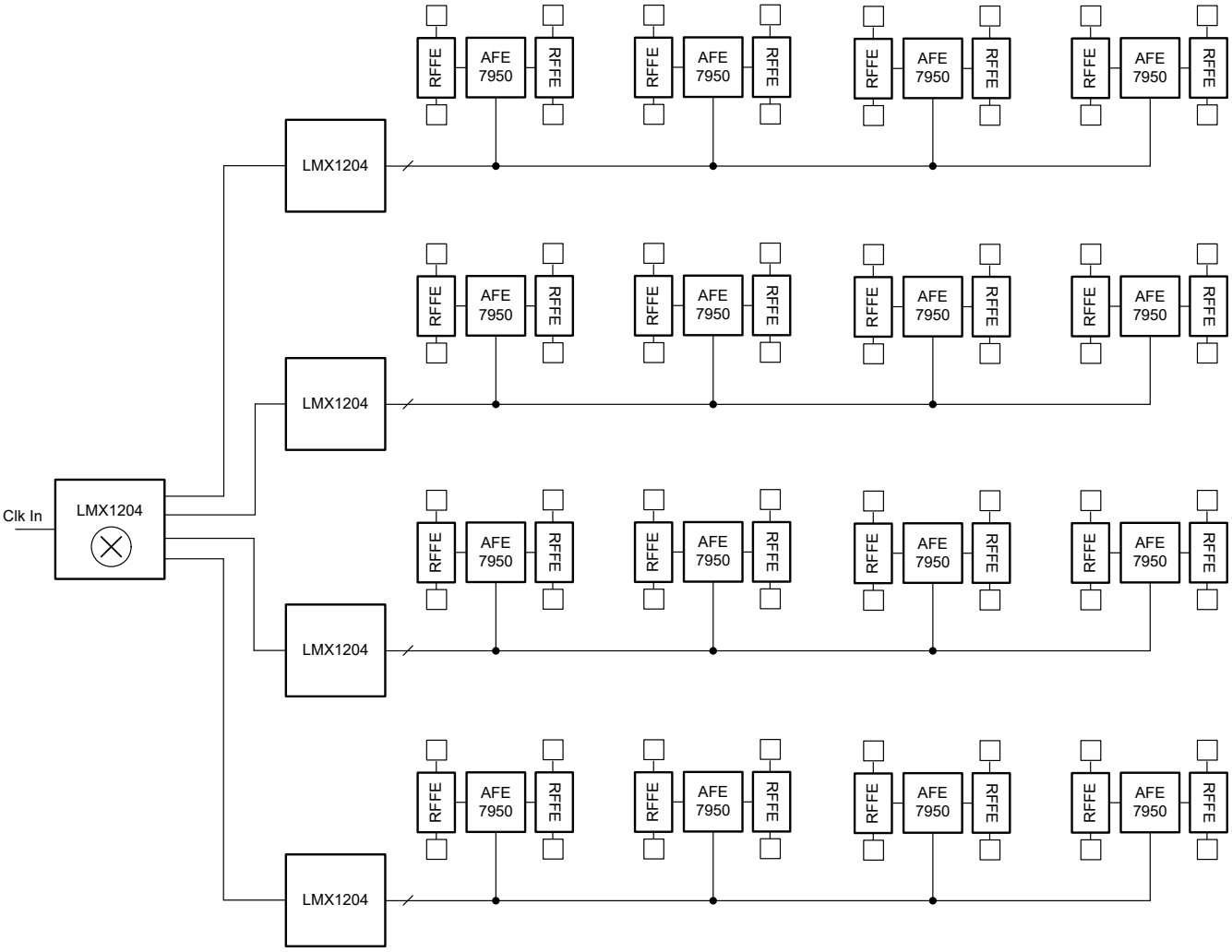

Figure 3-1. AFE7950 64T64R Phased-Array System With Clock Distribution

3.1 AFE7950 Clocking Measurement Setup

Measurement testing uses the cascaded LMX1204 reference design in conjunction with the AFE7950 EVM. The clock source is the Wenzel Oscillator pre-multiplied to 1474.56 MHz. The AFE7950 is programmed to for a 5898.24-MHz sample clock. The numerically controlled oscillator in the AFE7950 is set to 3500 MHz. The digital baseband signal is nearly 10 MHz. The DAC data rate is 491.52 MSPS; the ADC data rate is 245.76 MSPS. Figure 3-2 illustrates the measurement setup.

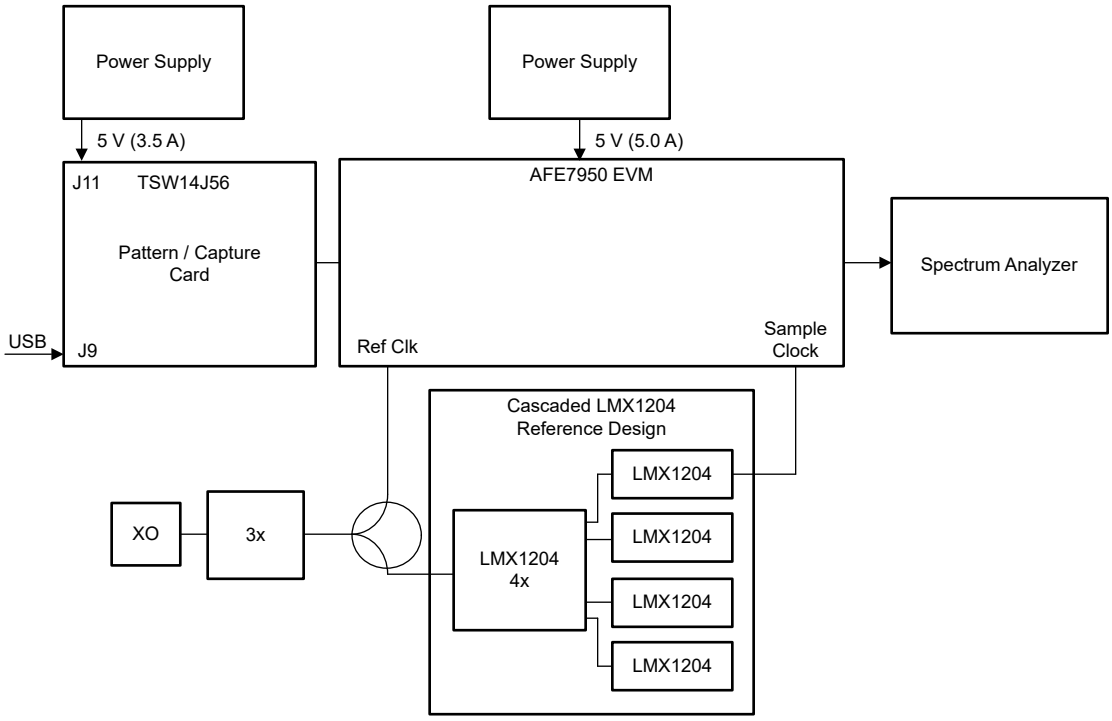

Figure 3-2. AFE7950 Measurement Setup With LMX1204 Clock Distribution

3.2 AFE7950 Clocking Measurement Results

Measurement results compare output phase-noise performance from the transmitter between the cascaded LMX1204 approach (with multiplier) and the internal PLL/VCO. Figure 3-3 shows the spectrum output comparison between the two options. Since the baseband signal is slightly under 10 MHz, the output tone resides just below 3510 MHz. The close-in spectrum performance of the cascaded LMX1204 with multiplier is better than that of the internal PLL/VCO operating at the same clock rate and same output frequency. Figure 3-4 shows the output phase noise plot measured with the Agilent PSA spectrum analyzer with phase-noise option to provide a relative comparison between the close-in phase-noise performance. As evident before, the cascaded LMX1204 approach yields a better close-in performance and equivalent farther out noise=floor performance.

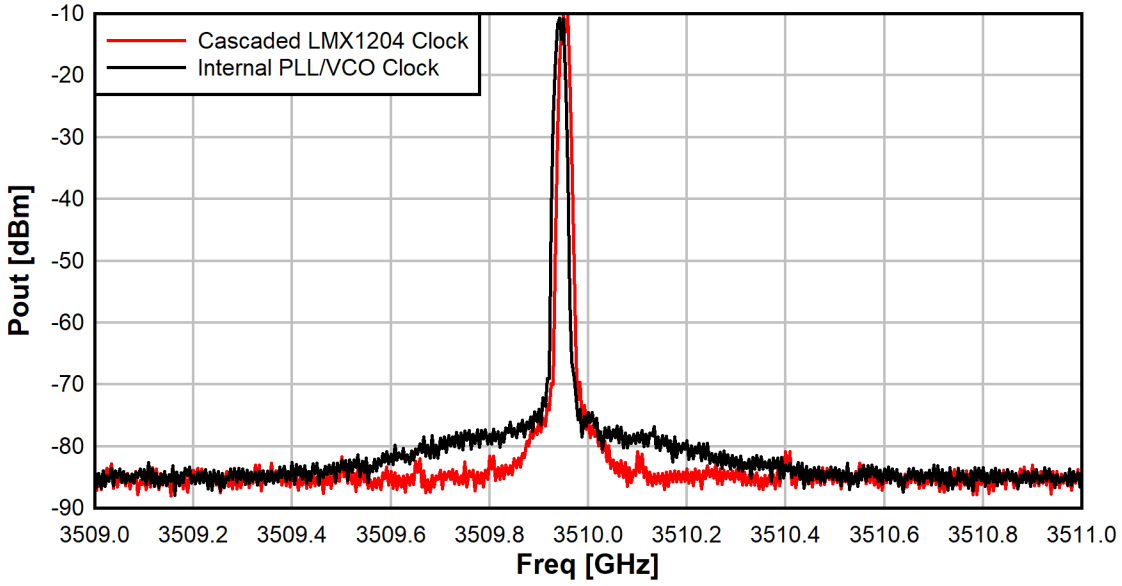

Figure 3-3. AFE7950 Output Spectrum Comparison

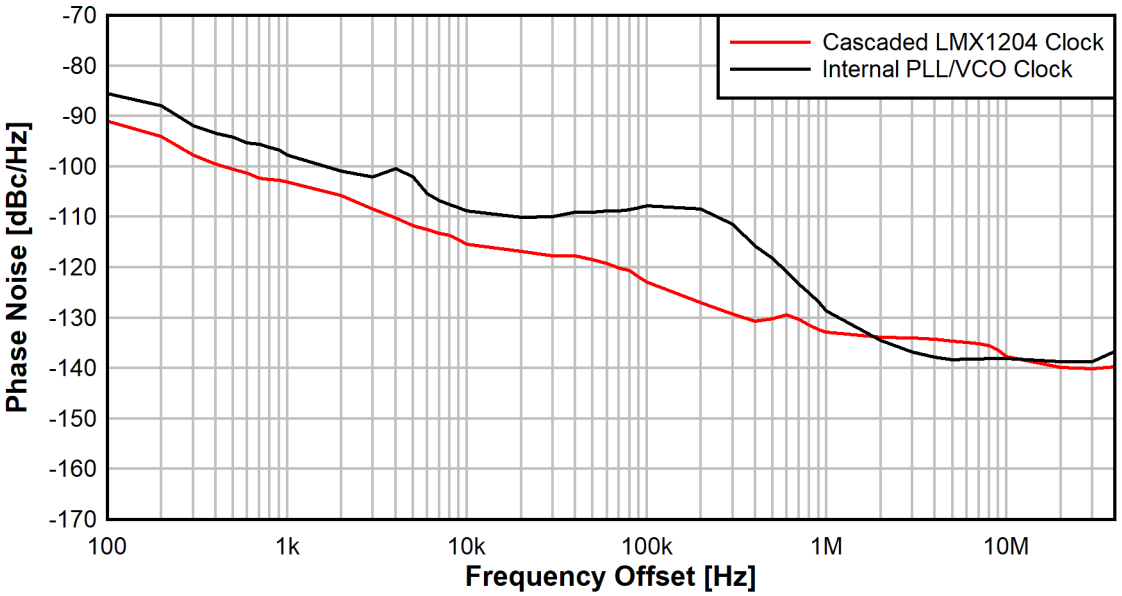

Figure 3-4. AFE7950 Signal Output Phase Noise Comparison

4 Conclusion

The LMX1204 is a good clock distribution device designed to disseminate a high-frequency, low phase-noise clock to a large array of data converter devices. Designers can cascade multiple layers of the LMX1204 to generate as many outputs for the system as needed. Use the internal multiplier feature of the LMX1204 to take a high-quality, low-frequency reference source to generate the required high-frequency sample clock. This approach eliminates the need for a dedicated high-frequency synthesizer. Performance is shown to be better than operation with the integrated PLL/VCO of the device. Given that systems already have a low-frequency reference and already need to distribute the clocks, this approach requires minimal extra devices. Further, for critical radar systems utilizing Doppler shifts where close-in phase-noise performance is critical, the multiplier approach yields better close-in performance compared to a standard synthesizer with equally good reference.

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