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ABSTRACT

LMX1205 is a versatile clocking product which can act as multiplier, divider, and buffer. When LMX1205 is used in the signal chain and deterministic nature across the signal chain is needed, certain sequence of events have to be performed. This deterministic nature of clock bringup in signal chain helps in predictable JESD link and post processing following it. This app note covers the sequence of events to be followed to maintain the deterministic nature.

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1 Introduction

Block diagram of the LMX1205 outputs is shown in [Figure 1-1](#). Consider a case, where LMX1205 is used as buffer/multiplier/divider in the clock path (CH0-CH3) and is required that all the channels (CH0-CH3) and sysref (SYS0-SYS3) need to be in sync and deterministic irrespective of the power supply toggling. This application note covers the steps to be followed to get that deterministic nature with lab measured waveforms using LMX1205 tics-pro. In general, sysref channels are low frequency clocks (<200MHz). Sync Signal is an external signal which can be both AC coupled and DC coupled. By default, it is AC coupled in LMX1205.

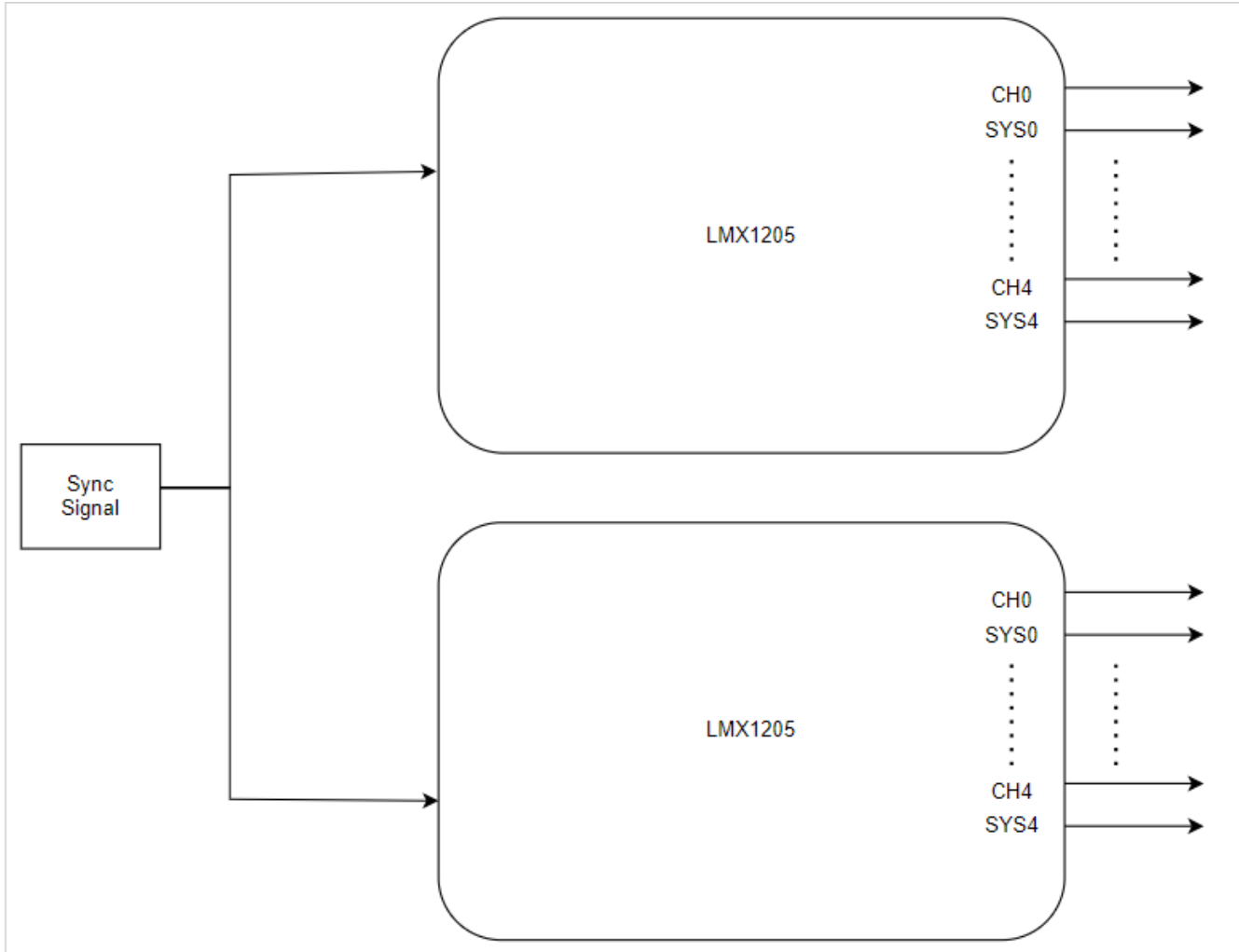


Figure 1-1. Sync Signal Driving Two LMX1205

There are different modes of operation to be taken care before we see the final synced output, which is discussed in the subsequent sections. Assuming (as shown in [Figure 1-2](#)) somehow the Sync Signal rise edge is coming on the clock negative edge. After some delay, SYS0 and SYS4 are synced and deterministic. Absolute delay depends on the divider used for sysref path. But for a particular sysref divider settings, no matter how many power cycles done, it is always deterministic. This application note focus on using sysref outputs for explaining the concepts and same is applicable for other channel outputs also. If sync signal is not going from low to high in one input clock window to two LMX1205s, then determinism is not achievable.

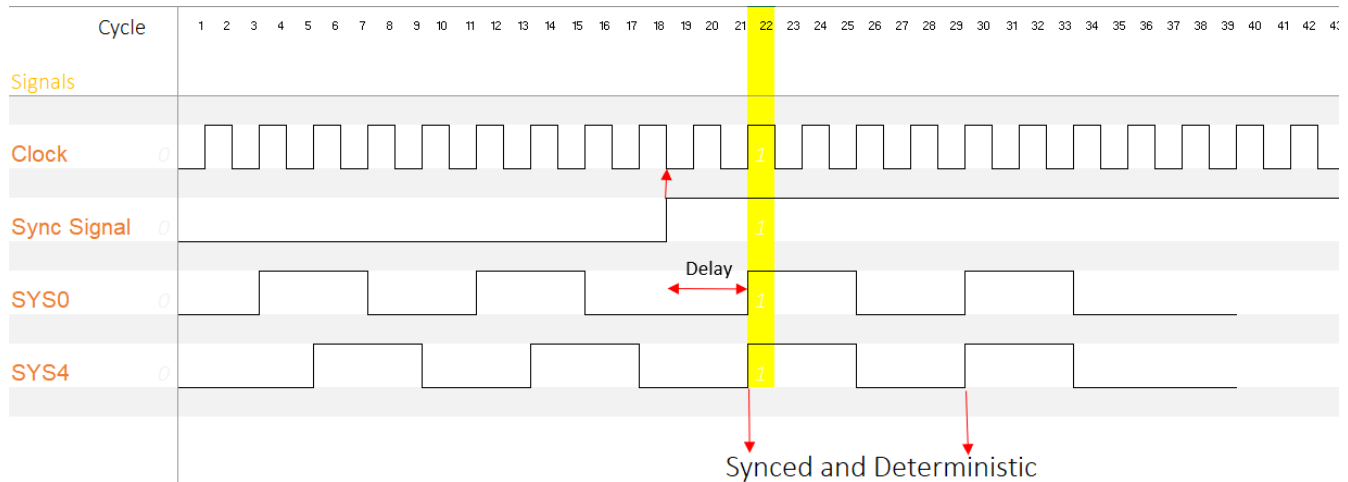


Figure 1-2. Pre and Post Sync Waveform Illustration

2 Where Does the Sync Signal Rise Come With Respect to the Clock Rise Edge?

To have reliable Sync operation, Sync signal needs to come on the fall edge of the clock. This can help avoid setup and hold regions of the flops inside LMX1205. What if the device generating the Sync signal do not have the option to delay the edge? Here comes the windowing feature. No matter where the Sync signal comes, windowing feature can help park this sync signal internally at the fall edge of the clock. Register(R18<5:0>, SYSREFREQ_DLY register) has to be written before doing sync operation whose value is obtained from windowing feature. In some cases, Sync signal can be periodic signal, which is internal multiple of clock period. In that case, on every low to high transition of Sync Signal, Syncing can happen. To stop that, there is an SYNC_STOP(R17<4>) option. If this bit is enabled, subsequent low to high transition on Sync Signal is ignored. All naming mentioned for the registers are as per the tics-pro Field names with tics-pro version 1.7.7.6.

As discussed previously, windowing needs to be done and then Sync. To enter into each of these modes, register have to be written as shown in [Table 2-1](#).

Table 2-1. LMX1205 Different Modes of Operation

SYSREFREQ_MODE (R17<1:0>)	Mode of operation
0	Sync Mode
1	Request Mode(Default)
2	Windowing Mode

When user is in Sync mode and Windowing mode, sysref signal is switched off. To get output from sysref, user has to enter Request mode post Windowing and Sync. [Figure 1-2](#) waveforms, showing sysref output in sync mode, are just for illustration purpose of the sync feature.

3 What is this Request Mode?

Request mode helps get glitch-free sysref outputs (SYS0-SYS3). Different modes of outputs are supported on SYS0-SYS3 as shown in [Table 3-1](#).

Table 3-1. LMX1205 Different Output Sysref Modes

SYSREF_MODE (R19<1:0>)	Sysref Mode of operation
0	Continuous mode
1	Pulse mode
2	Repeater Non-Sync mode
3	Repeater Sync mode

For this application note waveforms, Multi-site board of LMX1205 is used where 3 devices are present namely as primary, two secondary (secondary1 and secondary2). Following [Figure 3-1](#), shows the top level arrangement of the Multi-site board.

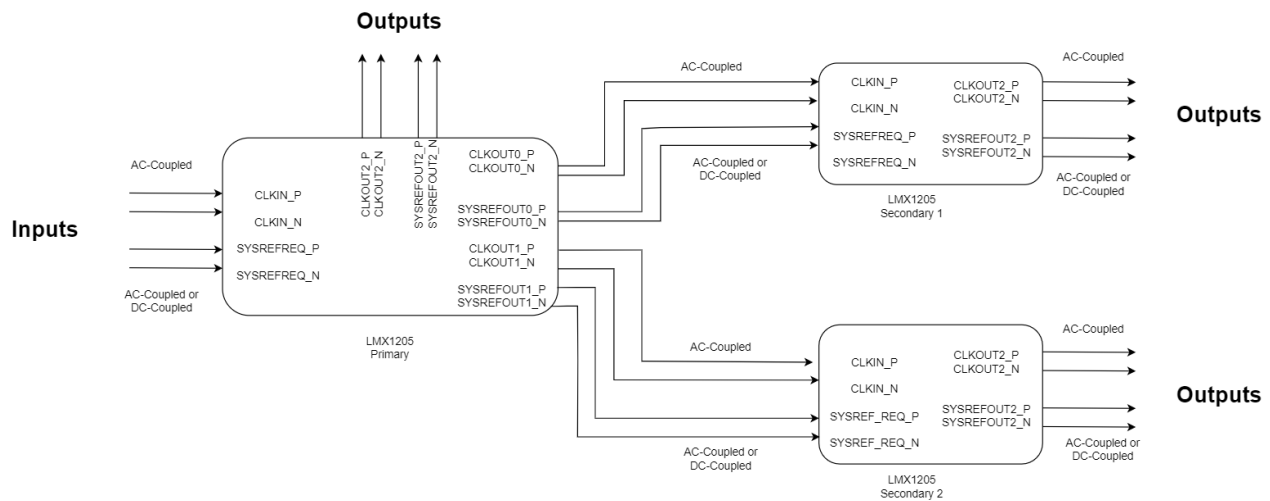


Figure 3-1. Multiple LMX1205 Configuration

[Table 3-2](#) summarizes the configuration used for the waveforms taken on the multi-site board. Secondary1 and secondary2 device has the same configuration. Naming of the Pins are as per the [LMX1205 Low-Noise, High-Frequency JESD Buffer/Multiplier/Divider](#), data sheet.

Table 3-2. Pin Configurations for Multiple LMX1205 on Multi-site Board

Primary Device	Pin Names (Pin number)	Format	Secondary1 Device	Pin Names (Pin number)	Format
Input	CLKIN_P (6)/ CLKIN_N (7)	AC Coupled	Input	CLKIN_P (6)/ CLKIN_N (7)	AC Coupled
	SYSREFREQ_P (2)/ SYSREFREQ_N (3)	50Ohm Termination		SYSREFREQ_P (2)/ SYSREFREQ_N (3)	DC Coupled
Outputs	CLKOUT2_P (33)/ CLKOUT2_N (32)	AC Coupled	Outputs	CLKOUT2_P (33)/ CLKOUT2_N (32)	AC Coupled
	SYSREFOUT2_P (30)/ SYSREFOUT2_N (29)	AC Coupled		SYSREFOUT2_P (33)/ SYSREFOUT2_N (32)	AC Coupled

Flow chart shown in [Figure 3-2](#), highlighting the sequence of steps to be followed when secondary1 device (driven by CH0 output from Primary) is supposed to be deterministic. Same applies for Secondary2 device except that different channel (CH1) from Primary device output drives the input pins.

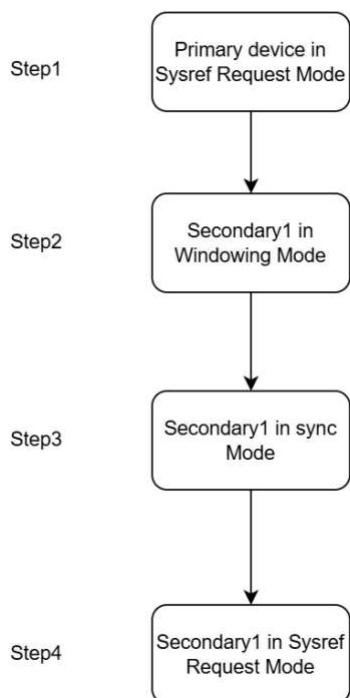


Figure 3-2. Sequence of Events on LMX1205 Multi-site Board

Assuming that secondary1 and secondary2 device needs to be setup such that it is always deterministic. During step1 from [Figure 3-2](#), load the tics pro details(See Appendix step1) such that Primary device is in sysref request mode. Output of Primary SYSREFOUT0/1_P/N drives the secondary 1 and 2 SYSREFREQ_P/N input pins and input respective setting needs to be written to that particular device. [Table 3-3](#) summarizes the different termination configurations.

Table 3-3. Input Termination Settings of LMX1205

SYSREFREQ_VCM(R16<1:0>)	Input mode for Pin 2,3 (SYSREFREQ_P/N)
0	AC Coupled
1	Pin P biased higher than pin M (AC coupled)
2	Pin M is biased higher than pin P (AC coupled)
3	DC Coupled

Multi-site board has 3 devices as discussed. On-board mux is present which write to only one device at a time based on the select lines. SEL0 and SEL1 are the two select lines which can be configured through tics-pro GUI under user controls --> Pins tab. Before writing to any device, make sure that device is selected through [Table 3-4](#).

Table 3-4. Multi-site Device Selection Settings in Tics-pro

SEL1	SEL0	Device to be written
0	0	Primary
0	1	Secondary1
1	0	Secondary2

After loading the tics pro file on primary device, continuous sysref signal can be coming on primary device output. If pulse mode needs to be engaged at primary output, give Low to High pulse at the Primary input Pin 2 using SPI registers SYSREFREQ_INPUT (R17<7:6>) by toggling from 1(decimal) to 3(decimal) and SYSREF_MODE as 1 . This can generate pulses at sysref output of primary in pulse mode. Secondary1 and Secondary2 needs to be kept in windowing mode using tics-pro(See Appendix step2) and generate pulse at the primary output. Before doing windowing, give 1 to 0 toggle for the register SYSREFREQ_CLR

(R17<2>). Read the windowing code(rb_CLKPOS R30<15:0>) from the secondary1 and secondary2 devices. If there is a continuous signal at the primary output, on every low to high transition, windowing keeps happening in secondary1 and secondary2. Readback of the windowing keeps changing, so to avoid that SYSWND_UPDATE_STOP(R17<5>) needs to be made 1. Write the SYSREFREQ_DLY position register in secondary1 and secondary2 device. This can make sure that rise edge at the pin of secondary1 and secondary2 can always align at the fall edge of the clock input through some internal delays.

Under calculations tab, there is a way to check what value to be written to SYSREFREQ_DLY register. When “Read CLKPOS” check button is pressed, it automatically reads rb_CLKPOS and calculates SYSREFREQ_DLY value. As shown below for this case, SYSREFREQ_DLY to be written is 12. This is an example for 10GHz input clock. Similar windowing snapshot for 1GHz as clock input is shown [Figure 3-3](#).

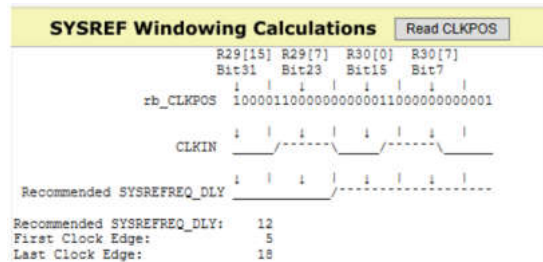


Figure 3-3. Sysref Windowing Tics-pro Snapshot Details for 10GHz

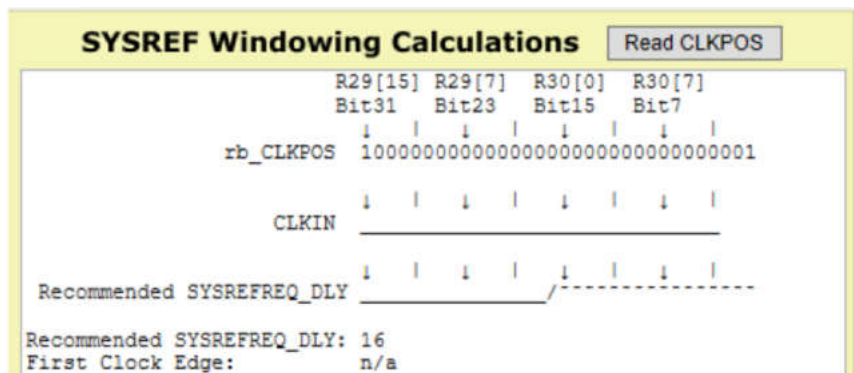


Figure 3-4. Sysref Windowing Tics-pro Snapshot Details for 1GHz

Make the secondary1 and secondary2 device in sync mode as shown in [Table 2-1](#) . Generate pulse at the primary output to secondary 1 and secondary 2 input (pin 3 and pin 4), this can make sure that both secondary1 and secondary2 are synced and can be deterministic.

Registers to be written on secondary1 and secondary2 to make devices sync after windowing:

1. SYSREFREQ_DLY
2. SYSREFREQ_CLR -->1-->0 toggle
3. SYSREFREQ_MODE -->0
4. SYNC_STOP-->1

After previous register writes, both secondary1 and secondary2 are synced. Make the secondary1 and secondary2 device in sysref request mode as shown in [Table 3-1](#). [Figure 3-5](#) shows the configuration where Primary is in continuous mode, secondary 1 and secondary2 are in continuous mode.

SYSREFREQ_MODE -->1 to enter request mode. As shown in [Figure 3-5](#), both secondary1 and secondary2 devices are deterministic.

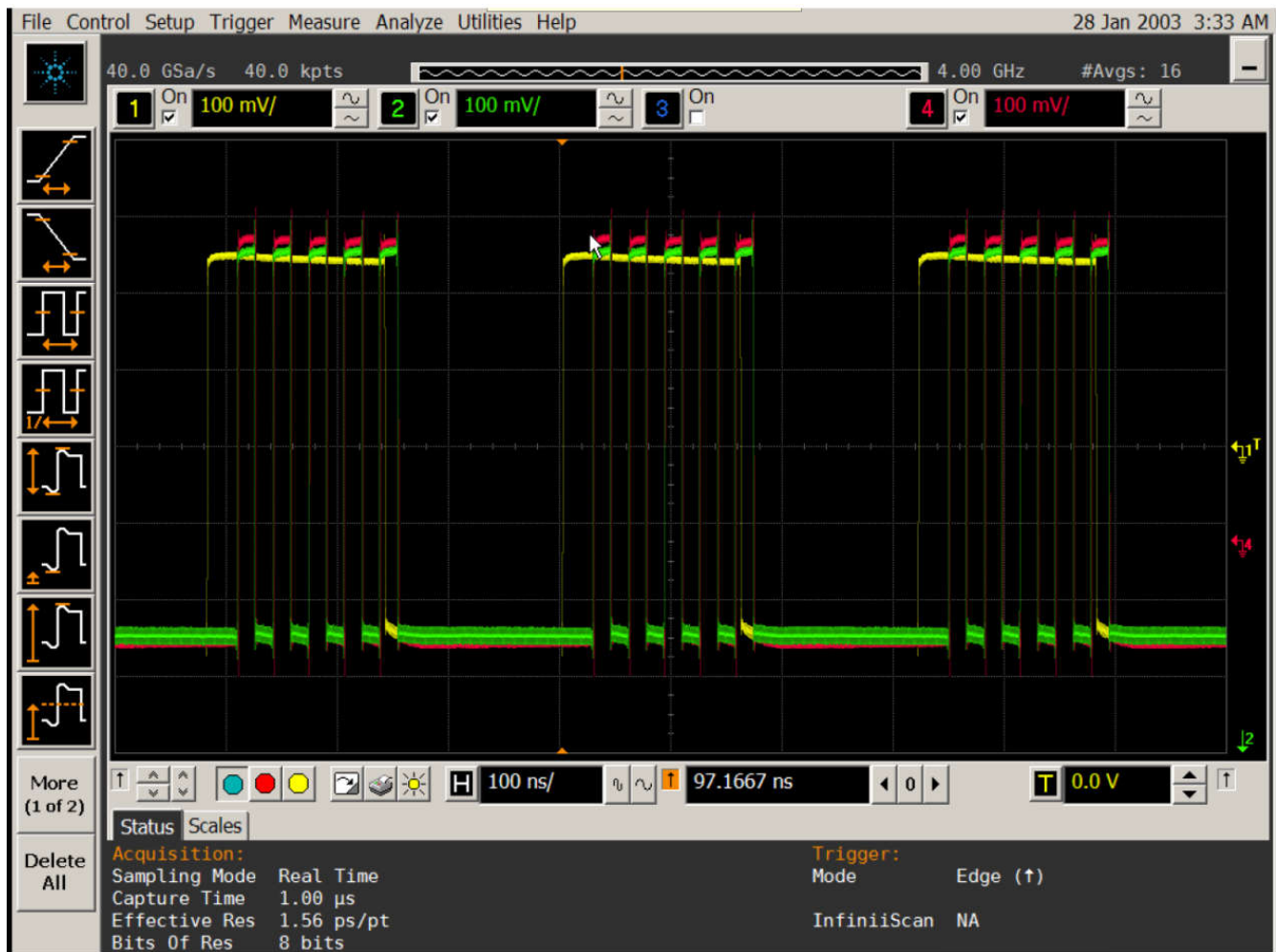


Figure 3-5. Synced Waveforms for Primary, Secondary1, and Secondary2 in Continuous Mode

Yellow: Continuous Primary sysrefout2_p

Red: Continuous Secondary1 sysrefout2_p

Green: Continuous Secondary2 sysrefout2_p

Frequencies used for the previous example:

CLKIN as 1GHz, Primary sysrefout2_p as 3.125MHz, Secondary1/2 sysrefout2_p as 31.25MHz

If the frequency of CLKIN is changed, make sure IQ divider value SYSREF_DLY_DIV(R20<15:14>) and frequency range settings (SYSREF_DLY_SCALE R16<7:6>) accordingly as shown in data sheet.

As shown previously, as primary is in continuous mode, when pin 3 is low, no sysref comes out. This can be avoided by pulling the pin3 internally high on secondary1 and secondary 2 using SPI as shown in [Table 3-5](#).

Table 3-5. Pin2 and Pin3 Configuration

SYSREFREQ_INPUT(R17<7:6>)	Input mode for Pin 2,3 (SYSREFREQ_P/N)
0	SYSREFREQ Pin Value
1	Internally pulled low through SPI
2	NA
3	Internally pulled high through SPI



Figure 3-6. Synced Waveforms for Primary, Secondary1, and Secondary2 With Continuous Secondary1 and Secondary2 in Continuous Mode

As shown in [Figure 3-6](#), Primary continuous pulse is bypassed in both secondary 1 and secondary2 device inputs.

As discussed in [Table 3-1](#) about different modes of sysref outputs, see the following section how the output waveforms looks like.

4 Pulse Mode

1. R17<7:6> is made 0. This makes secondary1 and secondary2 input pin3/4 to take from primary continuous signal.
2. SYSREF_PULSE_CNT(R19<5:2>) to be made 1, which generates one pulse at the output.
3. Figure 4-1 shows the 1 pulse output on Secondary1 sysrefout2_p(red) and Secondary2 sysrefout2_p(green).

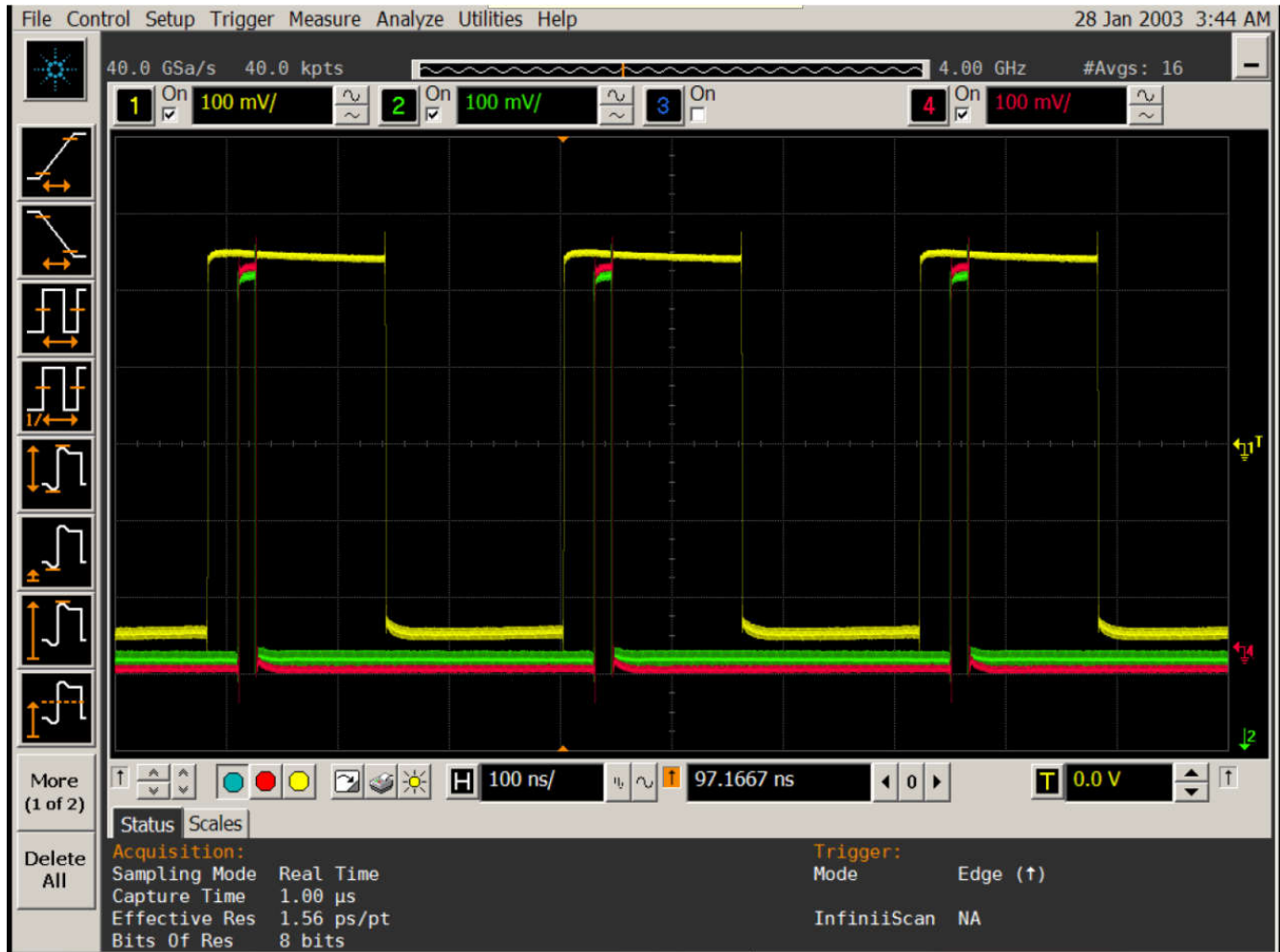


Figure 4-1. Synced Waveforms for Secondary1, and Secondary2 in Pulse Mode with Primary in Continuous Mode.

5 Repeater Non-sync Mode

1. SYSREF_MODE is made 2.
2. Figure 5-1 shows the repeated non-synced output on Secondary1 sysrefout2_p(red) and Secondary2 sysrefout2_p(green) from Primary sysrefout2_p(yellow).
3. Windowing is not necessary for repeater mode.
4. Zoomed version of rising edges of Primary, Secondary1 and secondary2 are shown in Figure 5-2.

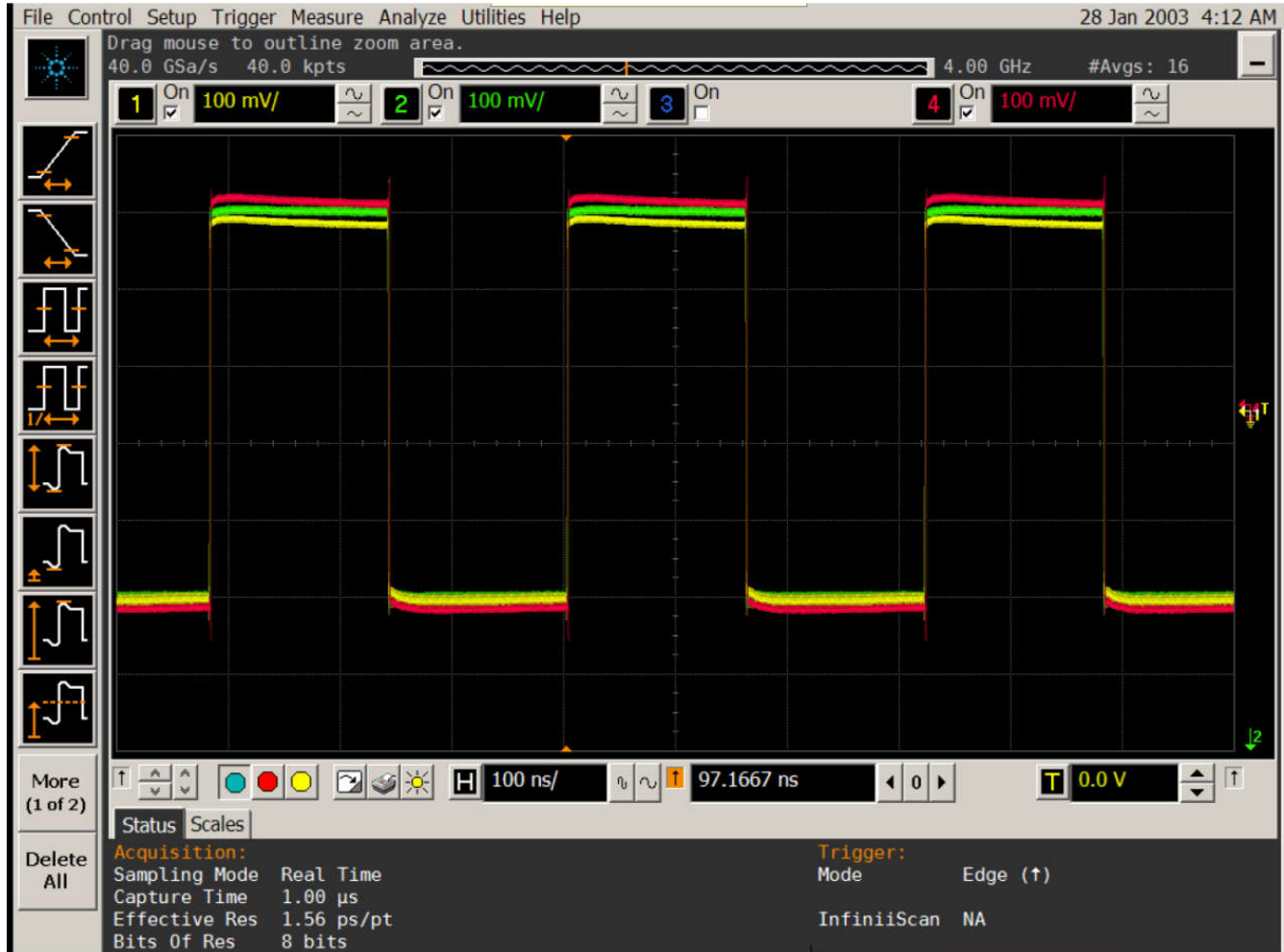


Figure 5-1. Waveforms for Secondary1, and Secondary2 in Repeater Non-sync Mode With Primary in Continuous Mode



Figure 5-2. Waveforms for Secondary1, and Secondary2 in Repeater Non-sync Mode with Primary in Continuous Mode (Zoomed in)

6 Repeater Sync Mode

1. SYSREF_MODE is made 3 Figure 6-1 shows the repeated synced output on Secondary1 sysrefout2_p(red) and Secondary2 sysrefout2_p(green) from Primary sysrefout2_p(yellow).
2. Major difference between Figure 6-1(repeater sync) an Figure 5-2 (repeater non-sync) is that in repeater sync mode, pin3 is synced with the input clock and 2 delay clock cycles is seen. In this example, Clock input is 1GHz, so extra delay of 2ns is expected.

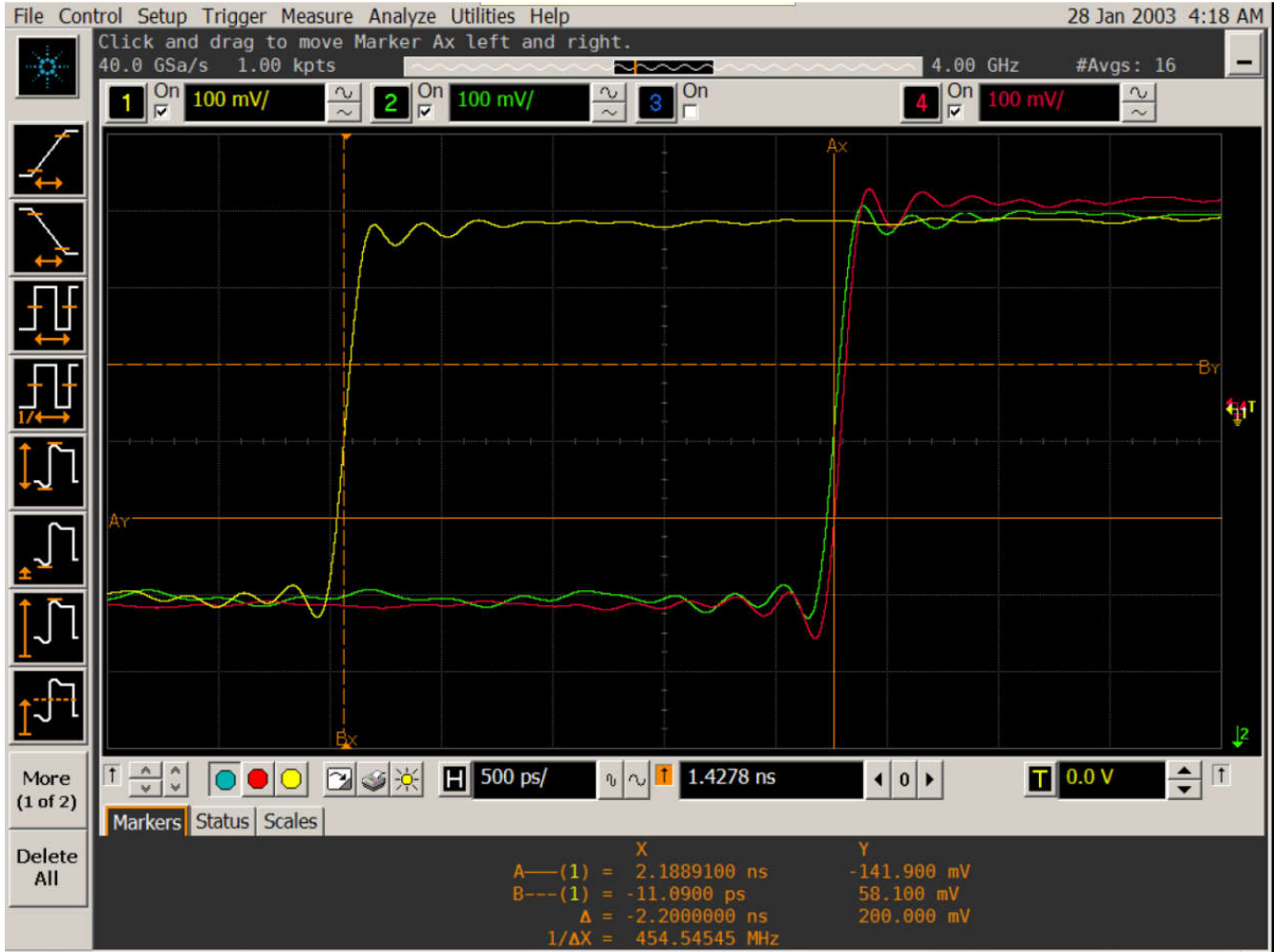


Figure 6-1. Waveforms for Secondary1, and Secondary2 in Repeater Sync Mode with Primary in Continuous Mode

7 Summary

This application note covers the theory portion of the Windowing, sync, sysref feature of LMX1205 and lab evaluation waveforms using multi-site board are shown for better understanding of the theory.

8 References

- Texas Instruments, [LMX1205 Low-Noise, High-Frequency JESD Buffer/Multiplier/Divider](#), data sheet.

9 Appendix A

Primary tics-pro file: save the below text as .tcs file and load in the primary device. SEL0=0 and SEL1=0

```
[SETUP]
ADDRESS=888
CLOCK=8
DATA=4
LE=2
PART=LMX1205
IFACE=SPI_CLKLOW
ADDRESS_I2C=0x0
[PINS]
PINNAME0=SEL0
LOCATION00=0
PINVALUE00=False
PINNAME01=SEL1
LOCATION01=1
PINVALUE01=False
[MODES]
NAME00=R77
VALUE00=5046272
NAME01=R55
VALUE01=3604486
NAME02=R54
VALUE02=3538944
NAME03=R37
VALUE03=2424832
NAME04=R36
VALUE04=2394439
NAME05=R32
VALUE05=2097152
NAME06=R31
VALUE06=2031616
NAME07=R30
VALUE07=1966080
NAME08=R29
VALUE08=1900544
NAME09=R27
```

VALUE09=1795593
NAME10=R26
VALUE10=1704145
NAME11=R25
VALUE11=1638908
NAME12=R24
VALUE12=1573372
NAME13=R23
VALUE13=1507836
NAME14=R22
VALUE14=1442300
NAME15=R21
VALUE15=1376764
NAME16=R20
VALUE16=1343810
NAME17=R19
VALUE17=1245252
NAME18=R18
VALUE18=1179648
NAME19=R17
VALUE19=1114305
NAME20=R16
VALUE20=1048624
NAME21=R15
VALUE21=983042
NAME22=R14
VALUE22=917636
NAME23=R13
VALUE23=852011
NAME24=R12
VALUE24=786475
NAME25=R11
VALUE25=745097
NAME26=R10
VALUE26=679561
NAME27=R9
VALUE27=614025

NAME28=R8
VALUE28=548489
NAME29=R7
VALUE29=458765
NAME30=R6
VALUE30=393229
NAME31=R5
VALUE31=327693
NAME32=R4
VALUE32=262157
NAME33=R3
VALUE33=196608
NAME34=R2
VALUE34=131327
NAME35=R1
VALUE35=65547
NAME36=R0
VALUE36=0
[FLEX]
CLK0_FREQ=12800.0
CLK1_FREQ=12800.0
CLK2_FREQ=12800.0
CLK3_FREQ=12800.0
CLKIN_FREQ=12800
LOGICLK_FREQ=200.0
LOGISYSREF_FREQ=40.0
SYSREF0_FREQ=40.0
SYSREF1_FREQ=40.0
SYSREF2_FREQ=40.0
SYSREF3_FREQ=40.0
SYSREF_FREQ_FREQ=
btnMULT_CAL=Calibrate Multiplier
btnRB_LD=Read Lock Detect
btnREAD_SYSWIN=Read SYSWIN Position
btnREAD_TEMP=Read
btnSetEdgeNeg0=- Edge
btnSetEdgeNeg1=- Edge

btnSetEdgeNeg2-- Edge
btnSetEdgeNeg3-- Edge
btnSetEdgeNeg4--
btnSetEdgePos0=Min
btnSetEdgePos1=Min
btnSetEdgePos2=Min
btnSetEdgePos3=Min
btnSetEdgePos4=Min
spnSYSDLY0=0
spnSYSDLY1=0
spnSYSDLY2=0
spnSYSDLY3=0
spnSYSDLY4=0
stCLKDLY0=19.375 ps
stCLKDLY1=0.625 ps
stCLKDLY2=0.625 ps
stCLKDLY3=
stCLKIN_DLY=
stCLKPOS=
stCLKPWR0=
stCLKPWR1=
stCLKPWR2=
stCLKPWR3=
stCURRENT=1208 mA
stClkPosSkew=
stDELAY_RANGE=[-312.50, 311.27] ps
stDELAY_STEPSIZE=1.23 ps
stDIV=n/a
stFACTOR=
stFINTERPOLATOR=3200.0
stFSMCLK=25.00000 MHz
stFSYSREF=
stMULT=n/a
stSYSDLY0=95.00 ps
stSYSDLY1=95.00 ps
stSYSDLY2=95.00 ps
stSYSDLY3=95.00 ps

stSYSDLY4=95.00 ps
stSYSPWR0=400.00 Vpp
stSYSPWR1=400.00 Vpp
stSYSPWR2=400.00 Vpp
stSYSPWR3=400.00 Vpp
stSYSVCM0=1.40 V
stSYSVCM1=1.40 V
stSYSVCM2=1.40 V
stSYSVCM3=1.40 V
stSysRefReqDlyRecommend=
stTJ=
AUTOSET_CLKPOS=0
AUTOSET_LOGICLK_DIV_PRE=1
AUTOSET_SMCLK=1
AUTOSET_SYSREFREQ_DLY_SCALE=0
AUTOSET_SYSREFREQ_DLY_STEP=1
AUTOSET_SYSREF_DIV_PRE=1
AUTOSET_SYSREF_DLY_DIV=1
WINDOW_STATUS=
btnREAD_WINDOW=Read CLKPOS
tcBoundaryCode=403.0
tcCLKDLY0=180.00 ps
tcCLKDLY1=180.00 ps
tcCLKDLY2=180.00 ps
tcCLKDLY3=180.00 ps
tcCLKDLY4=300.00 ps
tcCLKSYSDLY0=95.00 ps
tcCLKSYSDLY1=95.00 ps
tcCLKSYSDLY2=95.00 ps
tcCLKSYSDLY3=95.00 ps
tcCLKSYSDLY4=95.00 ps
tcCurrent_CLKout=
tcCurrent_Core=
tcCurrent_LOGICLKout=
tcCurrent_LOGISYSREFout=
tcCurrent_SYSREFGen=
tcCurrent_SYSREFout=

```
tcCurrent_Total=  
tcSYSDLY0=275.00 ps  
tcSYSDLY1=275.00 ps  
tcSYSDLY2=275.00 ps  
tcSYSDLY3=275.00 ps  
tcSYSDLY4=395.00 ps  
tcStep0=254  
tcStep1=254  
tcStep2=254  
tcStep3=254  
tcStep4=254
```

Secondary 1 and secondary2 tics-pro file: save the below text as .tcs file and load in the secondary1 (SEL0=1 and SEL1=0) and secondary2 device (SEL0=0 and SEL1=1)

```
[SETUP]  
ADDRESS=888  
CLOCK=8  
DATA=4  
LE=2  
PART=LMX1205  
IFACE=SPI_CLKLOW  
ADDRESS_I2C=0x0  
[PINS]  
PINNAME00=SEL0  
LOCATION00=0  
PINVALUE00=False  
PINNAME01=SEL1  
LOCATION01=1  
PINVALUE01=True  
[MODES]  
NAME00=R77  
VALUE00=5046272  
NAME01=R55  
VALUE01=3604480  
NAME02=R54  
VALUE02=3538944  
NAME03=R37  
VALUE03=2424832
```

NAME04=R36
VALUE04=2394439
NAME05=R32
VALUE05=2097152
NAME06=R31
VALUE06=2031616
NAME07=R30
VALUE07=1966080
NAME08=R29
VALUE08=1900544
NAME09=R27
VALUE09=1795593
NAME10=R26
VALUE10=1704145
NAME11=R25
VALUE11=1638908
NAME12=R24
VALUE12=1573372
NAME13=R23
VALUE13=1507836
NAME14=R22
VALUE14=1442300
NAME15=R21
VALUE15=1376764
NAME16=R20
VALUE16=1310754
NAME17=R19
VALUE17=1245248
NAME18=R18
VALUE18=1179648
NAME19=R17
VALUE19=1114114
NAME20=R16
VALUE20=1048579
NAME21=R15
VALUE21=983042
NAME22=R14

VALUE22=917636
NAME23=R13
VALUE23=852011
NAME24=R12
VALUE24=786475
NAME25=R11
VALUE25=745097
NAME26=R10
VALUE26=679561
NAME27=R9
VALUE27=614025
NAME28=R8
VALUE28=548489
NAME29=R7
VALUE29=458765
NAME30=R6
VALUE30=393229
NAME31=R5
VALUE31=327693
NAME32=R4
VALUE32=262157
NAME33=R3
VALUE33=196608
NAME34=R2
VALUE34=131327
NAME35=R1
VALUE35=65547
NAME36=R0
VALUE36=0
[FLEX]
CLK0_FREQ=12800.0
CLK1_FREQ=12800.0
CLK2_FREQ=12800.0
CLK3_FREQ=12800.0
CLKIN_FREQ=12800
LOGICLK_FREQ=200.0
LOGISYSREF_FREQ=400.0

SYSREF0_FREQ=400.0
SYSREF1_FREQ=400.0
SYSREF2_FREQ=400.0
SYSREF3_FREQ=400.0
SYSREF_FREQ=
btnMULT_CAL=Calibrate Multiplier
btnRB_LD=Read Lock Detect
btnREAD_SYSWIN=Read SYSWIN Position
btnREAD_TEMP=Read
btnSetEdgeNeg0=- Edge
btnSetEdgeNeg1=- Edge
btnSetEdgeNeg2=- Edge
btnSetEdgeNeg3=- Edge
btnSetEdgeNeg4=-
btnSetEdgePos0=Min
btnSetEdgePos1=Min
btnSetEdgePos2=Min
btnSetEdgePos3=Min
btnSetEdgePos4=Min
spnSYSDLY0=0
spnSYSDLY1=0
spnSYSDLY2=0
spnSYSDLY3=0
spnSYSDLY4=0
stCLKDLY0=19.375 ps
stCLKDLY1=0.625 ps
stCLKDLY2=0.625 ps
stCLKDLY3=
stCLKIN_DLY=
stCLKPOS=
stCLKPWR0=
stCLKPWR1=
stCLKPWR2=
stCLKPWR3=
stCURRENT=1228 mA
stClkPosSkew=
stDELAY_RANGE=[-78.13, 77.82] ps


```
stDELAY_STEPSIZE=0.31 ps
stDIV=n/a
stFACTOR=
stFINTERPOLATOR=12800.0
stFSMCLK=25.00000 MHz
stFSYSREF=
stMULT=n/a
stSYSDLY0=95.00 ps
stSYSDLY1=95.00 ps
stSYSDLY2=95.00 ps
stSYSDLY3=95.00 ps
stSYSDLY4=95.00 ps
stSYSPWR0=400.00 Vpp
stSYSPWR1=400.00 Vpp
stSYSPWR2=400.00 Vpp
stSYSPWR3=400.00 Vpp
stSYSVCM0=1.40 V
stSYSVCM1=1.40 V
stSYSVCM2=1.40 V
stSYSVCM3=1.40 V
stSysRefReqDlyRecommend=
stTJ=
AUTOSET_CLKPOS=0
AUTOSET_LOGICLK_DIV_PRE=1
AUTOSET_SMCLK=1
AUTOSET_SYSREFREQ_DLY_SCALE=0
AUTOSET_SYSREFREQ_DLY_STEP=1
AUTOSET_SYSREF_DIV_PRE=1
AUTOSET_SYSREF_DLY_DIV=1
WINDOW_STATUS=
btnREAD_WINDOW=Read CLKPOS
tcBoundaryCode=22.0
tcCLKDLY0=180.00 ps
tcCLKDLY1=180.00 ps
tcCLKDLY2=180.00 ps
tcCLKDLY3=180.00 ps
tcCLKDLY4=300.00 ps
```

tcCLKSYSDLY0=95.00 ps
tcCLKSYSDLY1=95.00 ps
tcCLKSYSDLY2=95.00 ps
tcCLKSYSDLY3=95.00 ps
tcCLKSYSDLY4=95.00 ps
tcCurrent_CLKout=
tcCurrent_Core=
tcCurrent_LOGICLKout=
tcCurrent_LOGISYSREFout=
tcCurrent_SYSREFGen=
tcCurrent_SYSREFout=
tcCurrent_Total=
tcSYSDLY0=275.00 ps
tcSYSDLY1=275.00 ps
tcSYSDLY2=275.00 ps
tcSYSDLY3=275.00 ps
tcSYSDLY4=395.00 ps
tcStep0=254
tcStep1=254
tcStep2=254
tcStep3=254
tcStep4=254

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