

## **DP83848-EP Reliability Report**

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### **ABSTRACT**

This report presents the reliability and qualification results for the DP83848-EP single port 10/100 MB/s ethernet physical layer transceiver. The DP83848-EP is manufactured with a controlled baseline and has the following:

- Product Traceability
- Extended Product-Change Notification

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### **Trademarks**

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## 1 Texas Instruments Enhanced Product Qualification and Reliability Report

TI qualification testing is a risk mitigation process that is engineered to assure device longevity in customer applications. Wafer fabrication process and package level reliability are evaluated in a variety of ways that may include accelerated environmental test conditions with subsequent derating to actual use conditions. Manufacturability of the device is evaluated to verify a robust assembly flow and assure continuity of supply to customers, TI Enhanced Products are qualified with industry standard test methodologies performed to the intent of Joint Electron Devices Engineering Council (JEDEC) standards and procedures. Texas Instruments Enhanced Products are certified to meet GEIA-STD-0002-1 [Aerospace Qualified Electronic Components](#).

## 2 Qualification by Similarity (Qualification Family)

A new device can be qualified either by performing a full scale quality and reliability test on the actual device or using previously qualified devices through "Qualification by Similarity" (QBS) rules. By establishing similarity between the new device and those previously qualified, repetitive tests are eliminated, allowing for timely production release. When adopting QBS methodology, the emphasis is on qualifying the differences between a previously qualified product and the new product under consideration. The QBS rules for a technology, product, test parameter, or package defines which attributes are required to remain fixed in order for the QBS rules to apply. The attributes that are expected and allowed to vary are reviewed and a QBS plan is developed, based on the reliability impact assessment above, specifying what subset of the full complement of environmental stresses is required to evaluate the reliability impact of those variations. Each new device is reviewed for the conformance to the QBS rule sets applicable to the device. See the JEDEC JESD47 for more information.

**Figure 1. Device Baseline**

Device Baseline <sup>1</sup>			
<i>TI Device:</i>	<b>DP83848MPHPEP</b>	<i>Assembly Site:</i>	TITL (Taiwan)
<i>DLA VID:</i>	V62/12615-01XE	<i>Test Site:</i>	TIEM (Malaysia)
<i>Wafer Fab:</i>	Maine Fab(USA)	<i>Pin/Package Type:</i>	HTQFP (PHP)   48
<i>Fab Process:</i>	CMOS9T.5	<i>Leadframe:</i>	Cu
<i>Fab Technology:</i>	CMOS9T	<i>Termination Finish:</i>	NiPdAu
<i>Die Revision:</i>	- ("-" denotes initial release)	<i>Mount Compound:</i>	Henkel FS849-TI
<i>Die Name:</i>	GHDP83848ABH1	<i>Bond Wire:</i>	24.8 μm Au
<i>ESD CDM:</i>	±4000V	<i>Mold Compound:</i>	Sumitomo EME-G700LB
<i>ESD HBM:</i>	±1500V	<i>Moisture Sensitivity:</i>	MSL 4 / 260°C
<sup>1</sup> Baseline information in effect as of the date of this report.			

Device Baseline <sup>1</sup>			
<i>TI Device:</i>	<b>DP83848MPTBEP</b>	<i>Assembly Site:</i>	ASEK (Taiwan)
<i>DLA VID:</i>	V62/12615-01YE	<i>Test Site:</i>	TIEM (Malaysia)
<i>Wafer Fab:</i>	Maine Fab(USA)	<i>Pin/Package Type:</i>	HLQFP (PHP)   48
<i>Fab Process:</i>	CMOS9T.5	<i>Leadframe:</i>	Cu
<i>Fab Technology:</i>	CMOS9T	<i>Termination Finish:</i>	NiPdAu-Ag
<i>Die Revision:</i>	- ("-" denotes initial release)	<i>Mount Compound:</i>	Hitachi EN_4900GC
<i>Die Name:</i>	GHDP83848ABH1	<i>Bond Wire:</i>	25.4 μm Au
<i>ESD CDM:</i>	±4000V	<i>Mold Compound:</i>	Sumitomo EME-G631H
<i>ESD HBM:</i>	±1500V	<i>Moisture Sensitivity:</i>	MSL 3 / 260°C
<sup>1</sup> Baseline information in effect as of the date of this report.			

**Figure 2. Enhanced Products New Device Qualification Matrix**

<b>Enhanced Products New Device Qualification Matrix</b>				
Note that qualification by similarity ("qualification family") per JEDEC JESD47 is allowed				
Description	Condition	Sample Size Used/Rejects	Lots Required	Test Method
<i>Electromigration</i>	Maximum Recommended Operating Conditions	N/A	N/A	Per TI Design Rules
<i>Wire Bond Life</i>	Maximum Recommended Operating Conditions	N/A	N/A	Per TI Design Rules
<i>Electrical Characterization</i>	TI Data Sheet	15	3	N/A
<i>Electrostatic Discharge Sensitivity</i>	HBM CDM	3 units/voltage	N/A	EIA/JESD22-A114 EIA/JESD22-C101
<i>Latch-up</i>	Per Technology	5/0	3	EIA/JESD78
<i>Physical Dimensions</i>	TI Data Sheet	5/0	1	EIA/JESD22- B100
<i>Thermal Impedance</i>	Theta-JA on board	Per Pin-Package	N/A	EIA/JESD51
<i>Bias Life Test</i>	125°C / 1000 hours or equivalent	45/0	3	JESD22-A108*
<i>Biased Humidity</i> or <i>Biased HAST</i>	85°C / 85% / 1000 hours or 130°C / 85% / 96 hours	77/0	3	JESD22-A101*  JESD22-A110*
<i>Extended Biased Humidity</i> or <i>Extended Biased HAST</i>	85°C / 85% / 2600 hours (for reference) or 130°C / 85% / 250 hours (for reference)	77/0	1	JESD22-A101*  JESD22-A110*
<i>Unbiased HAST</i>	130°C / 85% / 96 hours	77/0	3	JESD22-A.118*
<i>Temperature Cycle</i>	-65°C to +150°C non-biased for 500 cycles	77/0	3	JESD22-A104*
<i>Solder Heat</i>	260°C for 10 seconds	22/0	1	JESD22-B106
<i>Resistance to Solvents</i>	Ink symbol only	12/0	1	JESD22-B107
<i>Solderability</i>	Condition A (steam age for 8 hours)	22/0	1	ANSI/J-STD-002-92
<i>Flammability</i>	Method A / Method B	5/0	1	UL-1964
<i>Bond Shear</i>	Per wire size	5 units x 30/0 bonds	3	JESD22-B116
<i>Bond Pull Strength</i>	Per wire size	5 units x 30/0 bonds	3	ASTMF-459
<i>Die Shear</i>	Per die size	5/0	3	TM2019
<i>High Temp Storage</i>	150 °C / 1,000 hours	15/0	3	JESD22-A103-A*
<i>Moisture Sensitivity</i>	Surface Mount Only	12	1	J-STD-020-A*
*Precondition performed per JEDEC Std. 22, Method A112/A113				

### 3 Technology Family FIT/MTBF Data

Mean Time Between Fails (MTBF) and Failures in Time (FIT) rates are device reliability statistics calculated based on data collected from TI's internal reliability testing (life test). TI's DPPM/FIT/MTBF Estimator Search Tool reports generic data based on technology groupings and shows conditions under which the rates were derived. All terms used in the tool and definitions can be found on the TI reliability terminology page. Failure rates are summarized by technology and mapped to the associated material part numbers. The failure rates are highly dependent on the number of units tested, therefore, it is not recommended to compare failure rates.

Visit the TI DPPM/FIT/MTBF Estimator Search Tool at [www.ti.com/quality/docs/estimator.tsp](http://www.ti.com/quality/docs/estimator.tsp).

### 4 Device Family Qualification Data

TI's Qualification Summary Search Tool reports generic qualification data representative of the material sets, processes, and manufacturing sites used by the device family and may not include all of the testing performed for a specific EP device. See the [Figure 2](#) for the full suite of qualification testing performed to release Enhanced Product devices.

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### Quality and Reliability Data Disclaimer

The attached quality and reliability information is specific to the TI Enhanced Plastic product family of plastic encapsulated commercial-off-the-shelf (COTS) semiconductor products and components. Due to possible differences in product assembly and test baselines, this information is NOT APPLICABLE to TI standard, industrial, or automotive catalog commercial products.

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