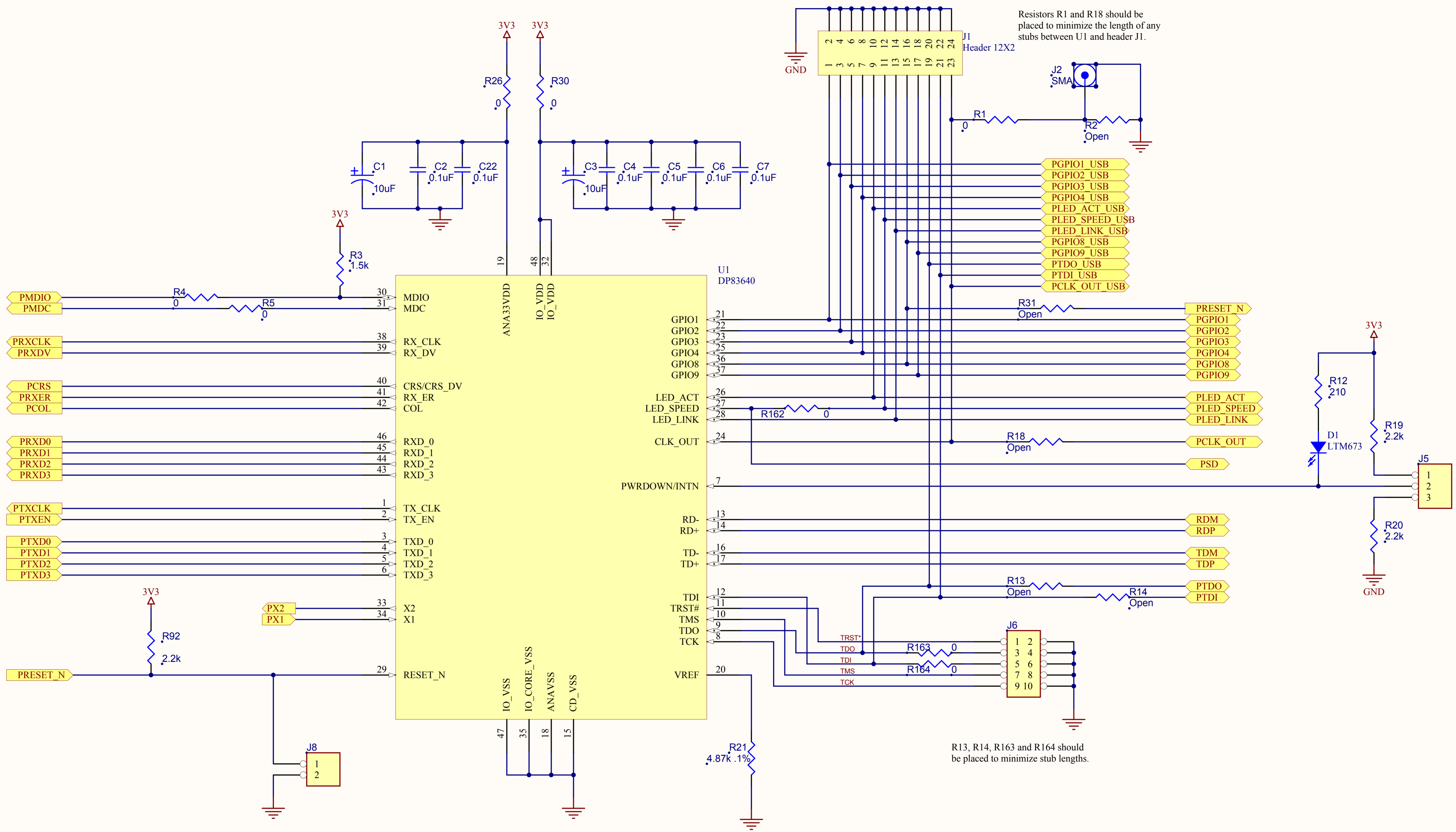


AN_EN	AN1	AN0	AUTO-NEG FORCED MODES	
0	0	0	10BASE-T	HALF-DUPLEX
0	0	1	10BASE-T	FULL-DUPLEX
0	1	0	100BASE-TX	HALF-DUPLEX
0	1	1	100BASE-TX	FULL-DUPLEX

AN_EN	AN1	AN0	AUTO-NEG ADVERTISED MODES	
1	0	0	10BASE-T	HALF/FULL-DUPLEX
1	0	1	100BASE-TX	HALF/FULL-DUPLEX
1	1	0	100BASE-TX	FULL-DUPLEX
1	1	1	10BASE-T	HALF/FULL-DUPLEX
			100BASE-TX	HALF/FULL-DUPLEX

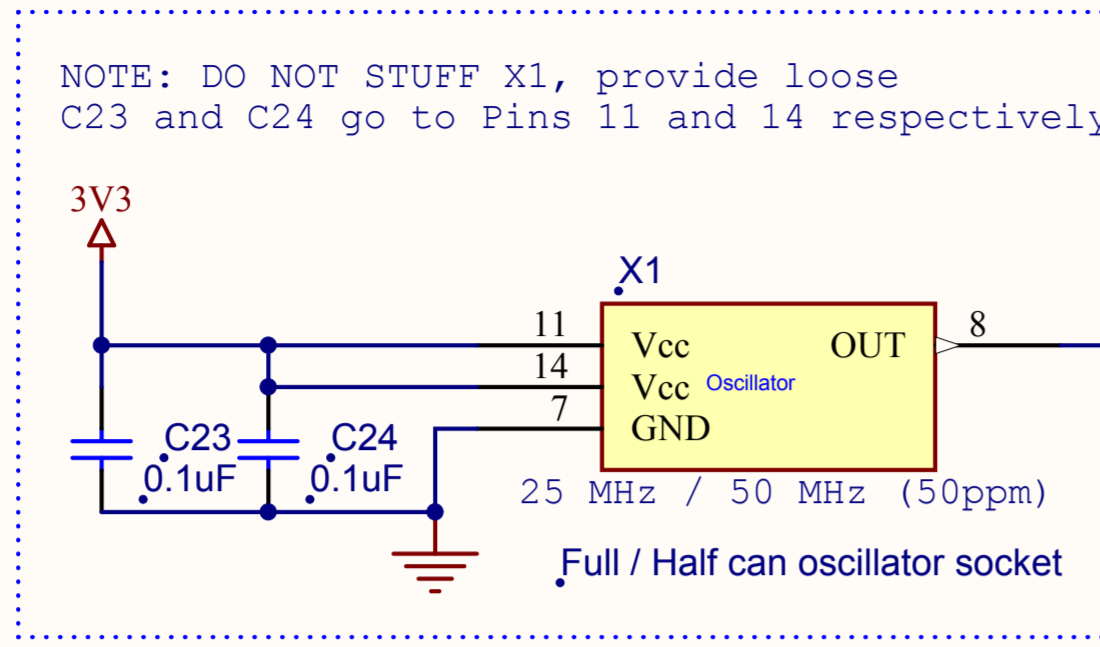
Title		
DP83640 TP&FX Demo Board - Cover		
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Resistors R1 and R18 should be placed to minimize the length of any stubs between U1 and header J1.

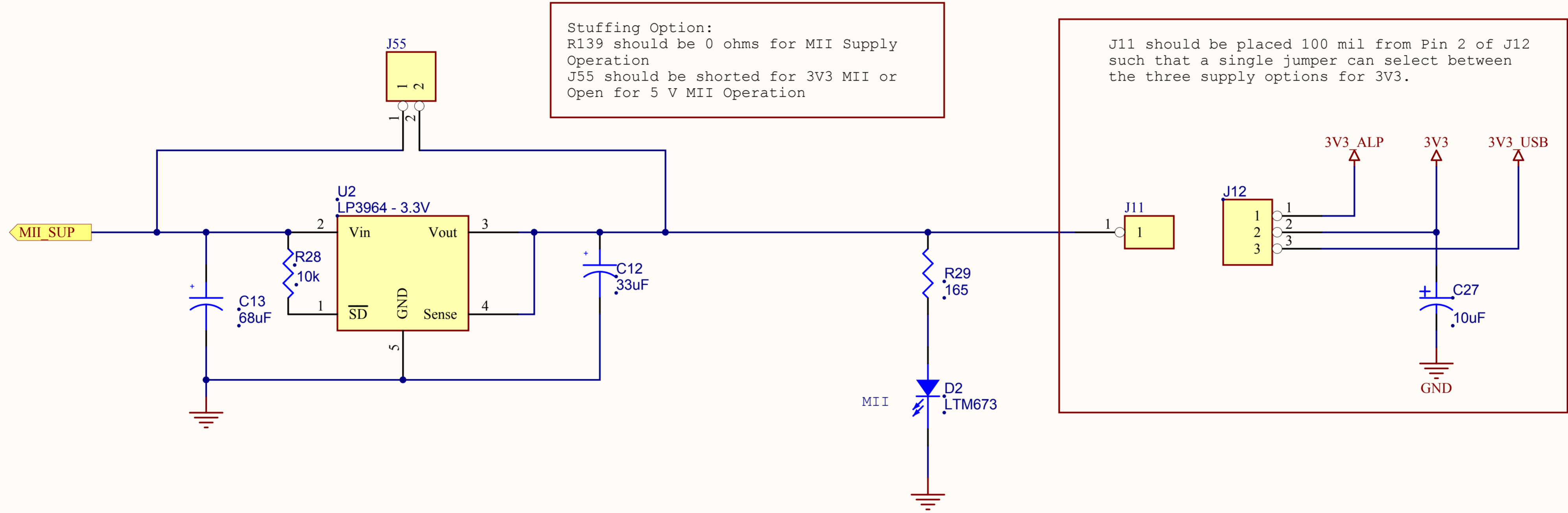
R13, R14, R163 and R164 should be placed to minimize stub lengths.

Title		
DP83640 TP&FX Demo Board - Ethernet PHY Page		
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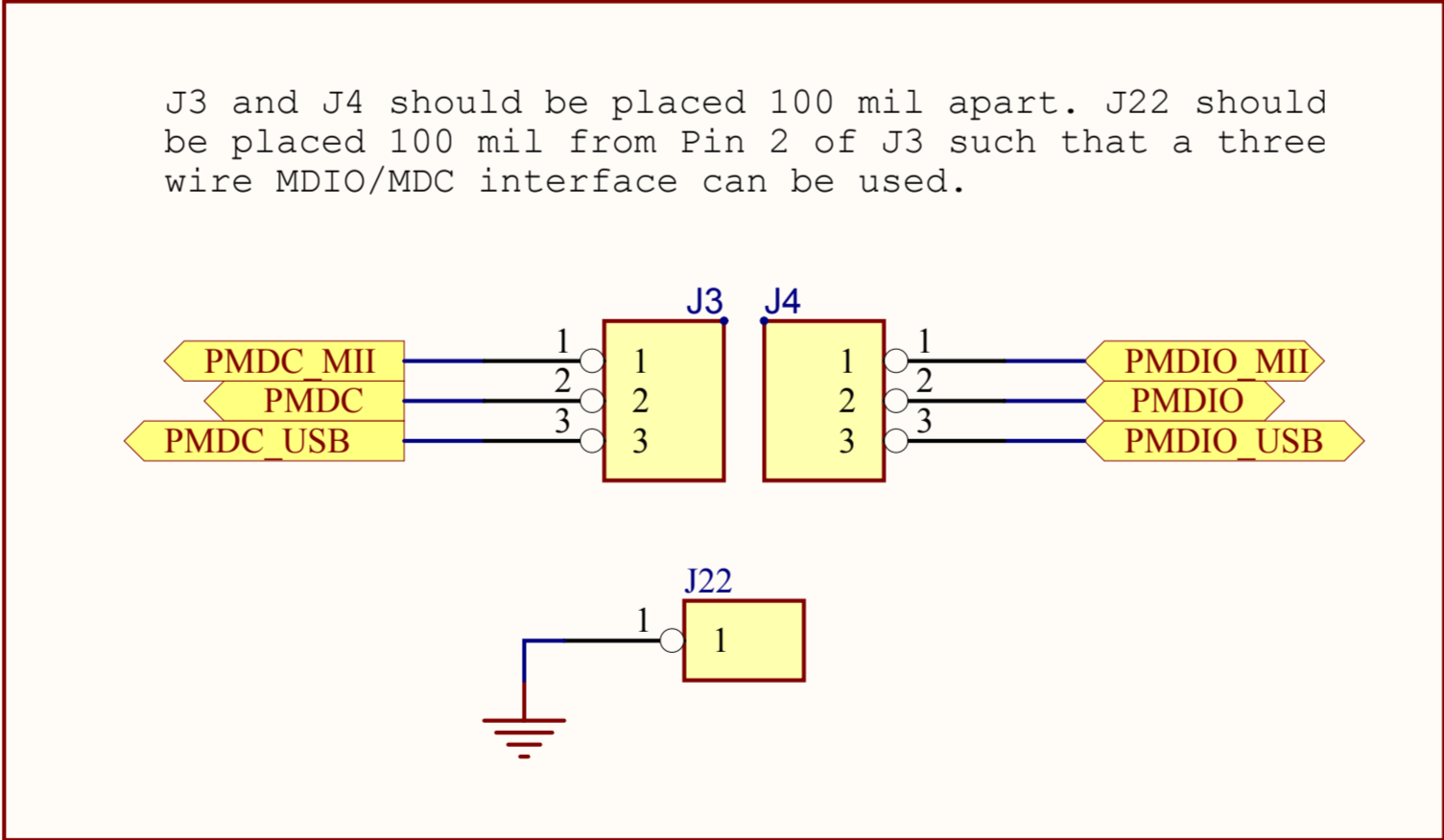
External Oscillator Stuffing Option:
R27 should be 0 ohms, R22 and R25 should
be Open for external oscillator

Crystal Stuffing Option:
Y1: Surface mount 5 x 7 package
Y2: Through-hole HC49-US package

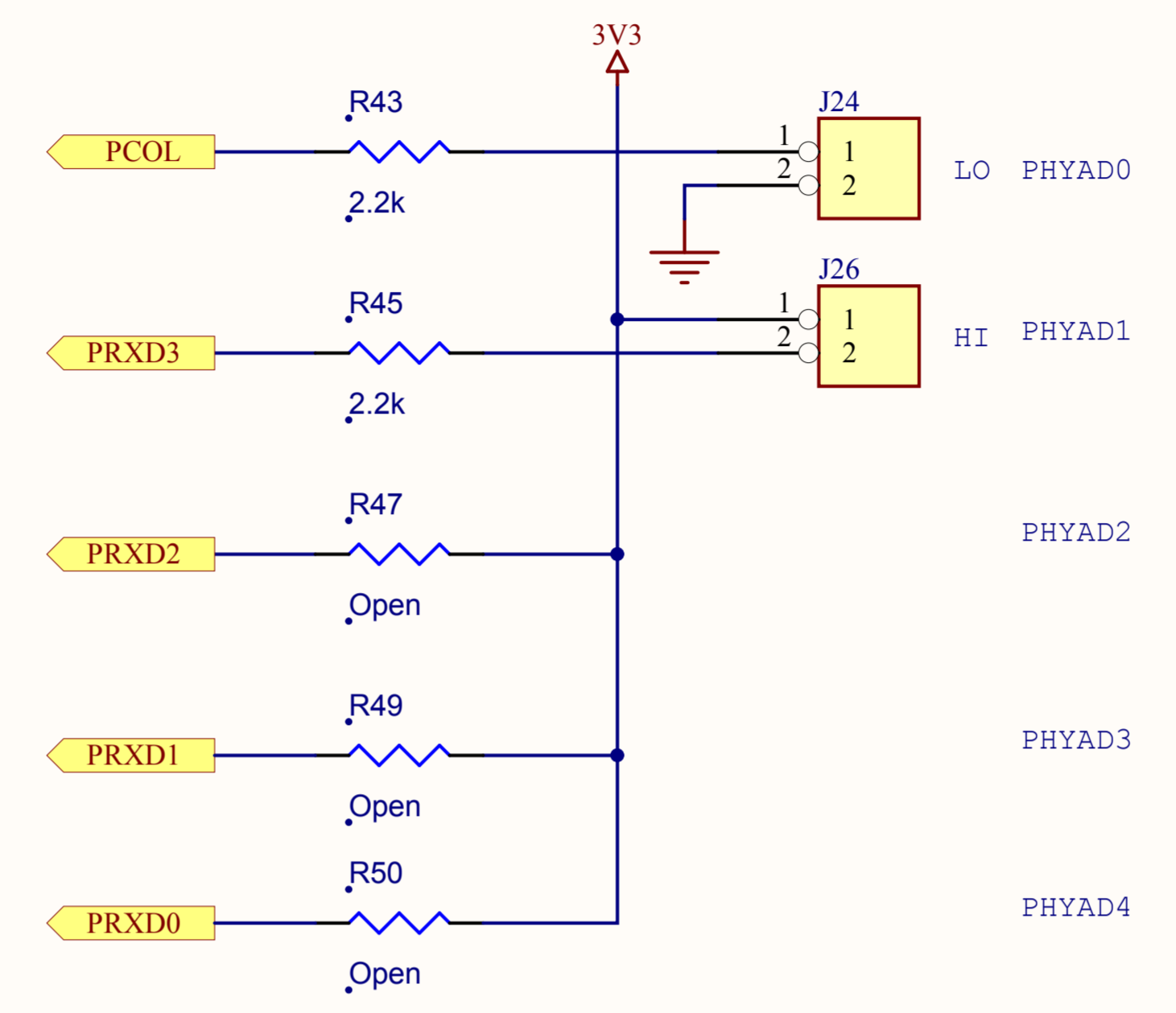
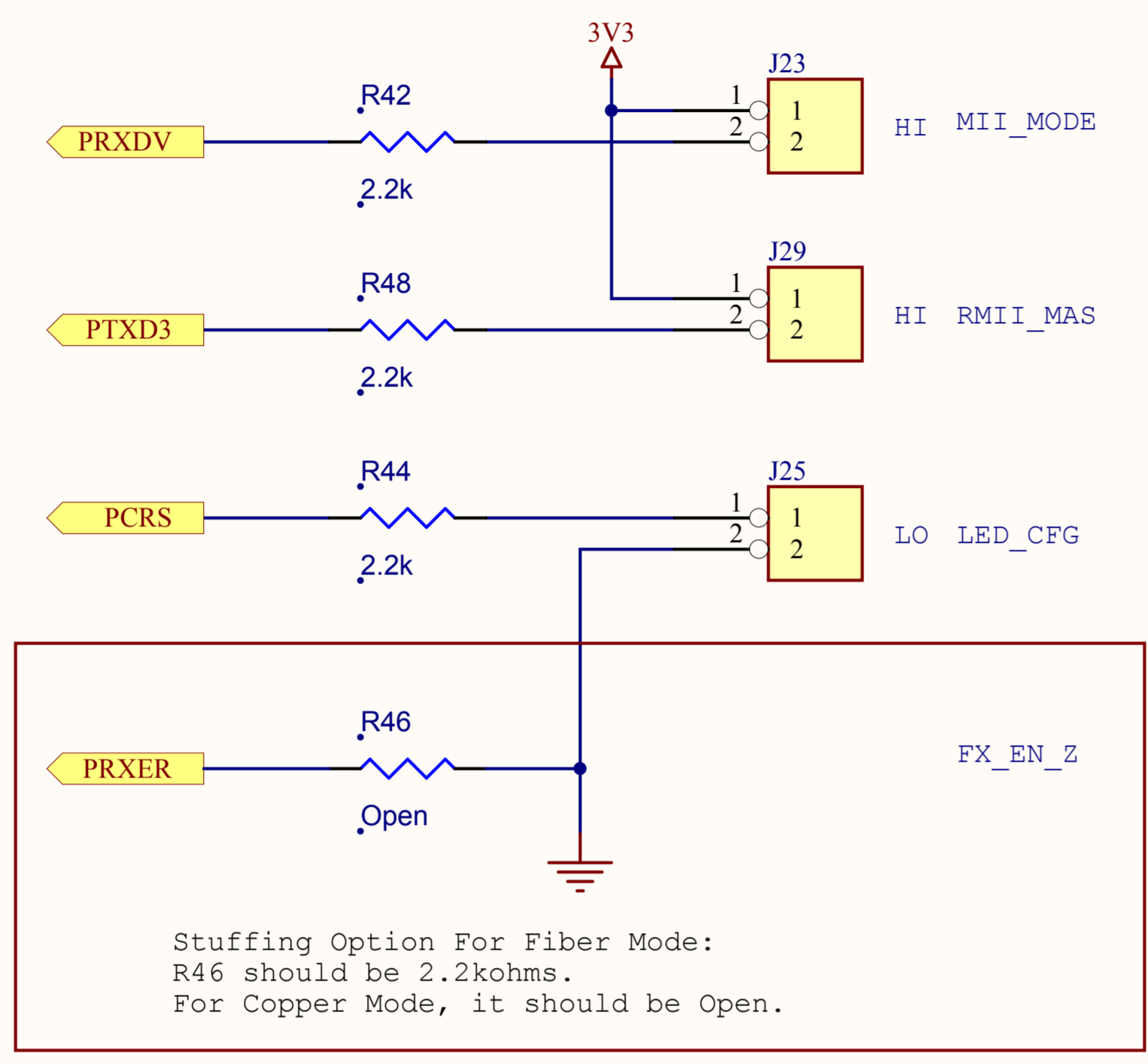


Stuffing Option:
R139 should be 0 ohms for MII Supply
Operation
J55 should be shorted for 3V3 MII or
Open for 5 V MII Operation

J11 should be placed 100 mil from Pin 2 of J12
such that a single jumper can select between
the three supply options for 3V3.



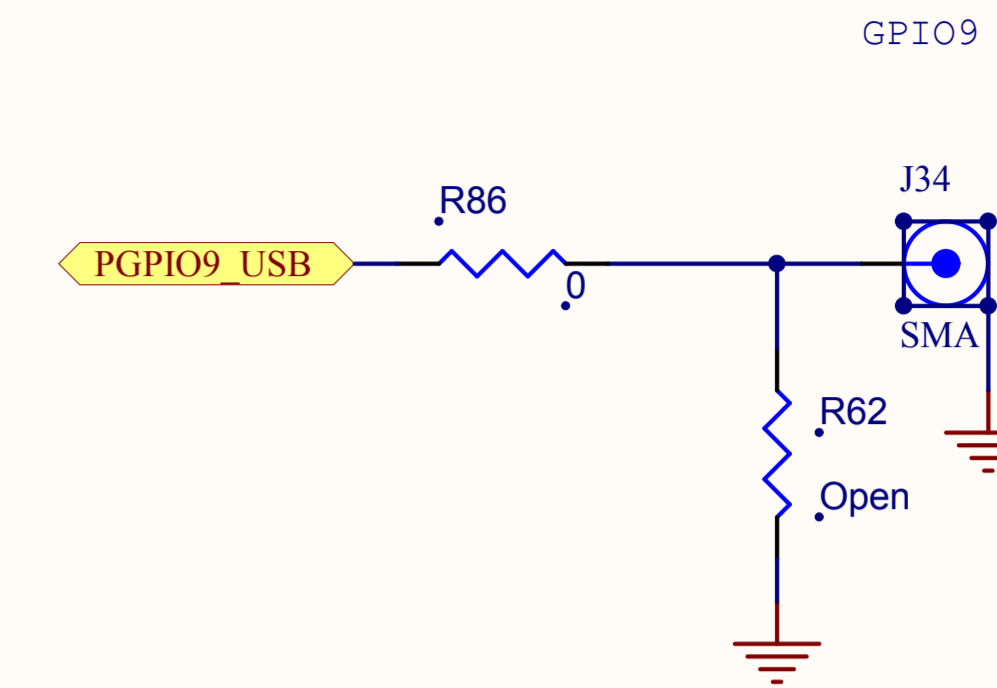
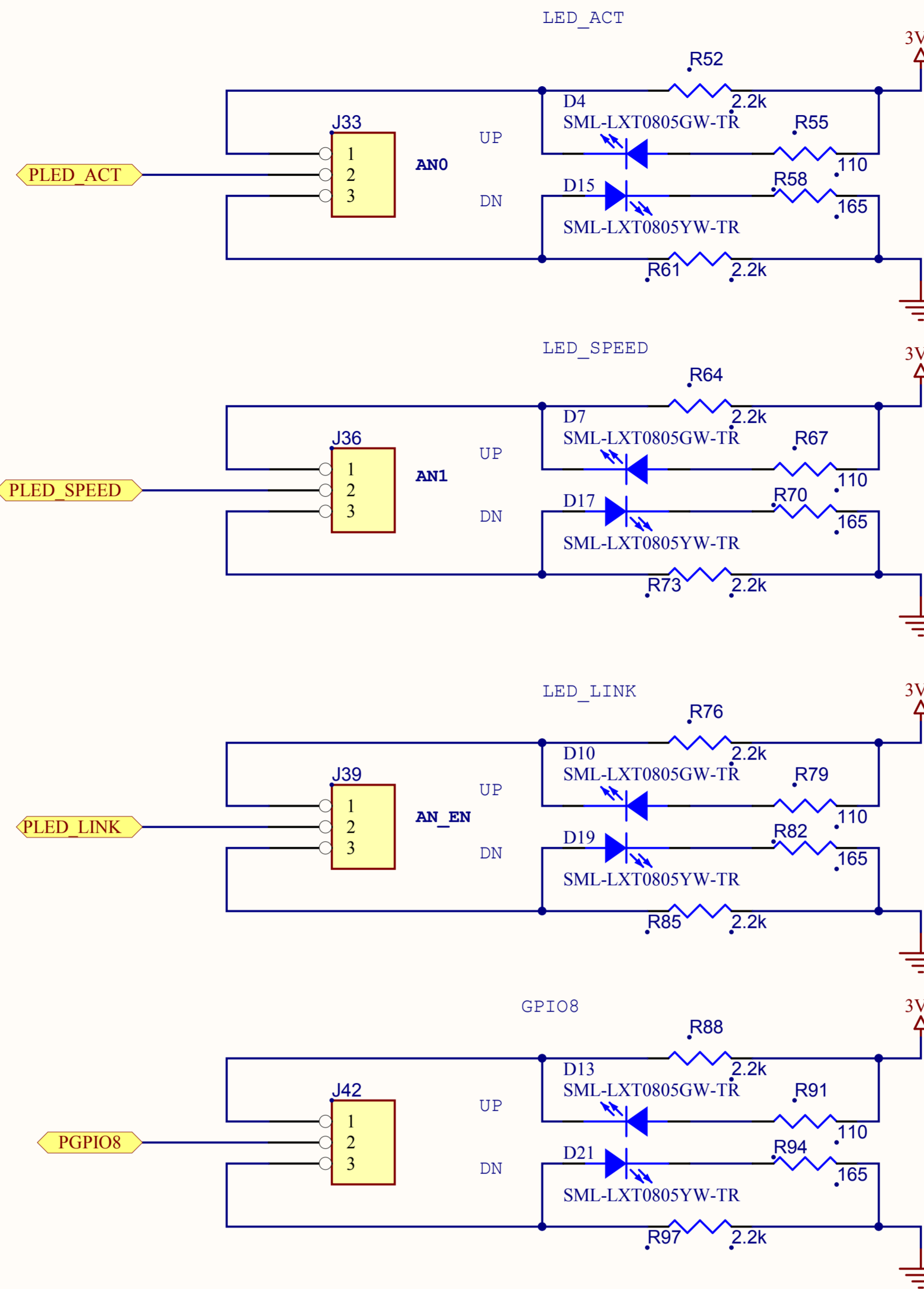
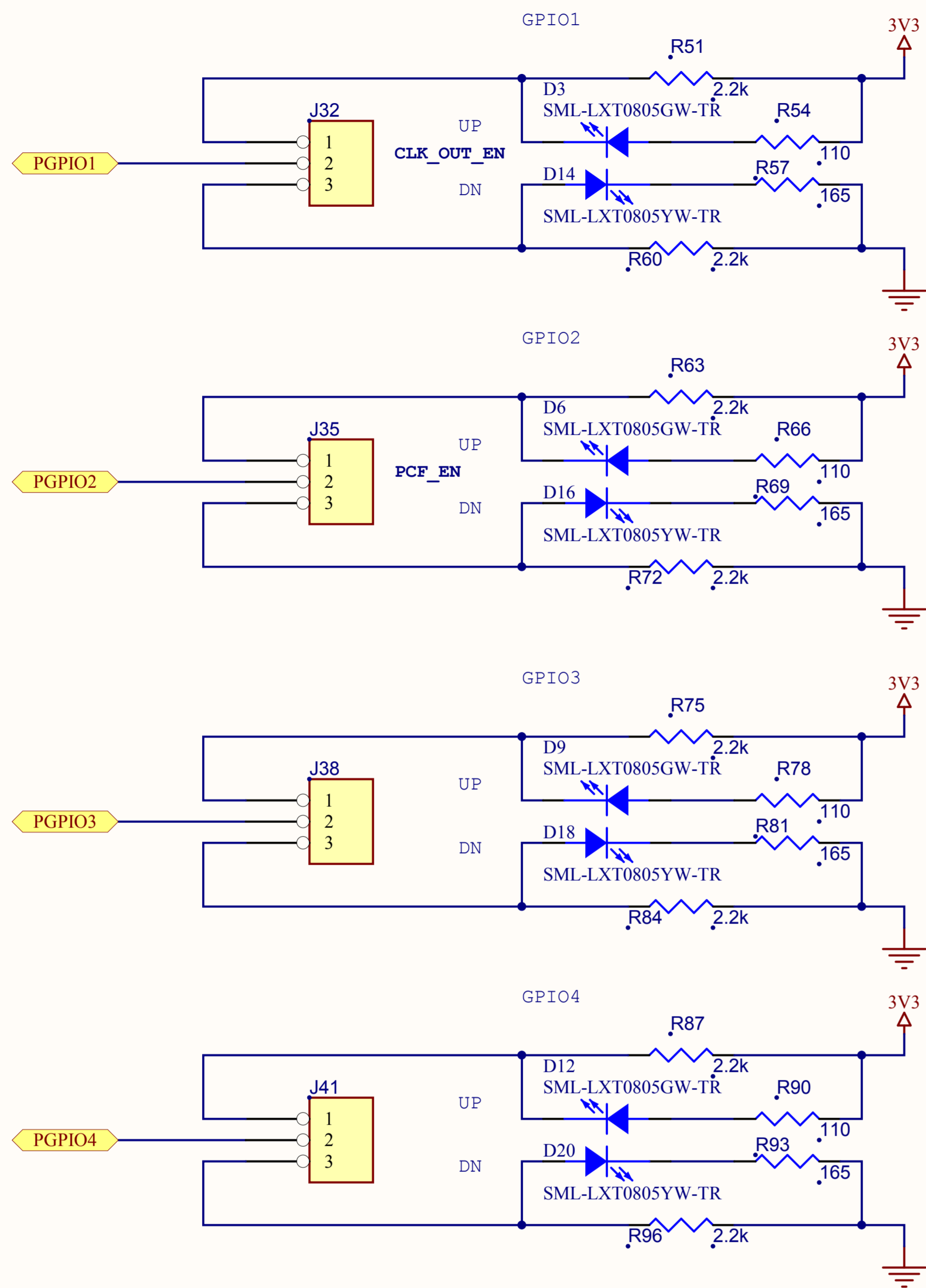
Title DP83640 TP&FX Demo Board - Power, Clock, MDIO Page		
Size A	Document Number 870013211-200	Rev 2.0
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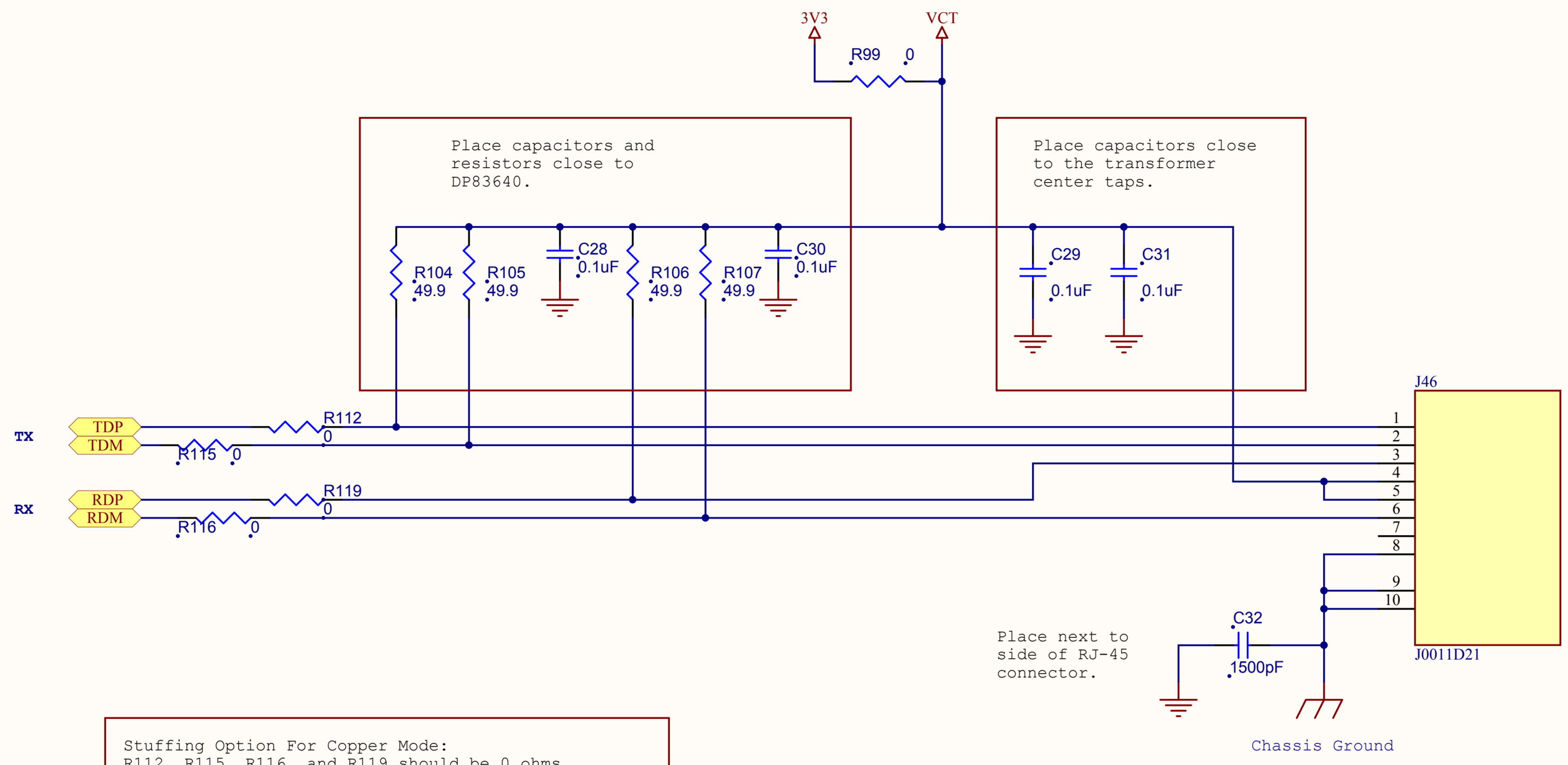
Phy Address Straps:

PHYAD1	PHYAD0	ADDRESS
0	0	0
0	1	1 (Default)
1	0	2
1	1	3

PHYAD2, PHYAD3 and PHYAD4 are internally strapped to 0.
R47, R49 and R50 can be stuffed with 2.2kohm to allow selection of Phy addresses above 3.



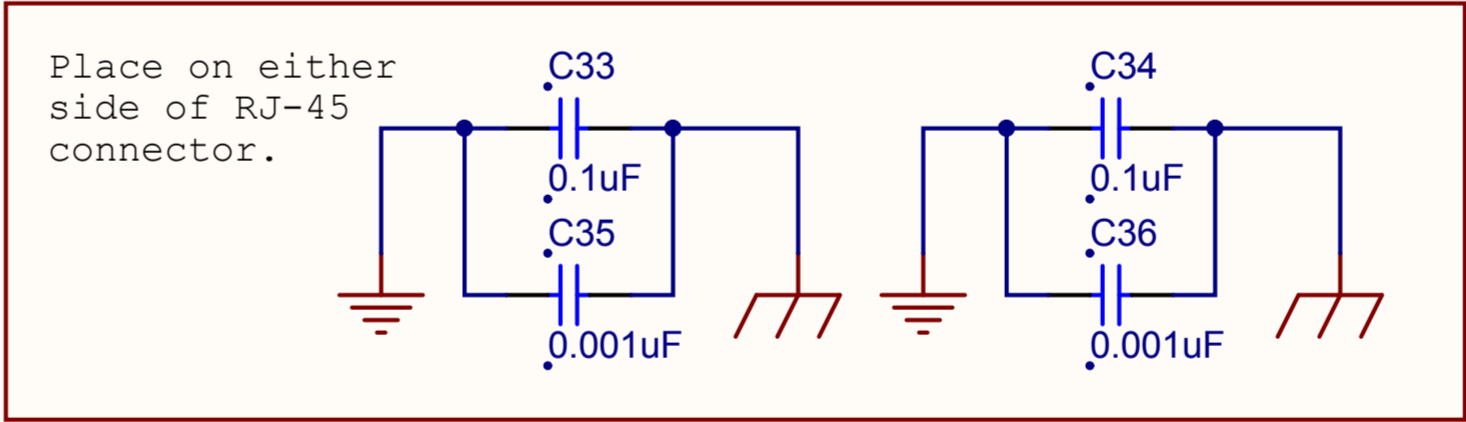
Title		
DP83640 TP&FX Demo Board - GPIO Page		
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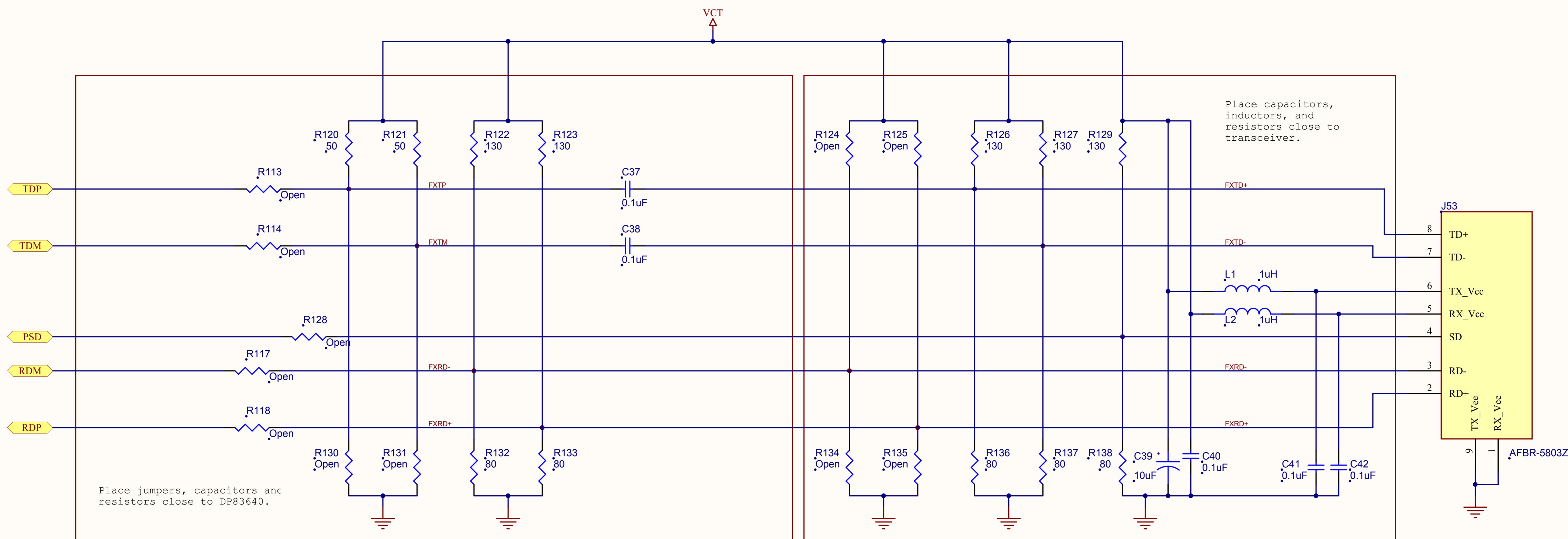
Place capacitors and resistors close to DP83640.

Place capacitors close to the transformer center taps.

Stuffing Option For Copper Mode:
R112, R115, R116, and R119 should be 0 ohms
For Fiber Mode, they should be Open.



Title		
DP83640 TP&FX Demo Board - TP Page		
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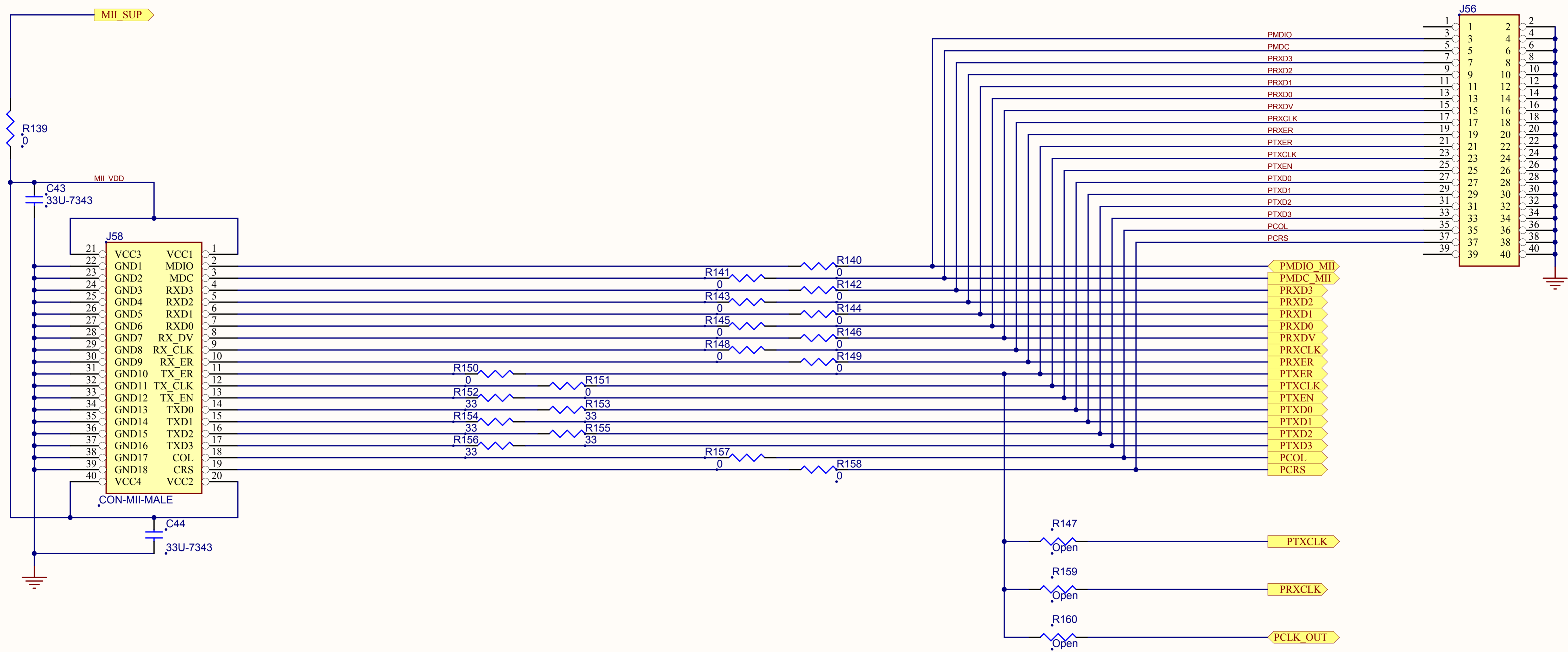


Place jumpers, capacitors and resistors close to DP83640.

Place capacitors, inductors, and resistors close to transceiver.

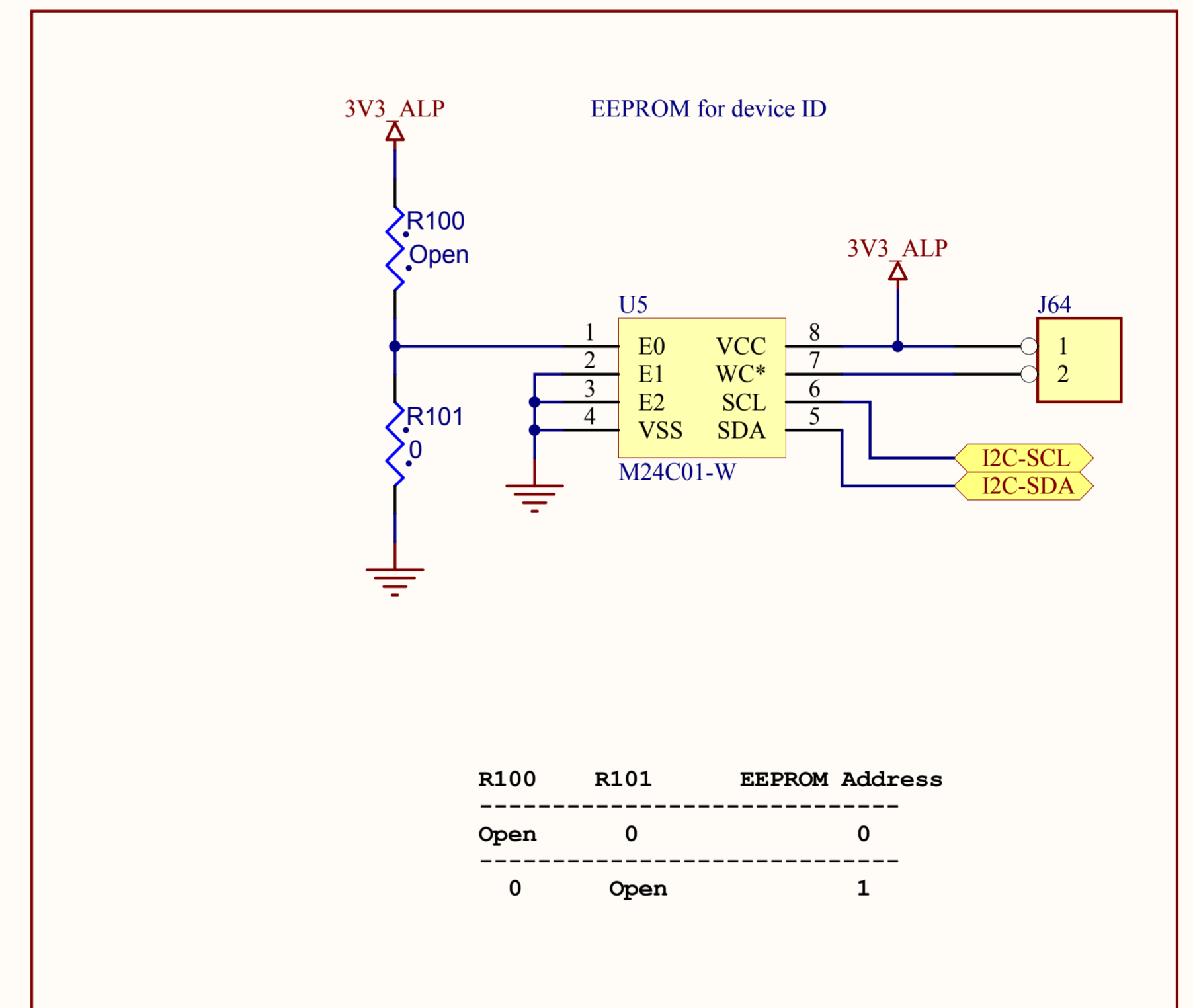
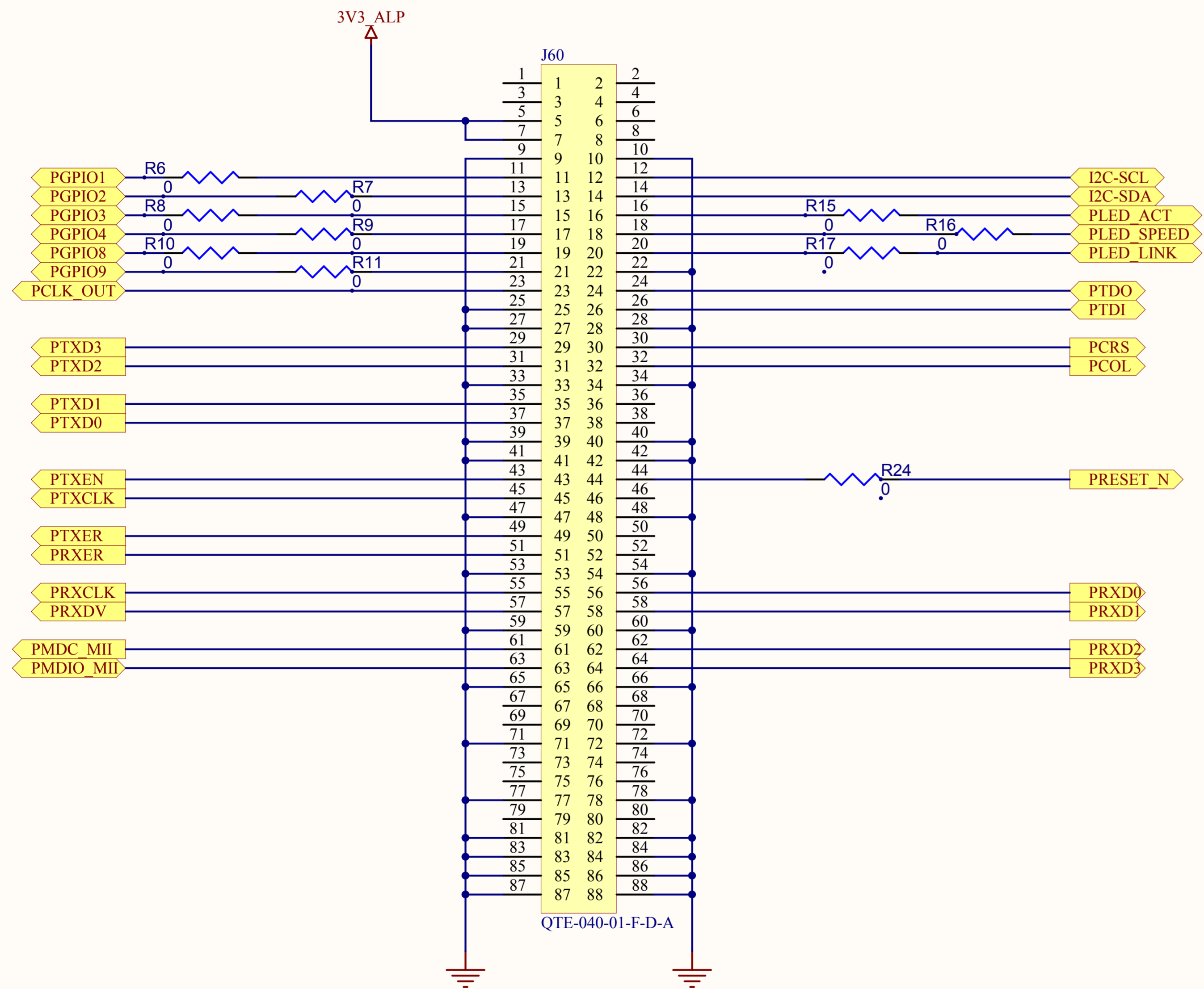
Important note:
 - R112, R115, R116, R119 are to be routed on top.
 - R113, R114, R117, R118 are to be routed on bottom.
 Stuffing option:
 For Copper Stuff: R112, R115, R116, R119
 For Fiber Stuff: R113, R114, R117, R118, R128

Title		
DP83640 TP&FX Demo Board - FX Page		
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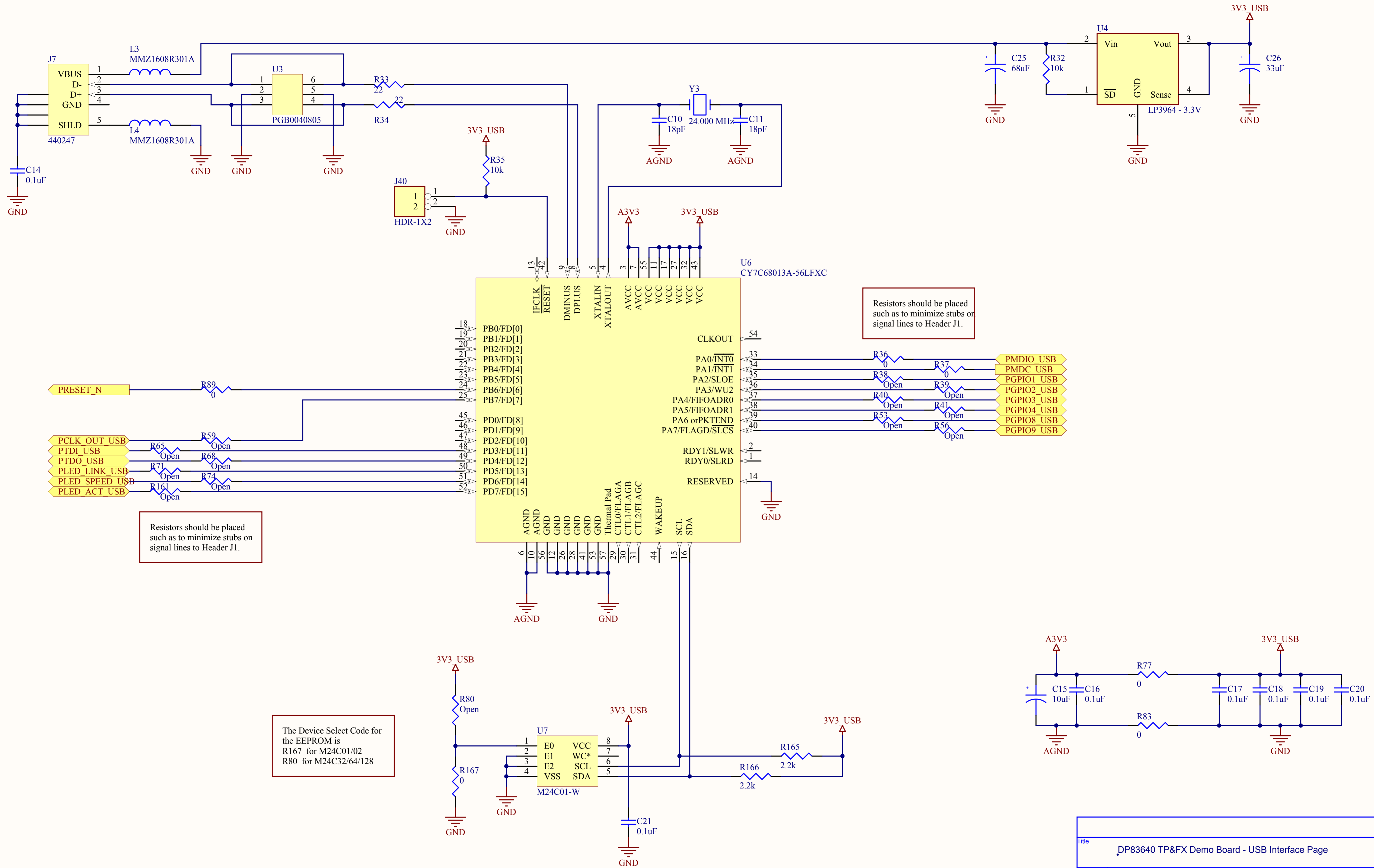


Resistor R147, R159 and R160 should be placed close to each other.

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DP83640 TP&FX Demo Board - MII Page		
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Title		
DP83640 TP&FX Demo Board - ALP Interface Page		
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Resistors should be placed such as to minimize stubs on signal lines to Header J1.

Resistors should be placed such as to minimize stubs on signal lines to Header J1.

The Device Select Code for the EEPROM is
 R167 for M24C01/02
 R80 for M24C32/64/128

Title		
DP83640 TP&FX Demo Board - USB Interface Page		
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