User's Guide

DS160PR810EVM-RSC Evaluation Module (EVM)

ABSTRACT

The DS160PR810EVM-RSC evaluation modules provides a complete high-bandwidth platform for evaluating the signal conditioning features of the Texas Instruments DS160PR810 Octal-Channel PCI-Express 4.0 Linear Redriver. This evaluation board can be used for standard compliance testing, performance evaluation, and initial system prototyping.

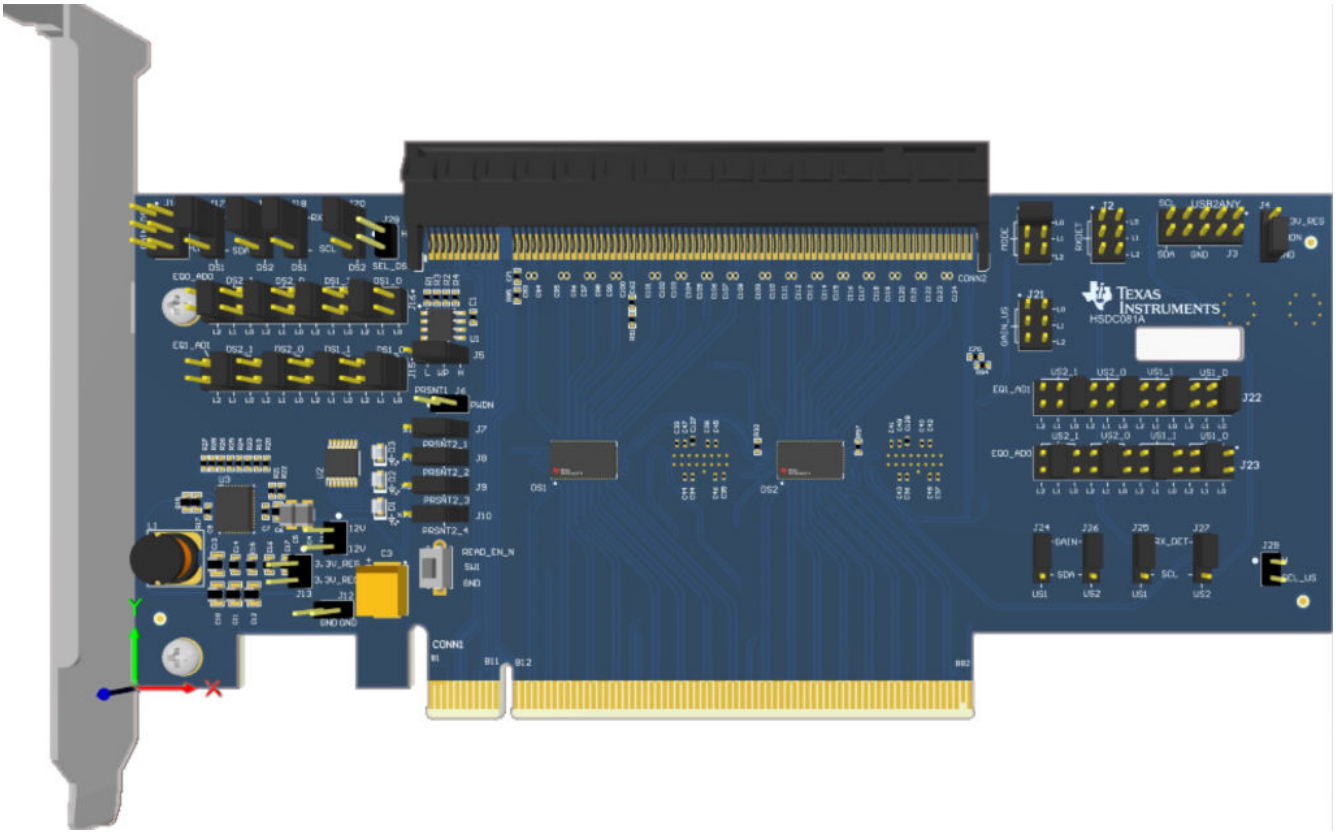

Figure 1-1. DS160PR810EVM-RSC - Top Side View

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1 Introduction

The DS160PR810EVM-RSC evaluation module features four DS160PR810 linear redrivers that can extend the transmission distance of a PCIe Gen-4 x16 bus. It can directly be plugged into a PCIe slot on a server or PC motherboard using one end of the board, and paired up with a PCIe add-in card using the straddle mount connector attached to the other end of the board.

1.1 Features

- PCIe x16 Riser Card option with four 8-channel unidirectional linear redrivers operating at rates up to 25 Gbps
- Linear equalization for seamless support of link training and PCIe channel extension
- CTLE boosts up to 18 dB at 8 GHz
- Programmable device configuration through GPIO or I2C, SMBus
- Onboard 12-V to 3.3-V, 2-A step-down DC/DC converter
- Industrial temperature range: –40°C to 85°C
- Flow-through layout in 5.5 mm × 10 mm, 64-pin, leadless WQFN 0.4-mm pitch package

1.2 Applications

- PCI Express Gen-1, 2, 3, and 4
- High-speed interfaces up to 25 Gbps
- Enterprise server motherboard, workstation
- Enterprise storage
- Enterprise add-in card, end-point

2 Description

2.1 DS160PR810 4-Level I/O Control Inputs

Each DS160PR810 features 4-level input pins (MODE, GAIN0, GAIN1, RX_DET, EQ0_0/ADDR0, EQ1_0/ADDR1, EQ0_1, and EQ1_1) that are used to control the configuration of the device. These 4-level inputs use a resistor divider to help set the four valid levels to provide a wider range of control settings.

Table 2-1. Four-Level Control Pin Settings

PIN LEVEL	PIN SETTING
L0	1 kΩ to GND
L1	13 kΩ to GND
L2	59 kΩ to GND
L3	Float

2.2 DS160PR810 Modes of Operation

Each DS160PR810 can be configured to operate in either Pin Mode, SMBus with I2C Slave Mode, or SMBus with I2C Master Mode. The mode of operation of the DS160PR810 is determined by the pin strap setting on the MODE pin as shown in Table 2-2.

Table 2-2. Modes of Operation

MODE PIN LEVEL	MODE OF OPERATION
L0	Pin Mode
L1	SMBus Mode or I2C Master Mode
L2	SMBus Mode or I2C Slave Mode
L3	RESERVED

2.3 DS160PR810 SMBus or I2C Register Control Interface

The DS160PR810 internal registers can be accessed through standard SMBus protocol. The DS160PR810 features two banks of channels, Bank 0 (Channels 0–3) and Bank 1 (Channels 4–7), each featuring a separate register set and requiring a unique SMBus slave address. The SMBus slave address pairs (one for each channel bank) are determined at power up based on the configuration of the EQ0_0/ADDR1 and EQ1_0/ADDR0 pins. The pin state is read on power up, after the internal power-on reset signal is deasserted.

There are 16 unique SMBus slave address pairs (one address for each channel bank) that can be assigned to the device by placing external resistor straps on the EQ0_0/ADDR1 and EQ1_0/ADDR0 pins as shown in Table 2-3. When multiple DS160PR810 devices are on the same SMBus interface bus, each channel bank of each device must be configured with a unique SMBus slave address pair.

Table 2-3. DS160PR810 SMBus Address Map

ADDR1 Pin Level	ADDR0 Pin Level	Bank 0: Channels 0-3: 7-Bit Address [HEX]	Bank 1 Channels 4-7: 7-Bit Address [HEX]
L0	L0	0x18	0x19
L0	L1	0x1A	0x1B
L0	L2	0x1C	0x1D
L0	L3	0x1E	0x1F
L1	L0	0x20	0x21
L1	L1	0x22	0x23
L1	L2	0x24	0x25
L1	L3	0x26	0x27
L2	L0	0x28	0x29
L2	L1	0x2A	0x2B
L2	L2	0x2C	0x2D
L2	L3	0x2E	0x2F
L3	L0	0x30	0x31
L3	L1	0x32	0x33
L3	L2	0x34	0x35
L3	L3	0x36	0x37

2.4 DS160PR810 Equalization Control

Each channel of the DS160PR810 features a continuous-time linear equalizer (CTLE) that applies high-frequency boost and low-frequency attenuation to help equalize the frequency-dependent insertion loss effects of the passive channel. Table 2-4 shows available equalization boost through EQ control pins (EQ1_0 and EQ0_0 for channels 0–3 and EQ1_1 and EQ0_1 for channels 4–7) when in Pin Control mode (MODE = L0).

Table 2-4. Equalization Control Settings

EQ INDEX	EQ1 PIN LEVEL	EQ0 PIN LEVEL	CTLE BOOST AT 4 GHz (dB)	CTLE BOOST AT 8 GHz (dB)
0	L0	L0	–0.25	–0.5
1	L0	L1	2.0	4.0
2	L0	L2	2.5	5.0
3	L0	L3	3.0	6.0
4	L1	L0	4.0	7.0
5	L1	L1	4.5	7.5
6	L1	L2	5.0	8.0
7	L1	L3	6.0	9.5
8	L2	L0	7.0	10
9	L2	L1	8.0	11
10	L2	L2	8.5	12.5
11	L2	L3	9.0	13
12	L3	L0	9.5	14.5
13	L3	L1	10.0	15
14	L3	L2	10.5	16.0
15	L3	L3	12	18

The equalization gain of each channel of each device can also be set by writing to SMBus, I2C registers in I2C Mode. Refer to the *DS160PR810 Programming Guide* (SNLU268) for details.

2.5 DS160PR810 RX Detect State Machine

Each DS160PR810 deploys an RX Detect state machine that governs the RX detection cycle as defined in the PCI Express specification. At power up or after a manually triggered event, the redriver determines whether or not a valid PCI Express termination is present at the far end of the link. The RX_DET pin of DS160PR810 provides additional flexibility to system designers to appropriately set the device in their desired mode, according to Table 2-5.

Table 2-5. Four-Level Control Pin Settings

PD PIN LEVEL	RX_DET/SCL PIN LEVEL	DESCRIPTION
L	L0	PCI Express RX detection state machine is disabled. Recommended for non-PCI Express use cases. Inputs are always 50 Ω.
L	L1	PCI Express RX detection state machine is enabled. Recommended for PCI Express use cases. Pre Detect: Hi-Z, Post Detect: 50 Ω. Outputs poll every approximate 150 µs until 3 consecutive valid RX termination detections.
L	L2	PCI Express RX detection state machine is enabled. Recommended for PCI Express use cases. Pre Detect: Hi-Z, Post Detect: 50 Ω. Outputs poll every approximate 150 µs until 2 consecutive valid RX termination detections.
L	L3 (Float)	PCI Express RX detection state machine is enabled. Recommended for PCI Express use cases. Pre Detect: Hi-Z, Post Detect: 50 Ω. Outputs poll every approximate 150 µs until a valid RX termination detection.
H	X	Manual reset, inputs are Hi-Z

2.6 DS160PR810 DC Gain Control

When operating in Pin Mode, the GAIN pins can be used to set the overall datapath DC (low frequency) gain of the DS160PR810 as shown in Table 2-6.

Table 2-6. GAIN Control

GAIN/SDA PIN LEVEL	GAIN SETTING
L0	–6 dB
L1	–3 dB
L2	3 dB
L3	0 dB (Recommended for most use cases)

The DC gain of each channel of each device can also be set by writing to SMBus, I2C registers in Slave or Master Modes. Refer to the *DS160PR810 Programming Guide* (SNLU268) for details.

2.7 DS160PR810 EVM Global Controls

Table 2-7 shows DS160PR810EVM-RSC global controls that affect all devices on the board.

Table 2-7. EVM Global Controls

COMPONENT	NAME	FUNCTION / DESCRIPTION
J1	3x2 Header	MODE control tied to MODE pins of all four DS160PR810 devices on the EVM L0: All devices set to Pin Mode (Default) L1: All devices set to SMBus, I2C Maseter Mode L2: SMBus, I2C Slave Mode L3: Reserved
J2	3x2 Header	RX DET control tied to RX DET pins of all four DS160PR810 devices on the EVM L0: RX Detect state machine disabled on all devices L1: RX Detect state machine enabled on all devices (3 valid detections needed) L2: RX Detect state machine enabled on all devices (2 valid detections needed) L3: RX Detect state machine enabled on all devices (1 valid detection needed) - Default
J3	5x2 Header	SMBus, I2C interface. All four DS160PR810 devices on the EVM are on the same bus and can be accessed through this interface.
J4	3x1 Header	PWDN control tied to PD1 and PD2 pins of all four DS160PR810 devices on the EVM PWDN tied to GND: All devices enabled (Default) PWDN tied to 3.3V_REG: All devices disabled. PWDN floating: Tie PCIe system PRSNT signal to PWDN using J6 for the PWDN control (optional for PCIe use case)
J5	3x1 Header	Access point to the WP (write protect) pin of the onboard EEPROM devices WP tied to GND: I2C Access to the EEPROM enabled WP floating: I2C Access to the EEPROM disabled (default)
J6	2x1 Header	Alternative PWDN Control PWDN floating: Use J3 for the PWDN control PWDN tied to PRSNT: PRSNT signal controls PWDN (optional for PCIe use case)
J7, J8, J9, J10	3x1 Headers	PCIe PRSNT Signal Controls Tie pins 1-2 on J7, J8, J9, and J10: Allow support any PCIe bus width (default) Tie pins 2-3 of J7, leave J8, J9, and J10 floating: Force x1 PCIe bus width Tie pins 2-3 of J8, leave J7, J9, and J10 floating: Force x4 PCIe bus width Tie pins 2-3 of J9, leave J7, J8, and J10 floating: Force x8 PCIe bus width Tie pins 2-3 of J10, leave J7, J8, and J9 floating: Force x16 PCIe bus width
J11	2x1 Header	Onboard regulator input. Apply 12 V when using the EVM as a standalone system. DO NOT APPLY power if plugging the EVM into a system as the power is provided through the gold finger connector (CONN1).
J12	2x1 Header	Access point to the GND reference
J13	2x1 Header	Onboard 3.3-V output

2.8 DS160PR810EVM Downstream Devices Control

Table 2-8 shows the DS160PR810EVM downstream device controls that affect DS1 and DS2 devices on the board.

Table 2-8. EVM Downstream Devices Controls

COMPONENT	NAME	FUNCTION / DESCRIPTION
J14	3x2 Header	Gain Controls tied to GAIN pins of all downstream device banks L0: –6 dB Gain Setting L1: –3 dB Gain Setting L2: 3 dB Gain Setting L3: 0 dB Gain Setting (default)
J15	12x2 Header	Pin Mode: EQ1 controls for each downstream device and device bank. Use pins 1–6 for configuring EQ1_0 pin of Bank 0 of DS1 device. Use pins 7–12 for configuring EQ1_1 pin of Bank 1 of DS1 device. Use pins 13–18 for configuring EQ1_0 pin of Bank 0 of DS2 device. Use pins 19–24 for configuring EQ1_1 pin of Bank 1 of DS2 device. SMBus, I2C Modes: ADDR1 controls for each downstream device. Use pins 1–6 for configuring ADDR1 pin of DS1 device. Use pins 13–18 for configuring ADDR1 pin of DS2 device. Install a shunt to achieve L0, L1, or L2 level on the pin. Leave floating to achieve L3 level on the pin.
J16	12x2 Header	Pin Mode: EQ0 controls for each downstream device and device bank. Use pins 1–6 for configuring EQ0_0 pin of Bank 0 of DS1 device. Use pins 7–12 for configuring EQ0_1 pin of Bank 1 of DS1 device. Use pins 13–18 for configuring EQ0_0 pin of Bank 0 of DS2 device. Use pins 19–24 for configuring EQ0_1 pin of Bank 1 of DS2 device. SMBus, I2C Modes: ADDR0 controls for each downstream device. Use pins 1–6 for configuring ADDR0 pin of DS1 device. Use pins 13–18 for configuring ADDR0 pin of DS2 device. Install a shunt to achieve L0, L1, or L2 level on the pin. Leave floating to achieve L3 level on the pin.
J17	3x1 Header	GAIN / SDA Dual Function Pin Provision for DS1 Device Install shunt across pins 1-2 for operation in Pin Mode (default) Install shunt across pins 2-3 for operation in SMBus, I2C Modes
J18	3x1 Header	RX DET / SCL Dual Function Pin Provision for DS1 Device Install shunt across pins 1-2 for operation in Pin Mode (default) Install shunt across pins 2-3 for operation in SMBus, I2C Modes
J19	3x1 Header	GAIN / SDA Dual Function Pin Provision for DS2 Device Install shunt across pins 1-2 for operation in Pin Mode (default) Install shunt across pins 2-3 for operation in SMBus, I2C Modes
J20	3x1 Header	RX DET / SCL Dual Function Pin Provision for DS2 Device Install shunt across pins 1-2 for operation in Pin Mode (default) Install shunt across pins 2-3 for operation in SMBus, I2C Modes

2.9 DS160PR810EVM Upstream Devices Control

Table 2-9 shows DS160PR810EVM upstream devices controls that affect US1-US2 devices on the board.

Table 2-9. EVM Upstream Devices Controls

COMPONENT	NAME	FUNCTION / DESCRIPTION
J21	3x2 Header	Gain Controls tied to GAIN pins of all upstream device banks L0: -6 dB Gain Setting L1: -3 dB Gain Setting L2: 3 dB Gain Setting L3: 0 dB Gain Setting (default)
J22	12x2	Pin Mode: EQ1 controls for each upstream device and device bank. Use pins 1–6 for configuring EQ1_0 pin of Bank 0 of US1 device. Use pins 7–12 for configuring EQ1_1 pin of Bank 1 of US1 device. Use pins 13–18 for configuring EQ1_0 pin of Bank 0 of US2 device. Use pins 19–24 for configuring EQ1_1 pin of Bank 1 of US2 device. SMBus, I2C Modes: ADDR1 controls for each upstream device. Use pins 1–6 for configuring ADDR1 pin of US1 device. Use pins 13–18 for configuring ADDR1 pin of US2 device. Install a shunt to achieve L0, L1, or L2 level on the pin. Leave floating to achieve L3 level on the pin.
J23	12x2 Header	Pin Mode: EQ0 controls for each upstream device and device bank. Use pins 1–6 for configuring EQ0_0 pin of Bank 0 of US1 device. Use pins 7–12 for configuring EQ0_1 pin of Bank 1 of US1 device. Use pins 13–18 for configuring EQ0_0 pin of Bank 0 of US2 device. Use pins 19–24 for configuring EQ0_1 pin of Bank 1 of US2 device. SMBus, I2C Modes: ADDR0 controls for each upstream device. Use pins 1–6 for configuring ADDR0 pin of US1 device. Use pins 13–18 for configuring ADDR0 pin of US2 device. Install a shunt to achieve L0, L1, or L2 level on the pin. Leave floating to achieve L3 level on the pin.
J24	3x1 Header	GAIN / SDA Dual Function Pin Provision for US1 Device Install shunt across pins 1-2 for operation in Pin Mode (default) Install shunt across pins 2-3 for operation in SMBus, I2C Modes
J25	3x1 Header	RX DET / SCL Dual Function Pin Provision for US1 Device Install shunt across pins 1-2 for operation in Pin Mode (default) Install shunt across pins 2-3 for operation in SMBus, I2C Modes
J26	3x1 Header	GAIN / SDA Dual Function Pin Provision for US2 Device Install shunt across pins 1-2 for operation in Pin Mode (default) Install shunt across pins 2-3 for operation in SMBus, I2C Modes
J27	3x1 Header	RX DET / SCL Dual Function Pin Provision for US2 Device Install shunt across pins 1-2 for operation in Pin Mode (default) Install shunt across pins 2-3 for operation in SMBus, I2C Modes

2.10 Quick-Start Guide (Pin Mode)

Check that the shunts are at the following positions as shown in Figure 1-1:

1. The redrivers are configured to operate in Pin Mode (MODE pins tied to L0 using J1 header).
2. RX_Detect state machine of all redrivers is enabled by leaving J2 open.
3. The redrivers are enabled (PWDN pins tied to GND using J4 header). Alternatevely, for PCIe applications, the PWDN pins may be driven by PCIe Present (PRSNT) signal by leaving J4 open and placing a shunt across pins 1 and 2 of J6.
4. The board is configured for any PCIe bus width (PRSNT signal controls set as shown in Figure 1-1 using J7, J8, J9 and J10 headers).
5. DC Gain of all redrivers is set to 0 dB by leaving J14 open for the downstream redrivers and by leaving J21 open for the upstream redrivers.
6. EQ level of the RX CTLEs of all redrivers is set to 8.4 dB at 8 GHz by using J15 and J16 for the downstream redrivers and J22 and J23 for the upstream redrivers.
7. If necessary, adjust EQ levels of the downstream redrivers, or upstream redrivers, or both, by arranging shunts on J15 and J16 for downstream redrivers and J22 and J23 for the upstream redrivers.
8. Plug the EVM into a PCIe x16 server motherboard slot. Ensure the motherboard is powered down before installing the EVM or configured for hot-plug operation.
9. Install a compatible PCIe endpoint card into the straddle connector of the EVM.
10. Power-up the motherboard.

2.11 Quick-Start Guide (SMBus Slave Mode)

1. Configure all devices to operate in the SMBus Slave Mode by setting their MODE pins to the L2 level. This is accomplished by placing a shunt on J1 L2 location.
2. Set a unique SMBus Slave address for each device by placing shunts in the following arrangement:
   - On J15 connector, place shunts in L0 locations for all downstream devices (DS1_0 and DS2_0; DS1_1 and DS2_1 are a Don't Care).
   - On J16 connector, place shunts in L0 locations for the DS1_0 and in L1 locations for DS2_0 (DS1_1 and DS2_1 are a Don't Care).
   - On J22 connector, place shunts in L0 locations for all upstream devices (US1_0 and US2_0; DS1_1 and DS2_1 are a Don't Care).
   - On J23 connector, place a shunt in L2 location for the US1_0 and remove shunts for US2_0 to achieve L3 level (US1_1 and US2_1 are a Don't Care).
3. Move shunts from pins 1-2 to pins 2-3 on J17, J18, J19, J20, J24, J25, J26, and J27 to connect the dual function redriver pins to the SMBus, I2C bus.
4. Enable all devices by pulling their PWDN pins to GND. This is accomplished by placing a shunt on J4 between PWDN and GND.
5. Connect the USB2ANY Adapter to J3 (Note that the USB2ANY Adapter is not supplied with the DS160PR810EVM-RSC).
6. Install SigCon Architect Version 3.0.0.14 application and the DS160PR810 profile.
7. Plug the EVM into a PCIe x16 server motherboard slot. Ensure the motherboard is powered down before installing the EVM or configured for hot-plug operation.
8. Install a compatible PCIe endpoint card into the straddle connector of the EVM.
9. Power-up the motherboard.
10. Start the SigCon Architect application.
11. Select the DS160PR810 Configuration Page and click on "Apply" box to enable the device profile. If necessary, edit devices addresses in the Edit Device Addresses box.
12. In the DS160PR810 High Level Page, select Block Diagram as shown in Figure 2-1.
13. Select the desired EQ Settings and Driver VOD.
14. Select devices to which you want to apply the selected settings and click "Apply to All Channels".

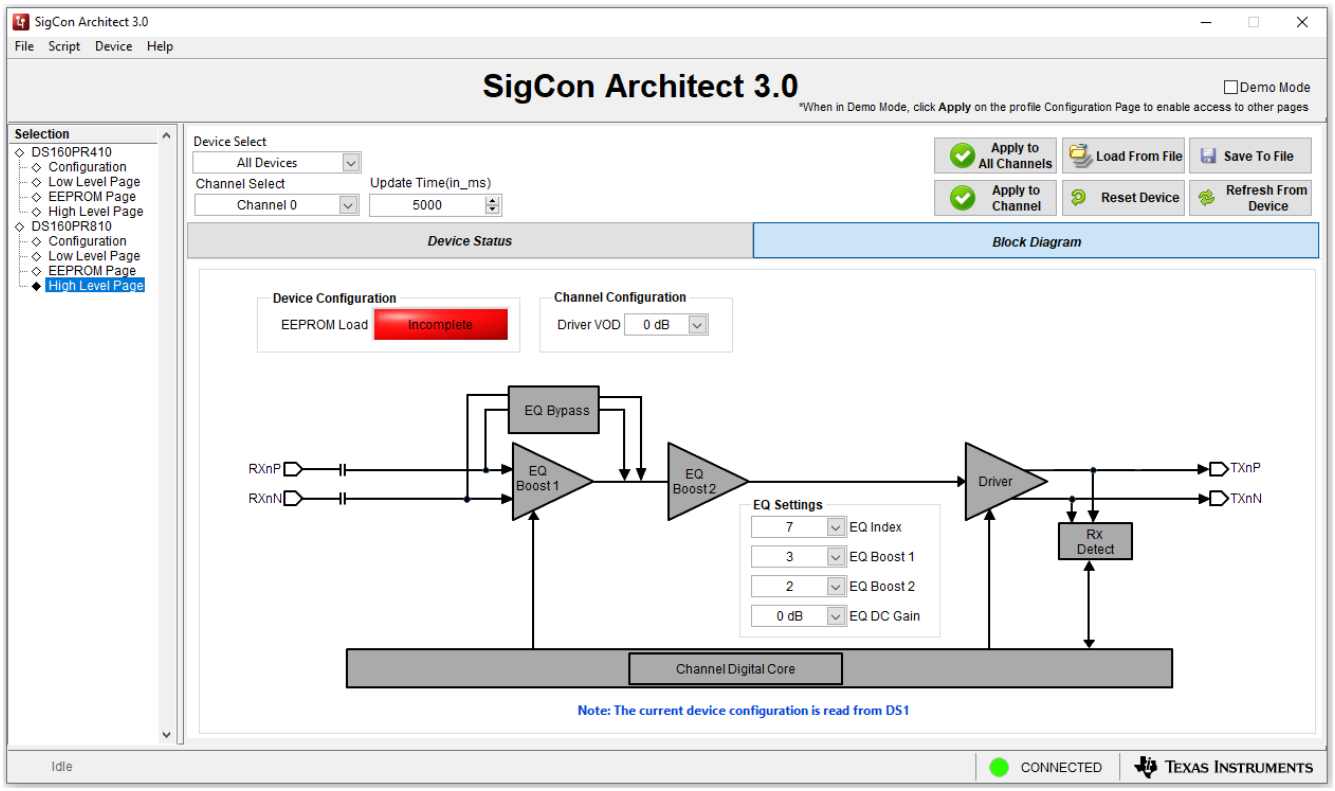


Figure 2-1. SigCon Architect DS160PR810 High Level Page

3 Test Setup and Results

Figure 3-1 shows a typical system setup with the DS160PR810EVM-RSC placed between a CPU on a server motherboard and an PCIe end point (Network Interface Card or NIC). Additional "Extender" cards are inserted to increase the channel loss and demonstrate the ability of the redriver to extend the reach.

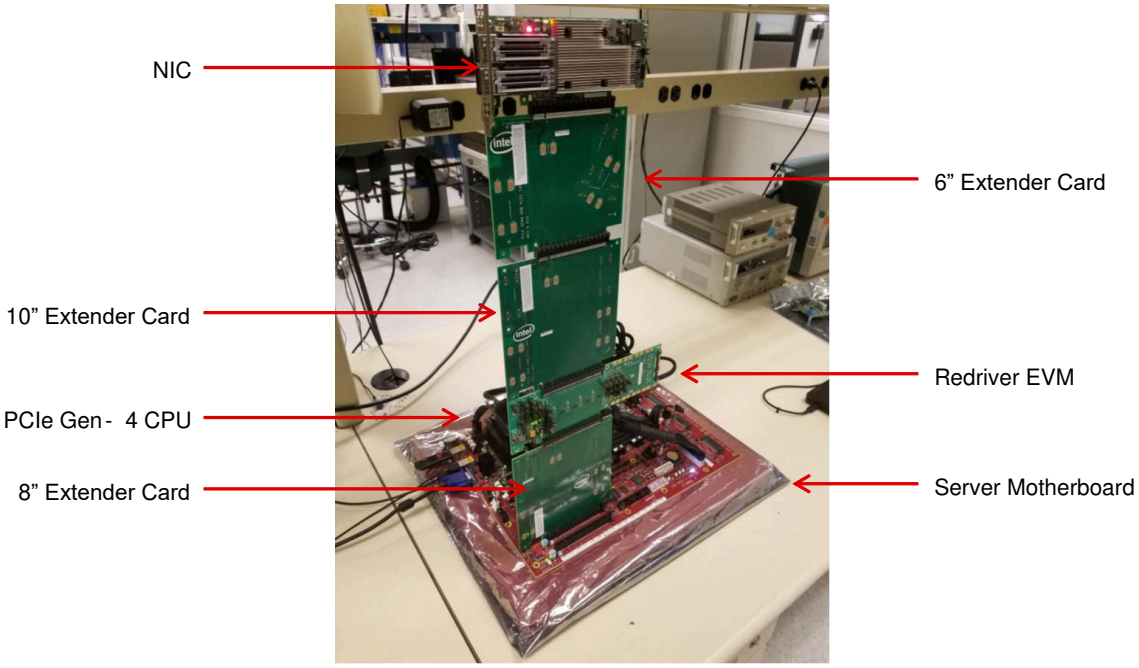


Figure 3-1. Example Test Setup

Figure 3-2 is a typical test result achieved with a system shown in Figure 3-1. As the result indicates, the end point (Mellanox NIC) with the DS160PR810EVM-RSC placed in the datapath achieves a stable Gen4, x16 PCIe link.

```
Address Decoding Per Root Port...
DMI uses subtractive decode.

**********************************************************************
*                                                                    *
*   Socket 1 (R0) PCIe Port Mappings                                 *
*   Segment #0, Buses 0x00,0x80,0x94,0xae,0xc8,0xe2,0xfe,0xff        *
*                                                                    *
**********************************************************************

=============================================================================================================
| PCIe port |          0a          | 0b | 0c | 0d | 1a  | 1b | 1c | 1d | 2a  | 2b | 2c | 2d | 3a | 3b | 3c | 3d |
-------------------------------------------------------------------------------------------------------------
| config as |          x16         |    |    |    | x16 |    |    |    | x16 |    |    |    | x4 | x4 | x4 | x4 |
-------------------------------------------------------------------------------------------------------------
|   width   |          x16         |    |    |    |     |    |    |    |     |    |    |    |    |    |    |    |
-------------------------------------------------------------------------------------------------------------
|   speed   |         Gen4         |    |    |    |     |    |    |    |     |    |    |    |    |    |    |    |
-------------------------------------------------------------------------------------------------------------
| slot/down |         slot         |    |    |    |     |    |    |    |     |    |    |    |    |    |    |    |
-------------------------------------------------------------------------------------------------------------
|  ASPM en  |          L1          |    |    |    |     |    |    |    |     |    |    |    |    |    |    |    |
-------------------------------------------------------------------------------------------------------------
| secbusno  |         95h          |    |    |    |     |    |    |    |     |    |    |    |    |    |    |    |
-------------------------------------------------------------------------------------------------------------
| subbusno  |         95h          |    |    |    |     |    |    |    |     |    |    |    |    |    |    |    |
-------------------------------------------------------------------------------------------------------------
| linkstate |       Up.L0          |    |    |    |     |    |    |    |     |    |    |    |    |    |    |    |
-------------------------------------------------------------------------------------------------------------
| VendorID  | Mellanox Technologies |    |    |    |     |    |    |    |     |    |    |    |    |    |    |    |
-------------------------------------------------------------------------------------------------------------
| DeviceID  |        1019h         |    |    |    |     |    |    |    |     |    |    |    |    |    |    |    |
-------------------------------------------------------------------------------------------------------------
|   RevID   |         00h          |    |    |    |     |    |    |    |     |    |    |    |    |    |    |    |
-------------------------------------------------------------------------------------------------------------
|  ASPM en  |          no          |    |    |    |     |    |    |    |     |    |    |    |    |    |    |    |
=============================================================================================================


Address Decoding Per Root Port...
Port 0a MBAS=          C8000000h MLIM=          C80FFFFFh
```

Figure 3-2. Example Test Results

4 Schematics

Figure 4-1 through Figure 4-8 illustrate the EVM schematics.

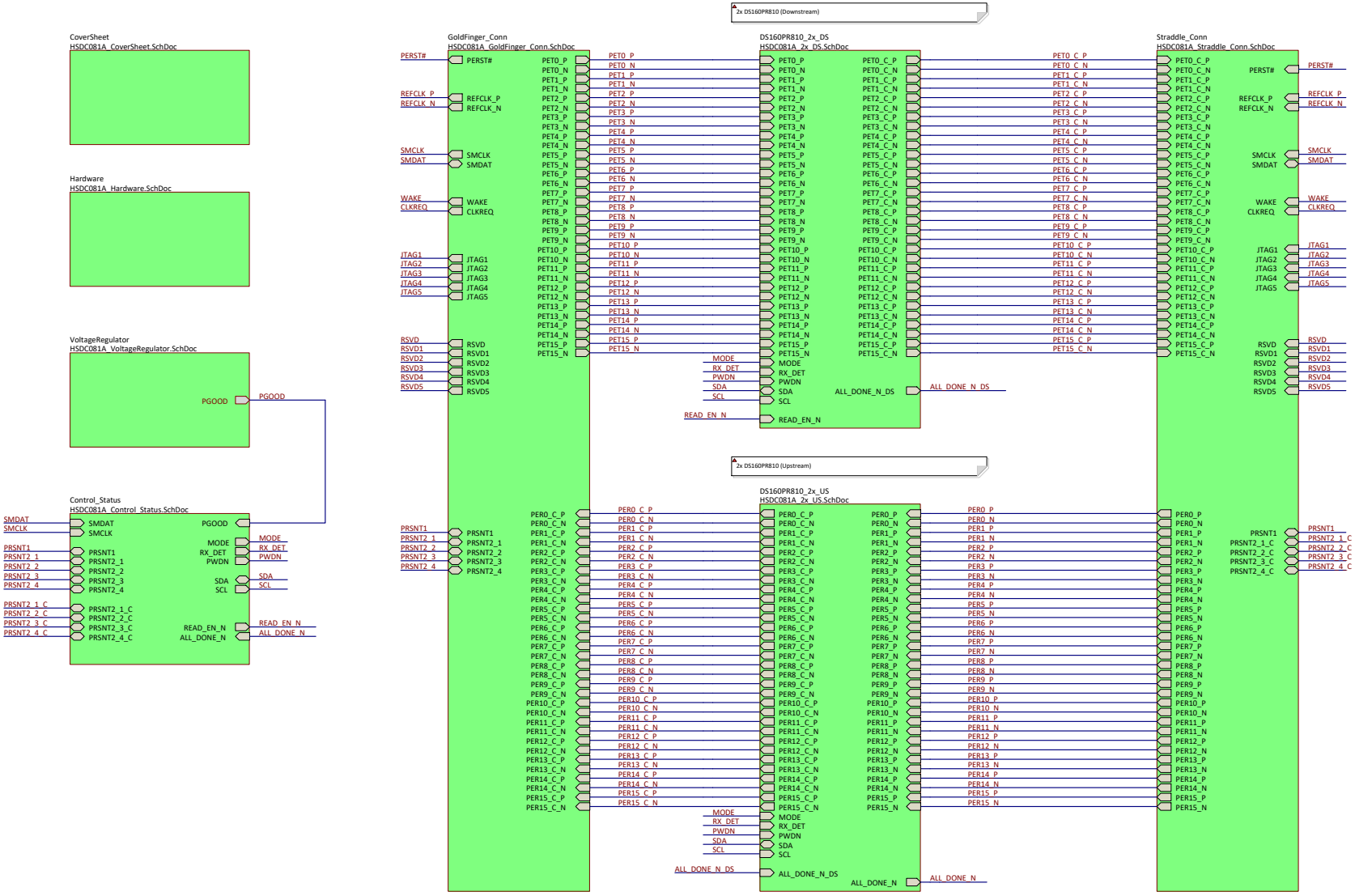


Figure 4-1. Top Level Schematic Page

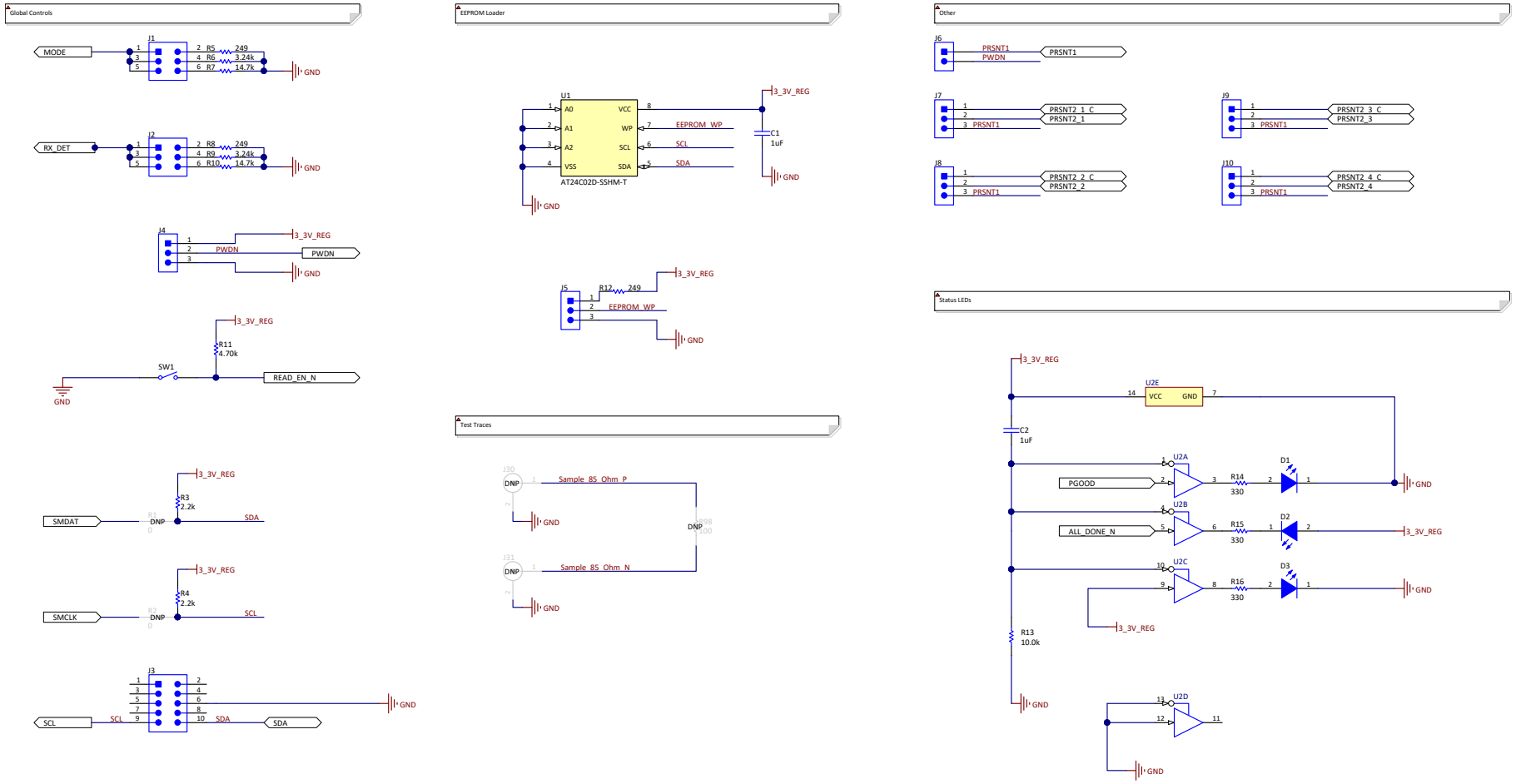


Figure 4-2. Control and Status Schematic Page

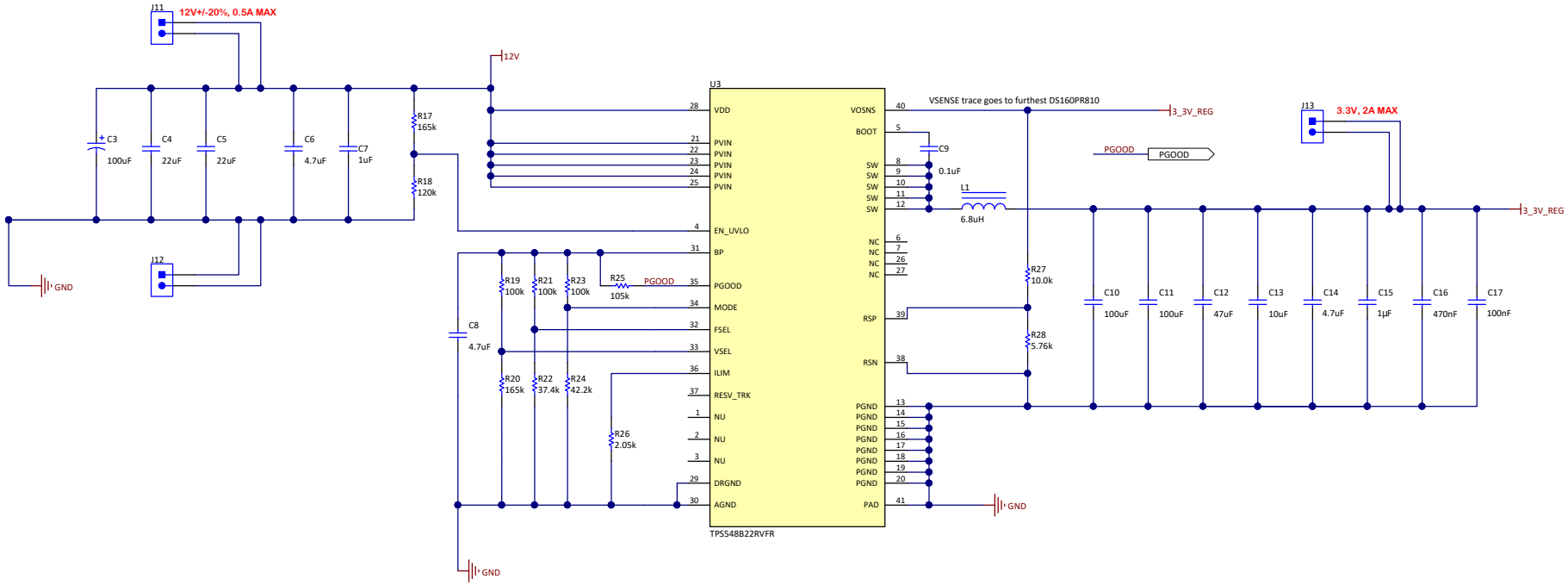


Figure 4-3. Voltage Regulator Schematic Page

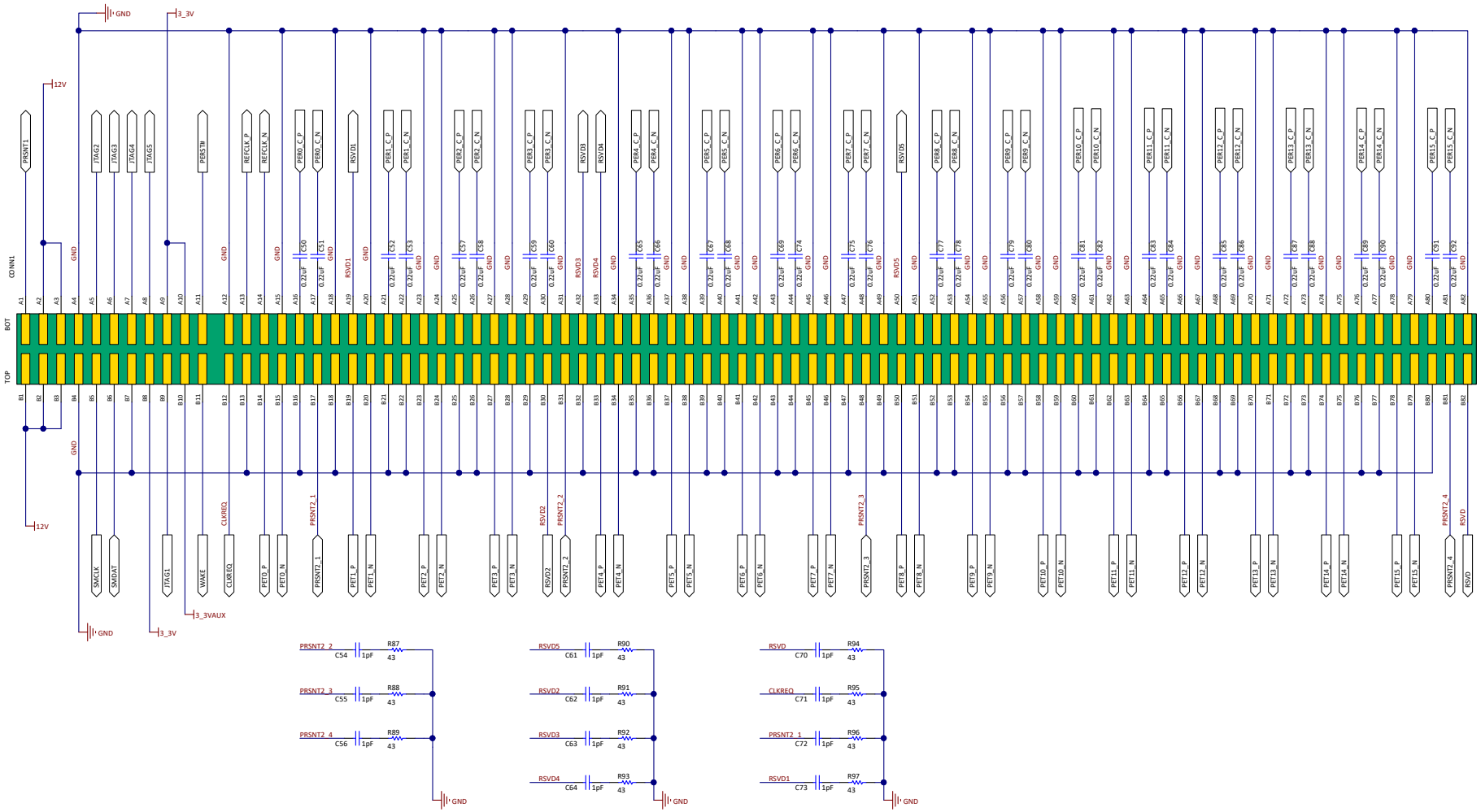


Figure 4-4. Gold Finger Connector Schematic Page

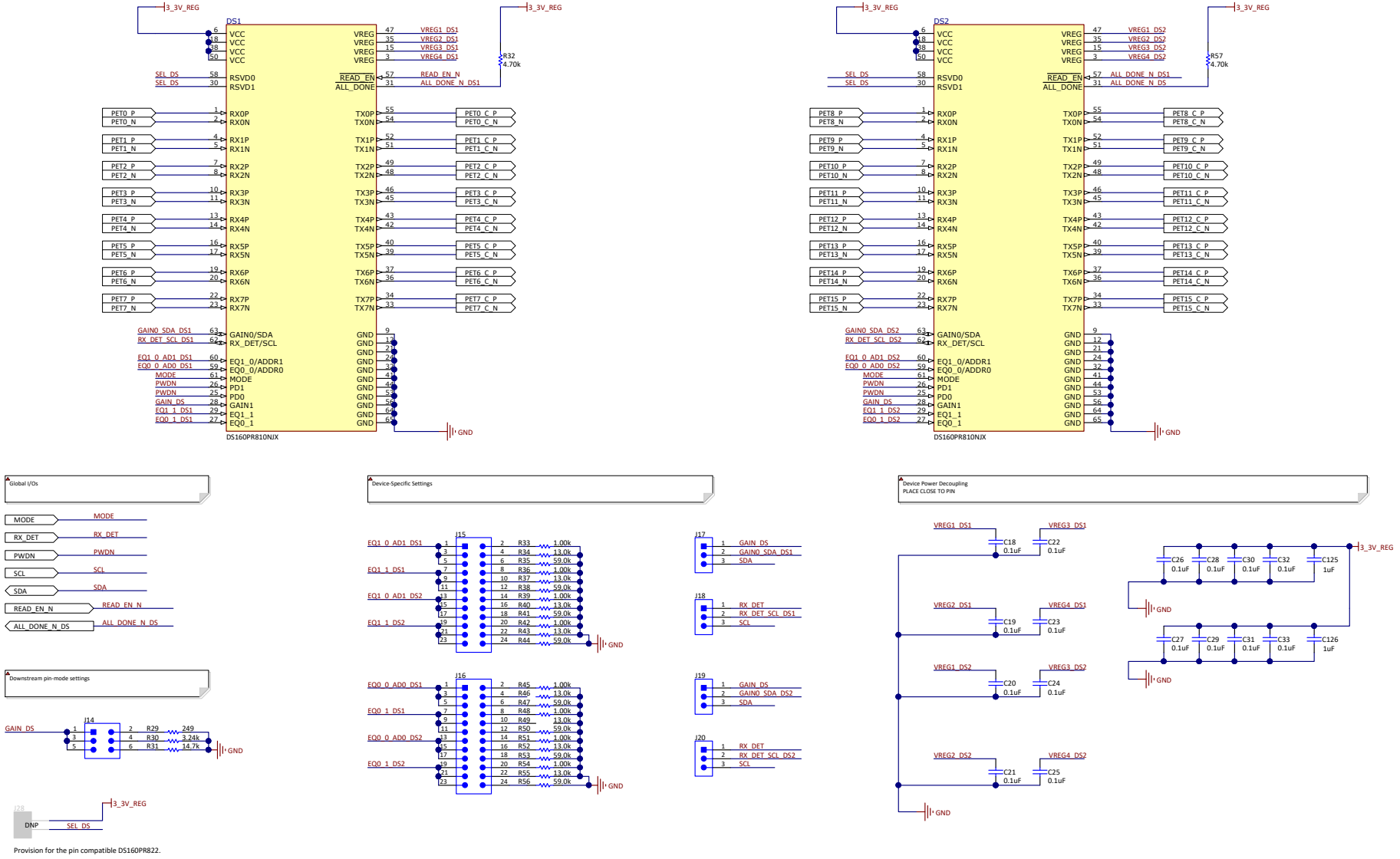


Figure 4-5. Downstream Devices Schematic Page

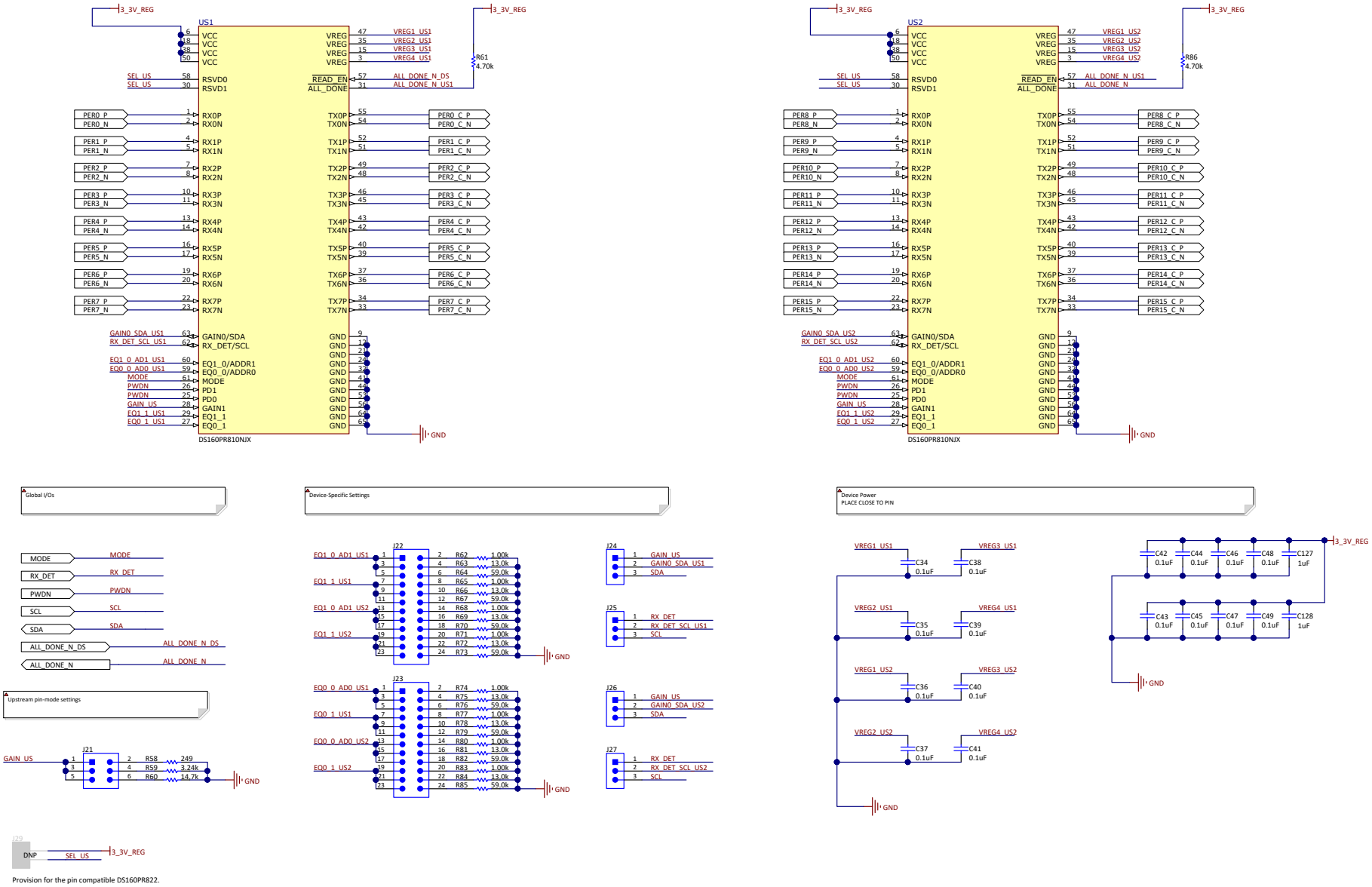


Figure 4-6. Upstream Devices Schematic Page

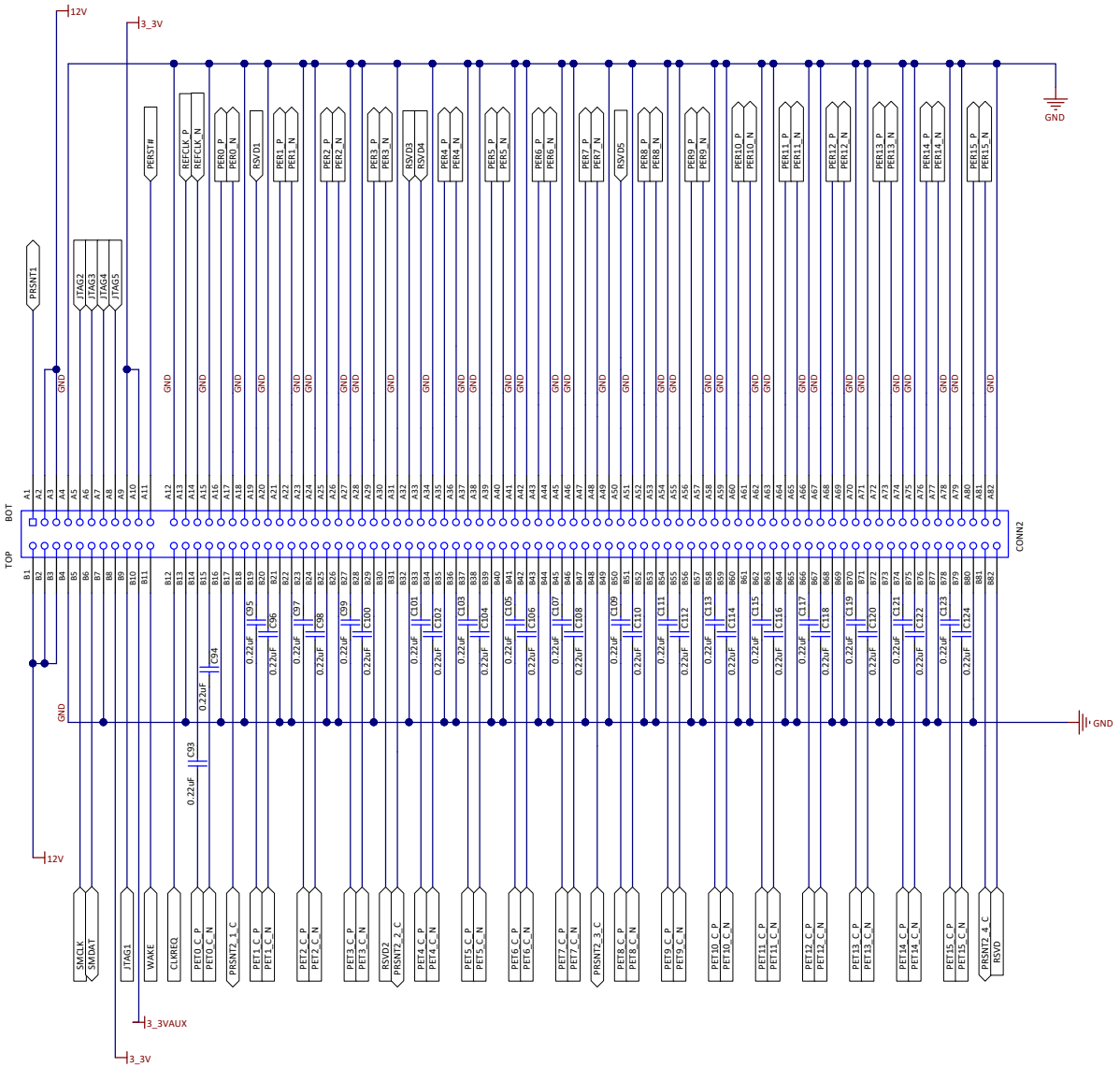
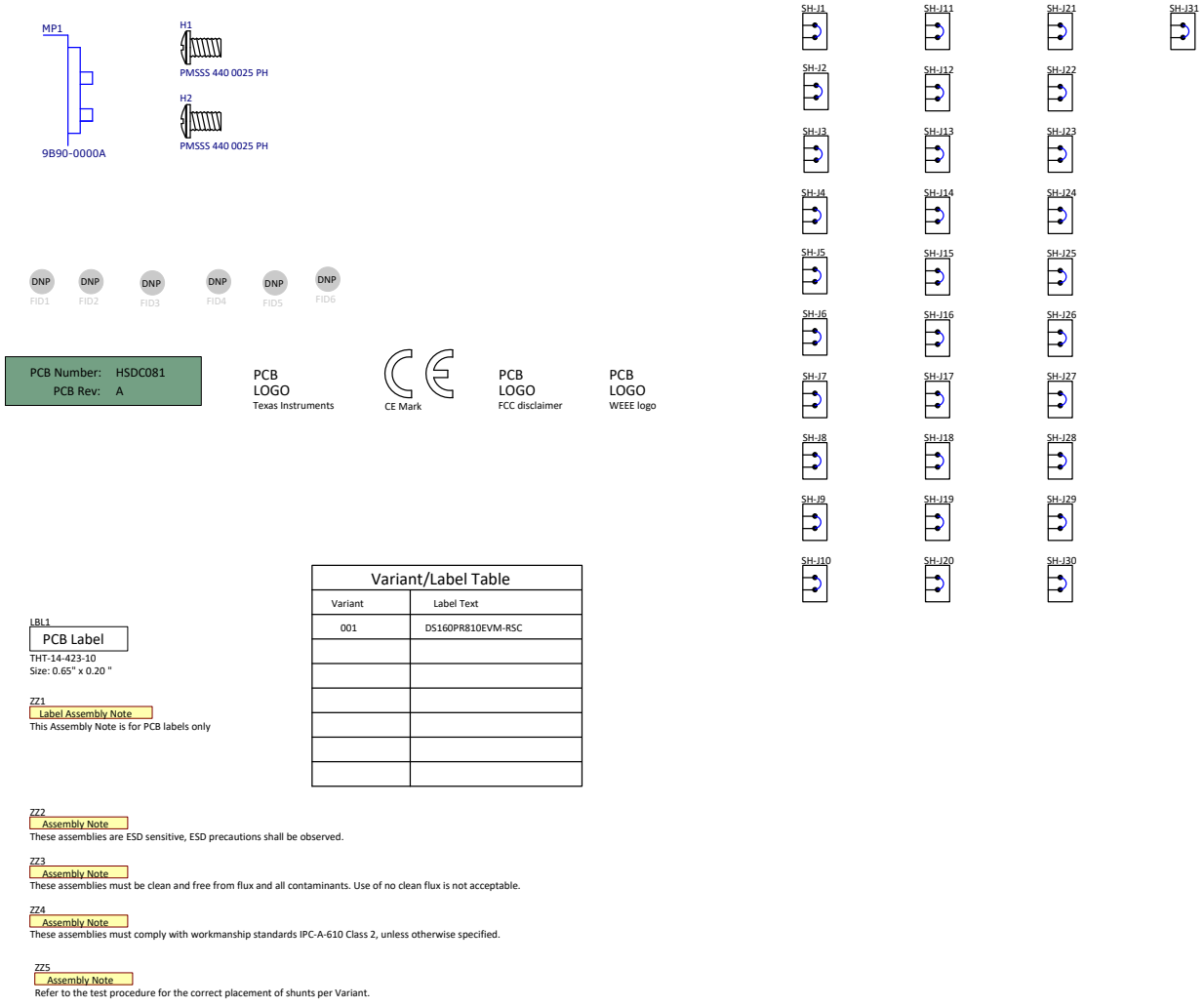


Figure 4-7. Straddle Connector Schematic Page



Variant/Label Table

Variant	Label Text
001	DS160PR810EVM-RSC

Figure 4-8. Hardware Page

5 Board Layout

Figure 5-1 and Figure 5-2 illustrate the EVM board layouts.

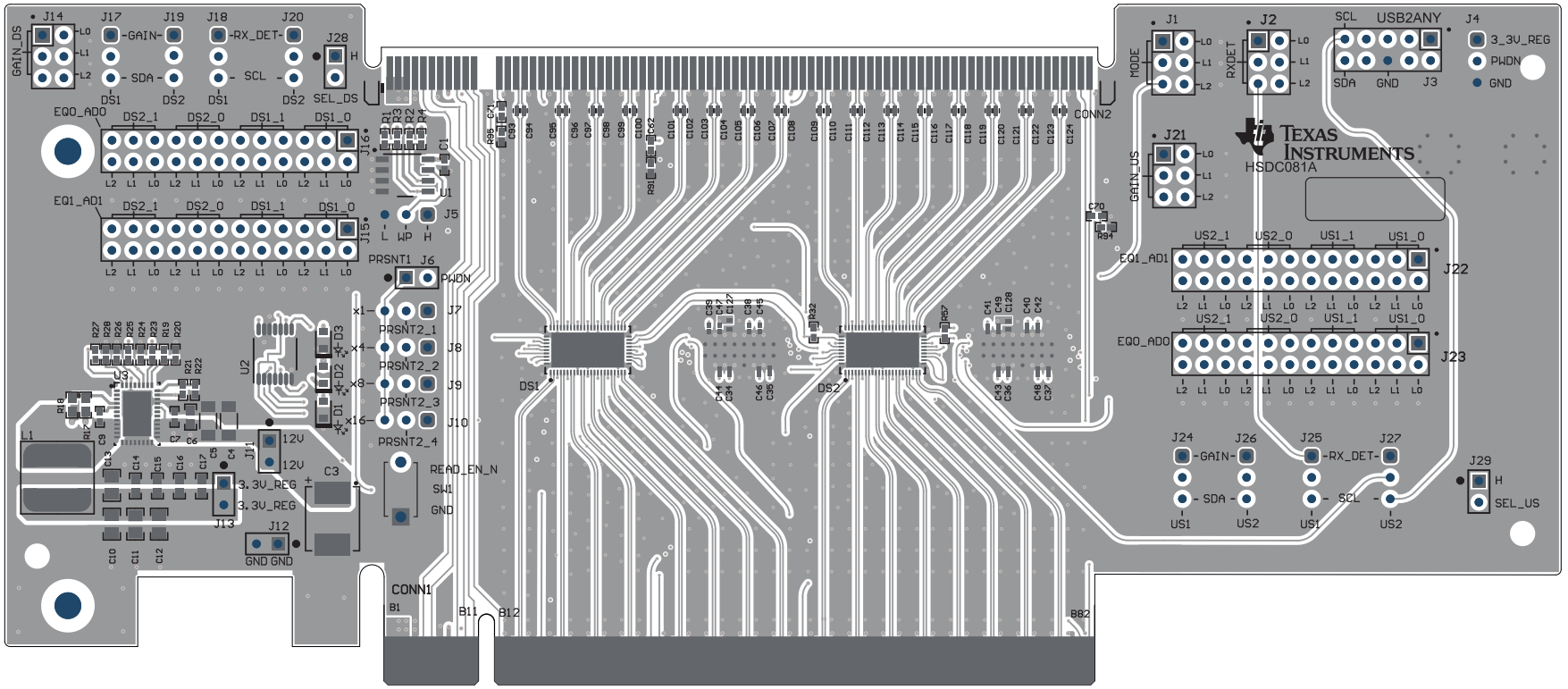


Figure 5-1. Top Layer

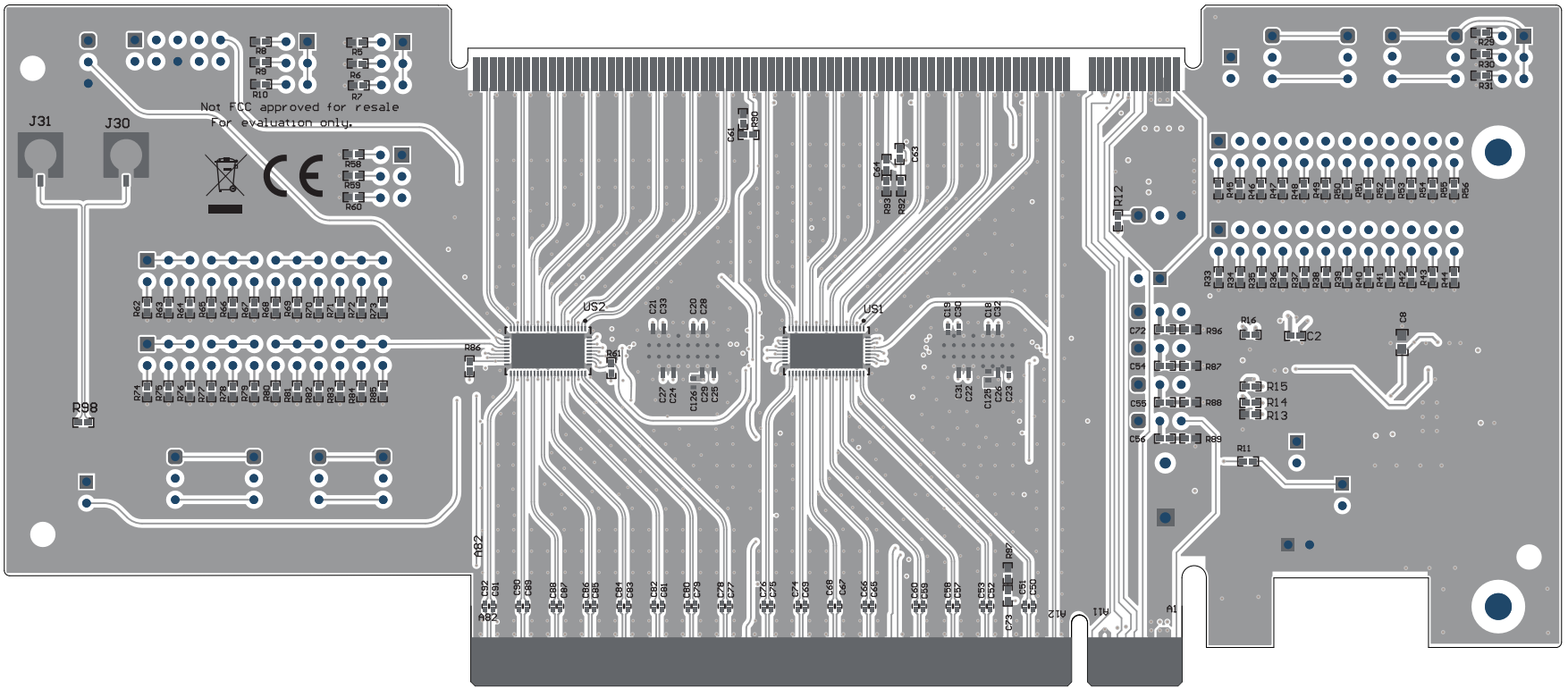


Figure 5-2. Bottom Layer

6 Bill of Materials

Table 6-1 lists the EVM bill of materials.

Table 6-1. Bill of Materials

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
!PCB1	1		Printed Circuit Board		HSDC081	Any
C1, C2, C7, C125, C126, C127, C128	7	1uF	CAP, CERM, 1 uF, 25 V, ±10%, X5R, 0402	0402	C1005X5R1E105K050BC	TDK
C3	1	100uF	CAP, TA, 100 uF, 25 V, ±10%, 0.1 ohm, SMD	7360-38	T495E107K025ATE100	Kemet
C4, C5	2	22uF	CAP, CERM, 22 uF, 25 V, ±20%, X5R, 1206_190	1206_190	TMK316BBJ226ML-T	Taiyo Yuden
C6, C8	2	4.7uF	CAP, CERM, 4.7 uF, 25 V, ±10%, X6S, 0603	0603	GRM188C81E475KE11D	MuRata
C9	1	0.1uF	CAP, CERM, 0.1 uF, 35 V, ±10%, X5R, 0402	0402	GMK105BJ104KV-F	Taiyo Yuden
C10, C11	2	100uF	CAP, CERM, 100 uF, 6.3 V, ±20%, X5R, 0805	0805	GRM21BR60J107M	MuRata
C12	1	47uF	CAP, CERM, 47 uF, 6.3 V, ±20%, X5R, 0805	0805	GRM219R60J476ME44D	MuRata
C13	1	10uF	CAP, CERM, 10 uF, 6.3 V, ±10%, X5R, 0805	0805	C0805C106K9PAC	Kemet
C14	1	4.7uF	CAP, CERM, 4.7 uF, 6.3 V, ±10%, X5R, 0603	0603	C0603C475K9PACTU	Kemet
C15	1	1uF	CAP, CERM, 1 uF, 25 V, ±10%, X7R, 0603	0603	C0603C105K3RACTU	Kemet
C16	1	0.47uF	CAP, CERM, 0.47 uF, 6.3 V, ±10%, X7R, 0603	0603	C0603C474K9RACTU	Kemet
C17	1	0.1uF	CAP, CERM, 0.1 uF, 10 V, ±10%, X7R, 0603	0603	C0603C104K8RACTU	Kemet
C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C47, C48, C49	32	0.1uF	CAP, CERM, 0.1 uF, 6.3 V, ±10%, X5R, 0201	0201	GRM033R60J104KE84D	MuRata

Table 6-1. Bill of Materials (continued)

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
C50, C51, C52, C53, C57, C58, C59, C60, C65, C66, C67, C68, C69, C74, C75, C76, C77, C78, C79, C80, C81, C82, C83, C84, C85, C86, C87, C88, C89, C90, C91, C92, C93, C94, C95, C96, C97, C98, C99, C100, C101, C102, C103, C104, C105, C106, C107, C108, C109, C110, C111, C112, C113, C114, C115, C116, C117, C118, C119, C120, C121, C122, C123, C124	64	0.22uF	CAP, CERM, 0.22 uF, 10 V, ±20%, X5R, 0201	0201	LMK063BJ224MP-F	Taiyo Yuden
C54, C55, C56, C61, C62, C63, C64, C70, C71, C72, C73	11	1pF	CAP, CERM, 1 pF, 50 V, ±10%, C0G/NP0, 0402	0402	GJM1555C1H1R0BB01D	MuRata
CONN2	1		Receptacle, 1mm, 82x2, Gold, SMT	Receptacle, 1mm, 82x2, SMT	GWE82DHRN-T9410	Sullins Connector Solutions
D1, D2, D3	3	Green	LED, Green, SMD	2x1.4mm	LG M67K-G1J2-24-Z	OSRAM
DS1, DS2, US1, US2	4		Octal-Channel PCI Express 4.0 Linear Redriver	WQFN64	DS160PR810NJX	Texas Instruments
H1, H2	2		MACHINE SCREW PAN PHILLIPS 4-40	Machine Screw, 4-40, 1/4 inch	PMSSS 440 0025 PH	B and F Fastener Supply
J1, J2, J14, J21	4		Header, 100mil, 3x2, Gold, TH	3x2 Header	TSW-103-07-G-D	Samtec
J3	1		Header, 100mil, 5x2, Gold, TH	5x2 Header	TSW-105-07-G-D	Samtec
J4, J5, J7, J8, J9, J10, J17, J18, J19, J20, J24, J25, J26, J27	14		Header, 100mil, 3x1, Gold, TH	3x1 Header	TSW-103-07-G-S	Samtec
J6, J11, J12, J13	4		Header, 100mil, 2x1, Gold, TH	Header, 2x1, 100mil	5-146261-1	TE Connectivity
J15, J16, J22, J23	4		Header, 100mil, 12x2, Gold, TH	12x2 Header	TSW-112-07-G-D	Samtec
L1	1	6.8uH	Inductor, Drum Core, Ferrite, 6.8 uH, 3.2 A, 0.04 ohm, SMD	SDR0805	SDR0805-6R8ML	Bourns
LBL1	1		Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	PCB Label 0.650 x 0.200 inch	THT-14-423-10	Brady
MP1	1		PCI bracket	PCI_BRCKT_NPTH_2	9B90-0000A	Gompf Brackets, Inc.
R3, R4	2	2.2k	RES, 2.2 k, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04022K20JNED	Vishay-Dale
R5, R8, R12, R29, R58	5	249	RES, 249, 1%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2RKF2490X	Panasonic
R6, R9, R30, R59	4	3.24k	RES, 3.24 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04023K24FKED	Vishay-Dale

Table 6-1. Bill of Materials (continued)

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
R7, R10, R31, R60	4	14.7k	RES, 14.7 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040214K7FKED	Vishay-Dale
R11, R32, R57, R61, R86	5	4.70k	RES, 4.70 k, 1%, 0.063 W, 0402	0402	CRG0402F4K7	TE Connectivity
R13	1	10.0k	RES, 10.0 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	AC0402FR-0710KL	Yageo America
R14, R15, R16	3	330	RES, 330, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402330RJNED	Vishay-Dale
R17	1	165k	RES, 165 k, 1%, 0.1 W, 0603	0603	RC0603FR-07165KL	Yageo
R18	1	120k	RES, 120 k, 1%, 0.1 W, 0603	0603	RC0603FR-07120KL	Yageo
R19, R21, R23	3	100k	RES, 100 k, 1%, 0.0625 W, 0402	0402	RC0402FR-07100KL	Yageo America
R20	1	165k	RES, 165 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2RKF1653X	Panasonic
R22	1	37.4k	RES, 37.4 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040237K4FKED	Vishay-Dale
R24	1	42.2k	RES, 42.2 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040242K2FKED	Vishay-Dale
R25	1	105k	RES, 105 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402105KFKED	Vishay-Dale
R26	1	2.05k	RES, 2.05 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04022K05FKED	Vishay-Dale
R27	1	10.0k	RES, 10.0 k, 1%, 0.063 W, 0402	0402	RC0402FR-0710KL	Yageo America
R28	1	5.76k	RES, 5.76 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04025K76FKED	Vishay-Dale
R33, R36, R39, R42, R45, R48, R51, R54, R62, R65, R68, R71, R74, R77, R80, R83	16	1.00k	RES, 1.00 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW04021K00FKED	Vishay-Dale
R34, R37, R40, R43, R46, R49, R52, R55, R63, R66, R69, R72, R75, R78, R81, R84	16	13.0k	RES, 13.0 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040213K0FKED	Vishay-Dale
R35, R38, R41, R44, R47, R50, R53, R56, R64, R67, R70, R73, R76, R79, R82, R85	16	59.0k	RES, 59.0 k, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040259K0FKED	Vishay-Dale
R87, R88, R89, R90, R91, R92, R93, R94, R95, R96, R97	11	43	RES, 43, 5%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW040243R0JNED	Vishay-Dale

Table 6-1. Bill of Materials (continued)

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
SH-J1, SH-J2, SH-J3, SH-J4, SH-J5, SH-J6, SH-J7, SH-J8, SH-J9, SH-J10, SH-J11, SH-J12, SH-J13, SH-J14, SH-J15, SH-J16, SH-J17, SH-J18, SH-J19, SH-J20, SH-J21, SH-J22, SH-J23, SH-J24, SH-J25, SH-J26, SH-J27, SH-J28, SH-J29, SH-J30, SH-J31	31	1x2	Shunt, 100mil, Flash Gold, Black	Closed Top 100mil Shunt	SPC02SYAN	Sullins Connector Solutions
SW1	1		Switch, Tactile, SPST-NO, 0.05A, 12V, TH	SW, SPST 3.5x5 mm	PTS635SL50LFS	C and K Components
U1	1		I2C-Compatible (2-wire) Serial EEPROM 2-Kbit (256 x 8), SOIC-8	SOIC-8	AT24C02D-SSHM-T	Atmel
U2	1		Quadruple Bus Buffer Gate With 3-State Outputs, PW0014A, LARGE T and R	PW0014A	SN74LVC125APWRG3	Texas Instruments
U3	1		1.5-V to 16-V VIN, 4.5-V to 22-V VDD, 25-A SWIFT Synchronous Step-Down Converter with Full Differential Sense, RVF0040A (LQFN-CLIP-40)	RVF0040A	TPS548B22RVFR	Texas Instruments
FID1, FID2, FID3, FID4, FID5, FID6	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A
J28, J29	0		Header, 100mil, 2x1, Gold, TH	Header, 2x1, 100mil	5-146261-1	TE Connectivity
J30, J31	0		Plug, 50 Ohm, Straight, SMT	SMA Plug, Straight, SMT	0853050232	Molex
R1, R2	0	0	RES, 0, 5%, 0.1 W, AEC-Q200 Grade 0, 0402	0402	ERJ-2GE0R00X	Panasonic
R98	0	100	RES, 100, 1%, 0.063 W, AEC-Q200 Grade 0, 0402	0402	CRCW0402100RFKED	Vishay-Dale

7 References

For references, see the following:

1. Texas Instruments, *DS160PR810 Octal-Channel PCI-Express 4.0 Linear Redriver Data Sheet*
2. Texas Instruments, *DS160PR810 Programming Guide*
3. Texas Instruments, *Understanding EEPROM Programming for DS160PR810 PCI-Express 4.0 Linear Redriver*
4. Texas Instruments, *CEM2SLIMSAS-EVM Evaluation Module (EVM) User's Guide*

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