LF347,LF351,LF353,LF355,LF356,LF357, LF411,LF412,LF441,LF442,LF444,TL081, TL082

Application Note 447 Protection Schemes for BI-FET Amplifiers and Switches

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Protection Schemes for BI-FET™ Amplifiers and Switches

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To use integrated circuits in real applications, designers must know the limitations of the devices. The majority of the limitations are published in the datasheets, and these fall into two categories: Absolute Maximums — which, if violated, can cause damage or destruction of the device; and Electrical Characteristics — which indicate the performance limitations. Unfortunately, these specifications don't explain the consequences of a violation, nor what may happen between the violation of an Electrical Characteristic limit and an Abs. Max. limit. This information is needed so the designer can design an appropriate protection scheme.

This article will focus on National Semiconductor Corp. BI-FET op amps: how to improve their reliability and performance. In most cases, the results are similar for bipolar op amps also.

THE BI-FET FAMILIES

Our BI-FET op amps are divided into families: LF411, LF441 and LF356. The LF411 family consists of LF411, LF351, and TL081 (all singles); LF412, LF353, and TL082 (duals); and LF347 (quad). This is a good general purpose set of op amps that all have the same internal design, differing only by grade.

The LF441 family consists of the LF441 (single), LF442 (dual), and LF444 (quad). This family gives nearly the same DC performance as the LF411's for 1/12th the supply current. However, because they are low-power devices, they are also proportionally slower than the 411's.

The LF356 family includes the LF355, LF356, and LF357 (in the commercial temperature range). The 355 is the low-I_{cc} part, and the 357 is the wide-bandwidth part. All of the family have good DC specs and can drive a lot of capacitance (to .01 µF, typically). They are also among our faster op amps, having slew rates which vary from 5V/µs (for the 355) to 50V/µs (for the 357).

The operating restrictions for these families are nearly all the same, as are the methods of protection. In some cases (as will be pointed out) certain families are better at surviving the abuses than others.

EXCEEDING COMMON-MODE INPUT VOLTAGE RANGE

The input common-mode range of any operational amplifier is the range of voltages on the input terminals for which the amplifier operates correctly. To understand what happens when the common-mode range is exceeded, four cases must be considered: open- and closed-loop operation at both the positive and negative common-mode limits.

Exceeding Negative Common-Mode Limit

In open-loop operation (i.e., no feedback from output to inverting input, or, during any time that the op amp is slew-rate limited), taking the non-inverting input below the inverting input causes the output to slew toward the negative supply rail. If the voltage at the non-inverting input is more negative than the negative common-mode limit, the input stage ceases to function properly and the output swings to its positive limit. This apparent "phase-reversal" is temporary; bringing the non-inverting input back within the legal input common-mode range restores the part's normal operation.

If the inverting input is taken below the non-inverting input while the op amp is operated open-loop, the output slews toward the positive rail. Exceeding the negative common-mode limit in this condition does not cause a "phase reversal", as the output will still head toward, or remain at, the positive rail.

In closed-loop operation, exceeding the negative common-mode at either input limit, also causes the output to swing to the positive supply rail.

Exceeding Positive Common-Mode Limit

In general, the positive common-mode limit is at or beyond the positive supply. Taking either input above the positive common-mode limit while in open-loop operation does not cause a "phase reversal" at the output; the output will slew toward whichever rail one might expect. However, if both inputs are driven above the positive common-mode limit, the output will slew to the positive rail. In addition, while operating in a closed-loop mode, taking either input above the positive common-mode limit will also drive the output to the positive rail.

INPUTS EXCEEDING SUPPLY RAILS

If either input is pulled above V^+, nothing happens until the difference between the input and V^+ gets near the breakdown voltage, typically 50V. At this point, the FET's gate-source junction avalanches and will draw all the current it can. Limiting this input current to something less than 3 mA helps prevent damage. The best protection (in addition to limiting the input current) is a diode clamp from each input to V^+. If transients are expected, use a fast-recovery diode, such as a IN4148. For low-leakage (but less speed), the C-B junction of a good transistor (i.e. 2N3904) is recommended.

Failure to clamp the voltage or limit the current adequately may not destroy the part, but the offset voltage and bias current will be permanently degraded.

If either input is pulled more than a few tenths of a Volt below V^- (even if this pin is floating), a lightly-doped parasitic substrate transistor turns on. This transistor's collector current cannot be controlled externally, so allowing it to turn on can cause metal migration and destruction of the input stage (or at least a major unbalancing). In the newer LF411 and LF441 families, this transistor has been controlled by the addition of a diode from base to emitter which kills the gain of the transistor and keeps its current low. Any input current should still be limited to 1 mA or less. However, the older parts and members of the LF356 family are still susceptible, so it is best to protect all the BI-FETs from this potential abuse by using the clamp diodes (see *Figure 1* below).

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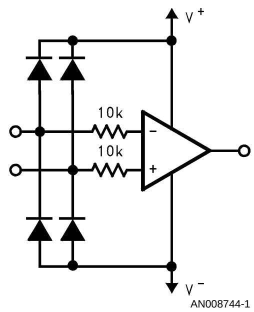

FIGURE 1. Clamping Inputs of Op Amp

Since this parasitic transistor turns on easily, the best way to keep it turned off is to use a Schottky diode, its on-voltage being less than that required to turn on the transistor. For lower leakage, a short-base switching diode (such as the Fairchild FD200 series) may be used. Its forward drop will be larger at low currents, but will stay constant for a wide current range, as opposed to the relatively leaky Schottky diodes.

POWER SUPPLY SEQUENCING

Adding the clamp diodes shown in *Figure 1* not only protects the inputs from transients when the circuit is operating, but protects them as power is being applied to the circuit. Because the parasitic transistor appears when the input voltage is less than the negative supply, applying the positive supply or input voltage before the negative supply is applied can cause this problem. For this reason, it is always recommended that the negative supply be turned on **first**, if the supplies can be turned on independently. This is especially important for protection of the BI-FET switches.

Also, even if the input stage is well protected with clamp diodes and current limiting, the inputs should not be allowed to be heavily unbalanced (for example, one input at ground and the other at the rail) for extended periods of time (for example, many hours). The long-term effects of an unbalanced differential pair are increased offset voltage and offset current.

SUPPLY VOLTAGES OUT OF RECOMMENDED RANGE

Attempting to run a BI-FET on supply voltages less than the recommended total of 10V will narrow the common-mode input and output ranges, and slow the part down. In the LF411 family, at supply voltages less than 7V, an internal biasing zener turns off and the entire part quits working. With the LF441 family, a supply voltage of less than 6V is not enough to support the internal current source biasing, so eventually these also turn off. And the LF356 family needs all of the 10V to stay in operation.

Running the BI-FETs on supply voltages greater than the Abs. Max limit generally does no harm until the parasitic diode from V^+ to the substrate breaks down (in LV_{ceo}) or the input gate-source junction breaks down (BV_{gso}). Limiting the supply current to something less than 10 mA improves the chances of the op amp's survival. These breakdowns typically occur at about 50V, but the devices are only tested up to 36V or 40V, depending on the device. In addition, power dissipation must be considered when the supply voltage is large.

OPERATING TEMPERATURE OUT OF ABSMAX RANGE

BI-FETs generally operate well when the ambient temperature is cold. The bias current becomes minimal, the input noise often decreases, and the bandwidth increases. However, if the device is in a marginally stable design, it may oscillate as its phase margin will also decrease.

Conversely, running the BI-FETs at temperatures greater than 100˚C brings the bias current into the nanoamp range, and drops the gain-bandwidth product by 20% or more (compared to 25˚C performance). Most op amps quit working between 180˚C and 250˚C due to excessive leakage currents or internal thermal shutdown mechanisms, and the BI-FETs are no exception. The maximum guaranteed junction (die) temperature of our ICs is 150˚C, and some lower-grade parts and those in plastic DIP packages are guaranteed to as low as 100˚C.

The type of package used affects the maximum ambient temperature allowed, since the junction temperature must remain in the "legal" range and the different packages have different heat-sinking properties. The metal can packages have the lowest thermal resistance, and have the additional advantage that heat-sink fins are easy to find and attach to the package (when needed).

DRIVING CAPACITANCE

Both the LF411 and LF441 families have a lot of trouble driving more than about 200 pF without oscillating. Standard techniques to get around this problem are to add a small resistor (about 50Ω) in series with the output (see *Figure 2*) or to use one of the LF356 family (the 356 itself being the most popular for this purpose). An explanation of why the 356 output stage is so unusually strong is provided in the second reference listed.

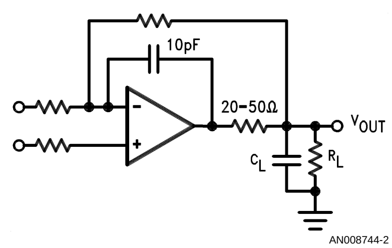

FIGURE 2. Isolating a Capacitive Load

When extra output filtering is desired, a series RC damper will often be more effective than just a large filter capacitor.

POWER SUPPLY BYPASSING

Another potential cause of oscillation is inadequate power supply bypassing.

In addition to the familiar problem of noise added through the supply inputs (due to poor high-frequency rejection), the in-

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ductance of the power supply leads degrades the effectiveness of the op amp's internal compensation, which invites oscillation.

The BI-FETs need the supply bypassing most on their V^- terminals, as do many of the bipolar-input amplifiers. Good bypassing techniques include (1) putting the bypass capacitors right next to the IC, and (2) using an appropriate type and size of capacitor. Ceramic types are often used because of their small size and low cost, but their effectiveness is limited to about 1 MHz. Typical values used are between 0.01 µF and 0.47 µF.

Tantalum capacitors are often used for high-frequency bypassing. However, their lead inductance can sometimes aggravate the situation instead of correcting it. Adding a small (0.01 µF) ceramic disc capacitor in parallel with the tantalum improves the overall performance. Typical values used for tantalum bypass capacitors range from 2.2 µF to 10 µF.

Mylar capacitors are also used for bypassing, but the monolithic ceramics have better high frequency performance and cost less.

Where the supply voltages have poor load regulation, electrolytic capacitors (typically 10 µF to 47 µF) can provide additional filtering.

DEALING WITH THE OFFSET VOLTAGE

If the offset voltage of a BI-FET op amp is first measured in a test circuit, and then again after the device is installed in the final circuit, a change in V_{os} will often be detected. This is due to a difference in stress put on the die when the device (packaged or not) is installed in the two circuits. Because the input JFETs are largely surface devices, any stress on them changes their characteristics noticeably. This, then, changes the V_{os} of the input stage. This problem is more apparent with the larger devices and packages, i.e. when there is more surface to be stressed. Thus, the most sensitive would be a large quad in a 14-pin DIP; the least, a small single op amp in a metal can (TO-5) package.

To improve the accuracy of the BI-FET op amps, the offset voltage should be nulled after the devices are in their final circuits. The BI-FET offset voltage has an associated drift of between 2 µV/˚C and 10 µV/˚C (depending on the device) for every millivolt of offset at room temperature. The V_{os} null schemes will affect the offset drift; it is equally likely that the drift will increase rather than decrease, because the sources of BI-FET V_{os} are complex.

The easiest V_{os} cancelling technique is the trim scheme provided in the op amp's datasheet. The LF411 and LF441 require a 10k potentiometer between the trim pins (1 and 5), with the wiper to V^-. The LF356 family requires a 25k pot with the wiper to V^+. A larger pot would extend the trim range, but this is not necessary since the specified resistance is sufficient to correct even the worst case V_{os}.

Dual and quad op amps have no trim pins, so they are used most often when small offsets can be tolerated. An external bias voltage can be added at the input to cancel the V_{os} at a given ambient temperature (T_A). Typical trim schemes are given in Applications Note AN-3.

In general, the reasons for the Abs. Max. ratings and recommendations are a combination of convention and necessity. Exceeding the ratings and recommendations does not always mean death of the op amp, but the reliability and performance of the amplifier are kept at their highest when the part is used properly and protected from excesses.

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