

AN-1813 LP2998 Evaluation Board

The LP2998 evaluation board is designed to provide the design engineer with a fully functional prototype system in which to evaluate the LP2998 in both a static environment and with a complete memory system. This application note contains information regarding the board, for more information please refer to the *LP2998 DDR-I and DDR-II Termination Regulator* ([SNVS521](#)) data sheet.

1 Schematic

The following schematic was used to create the layout.

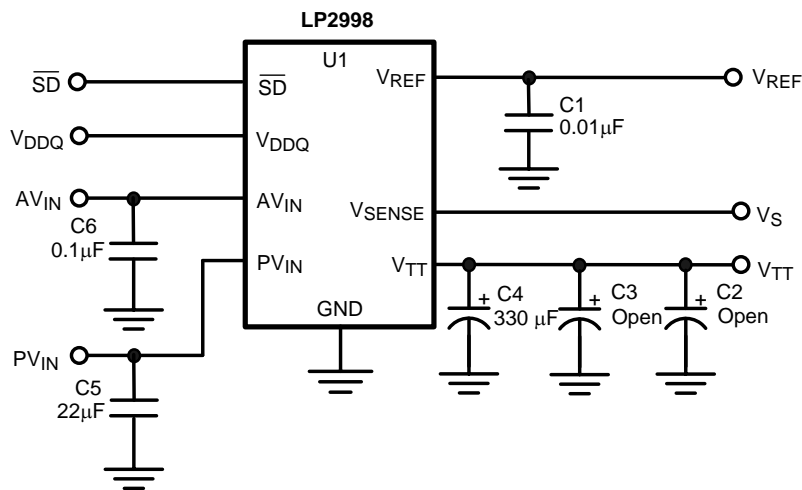


Figure 1. Schematic Used to Create Layout

Table 1. Bill of Materials

Name	Value	Description	Manufacturer	Model Number
U1		LP2998 DDR Linear Regulator	National Semiconductor	LP2998 or LP2998
C6	0.1 μ F	0805 Ceramic Capacitor X7R 16V	MuRata	GRM219R71C104KA01
C4	330 μ F	6.3V ,D3L. POSCAP	Sanyo	6TPE330MIL
C1	0.01 μ F	0805 Ceramic Capacitor X7R 25V	MuRata	GRM216R71E103KA01
C5	22 μ F	0805 Ceramic Capacitor X5R 6.3V	MuRata	GRM21BR60J226ME39
C2, C3	Open			

2 Application

The LP2998 evaluation board can be used immediately in either a static test environment to check functionality or in a memory termination scheme on a motherboard. In either implementation the following steps should be taken to ensure correct operation.

1. Connect AVIN and PVIN to a 2.5V power supply. The voltage on AVIN and PVIN can be separated provided the voltage on ether does not exceed 5.5V and is greater than the minimum operating voltage specified in the datasheet.
2. The VDDQ input provides the internal divide by two reference voltage. Both VREF and VTT will track this internal voltage, nominally a 2.5V will be applied for DDR I and a 1.8V supply for DDR II applicaitons.
3. The VREF pin is the output for the VREF from the LP2998 after being bypassed by a ceramic capacitor. This can be connected either to a multimeter for confirmation or directly to the memory controller and DIMMS.
4. The SD pin can be initially left floating as it has an internal pull-up
5. The remaining two pins are for the force and sense leads of the VTT output. These should be connected directly to the termination plane or a multimeter if interested in verification. The output will be regulated where the VS lead connects to VTT. Remote sensing with VS permits a connection to a motherboard without suffering from large resistance drops.

3 Performance

The LP2998 has been designed to accommodate several different capacitor options to allow the designer to optimize the solution for the specific application. For most desktop systems large aluminum electrolytic capacitors will be used for their low cost. However, in height limited situations such as laptops fewer high performance capacitors might be implemented such as specialty polymers. The table below lists some of the capacitors that can be used and a vendor that offers that product line.

Capacitor Series	Vendor	Vendor Phone Number
Oscon	Vishay	(207)-324-4140
SP	Panasonic	(714)-373-7857
MLCC	Taiyo Yuden	(800)-348-2496
Aluminum	Panasonic	(714)-373-7857
POSCAP	Sanyo	(619)-661-6835

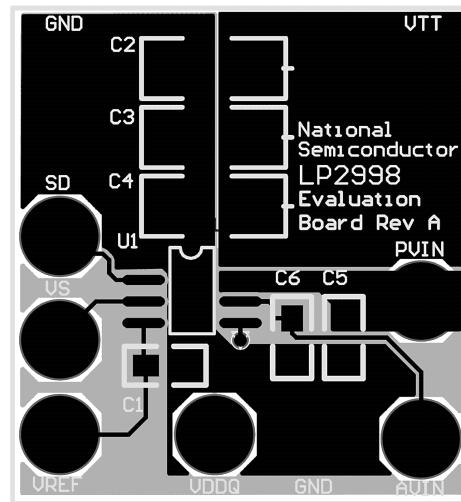


Figure 2. SO PowerPAD™ Top Layer

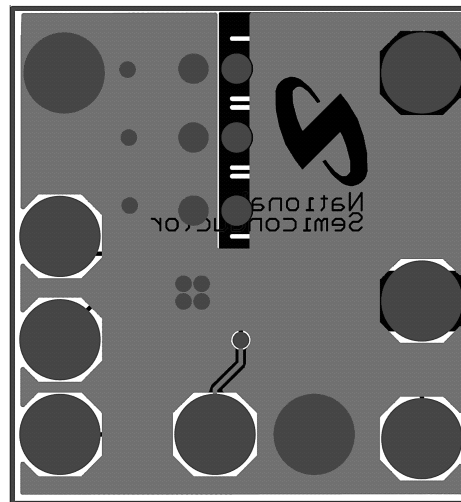


Figure 3. SO PowerPAD Bottom Layer

Information	
Board Material	FR4
Size	1.0 x 1.5 inches
Board Thickness	0.062 inch
Layers	2
Copper Thickness	1oz.
Plating	Immersion Gold
Thermal Vias	4
Thermal Vias Size	12 mil
Board Thickness	0.062 inch

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