

AN-2284 LM34926 Isolated Evaluation Board

1 Introduction

An isolated bias supply is implemented in this evaluation board with LM34926 Constant-On-Time regulator. LM34926 regulator integrates both the high and low side power switches essential for creating isolated buck converter.

Board Specifications:

- Input Range: 20V to 100V
- Primary Output Voltage: 10V
- Secondary (Isolated) Output Voltage: 9.5V
- Maximum Load Current (Primary + Secondary): 250mA
- Maximum Power Output: 2.5W
- Nominal Switching Frequency: 750kHz
- Efficiency (FIN = 36V, IOU2 = 250mA): 77 percent
- Board size: 2 inch x 2 inch

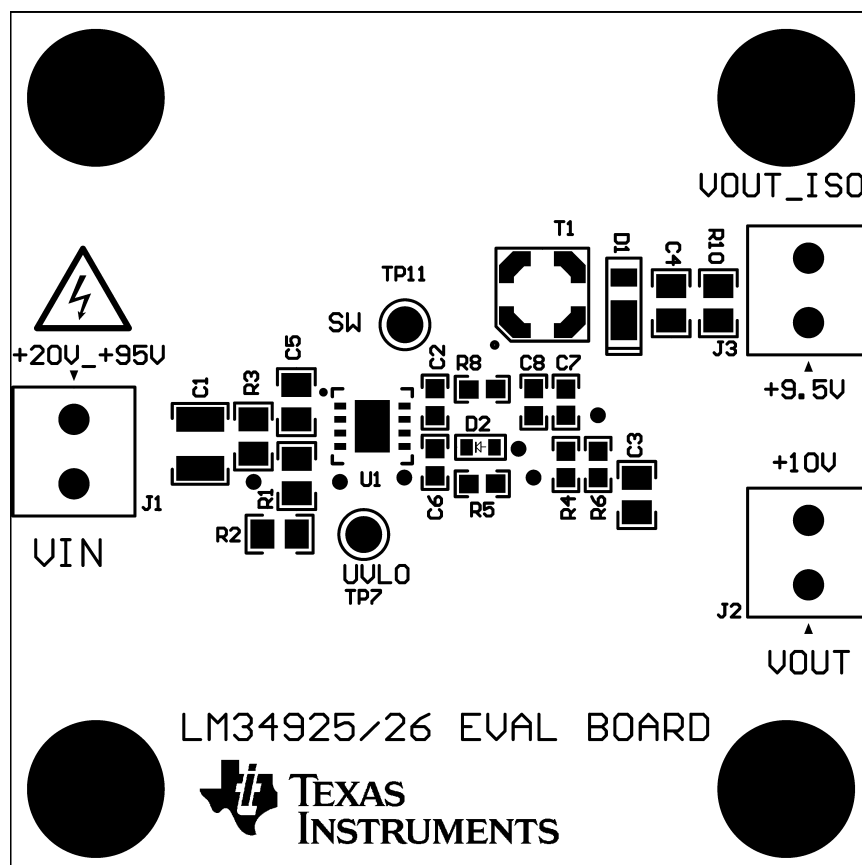


Figure 1. LM34926 Evaluation Board (Top View)

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2 UVLO Threshold and Hysteresis

The UVLO resistors are selected using the following two equations:

$$V_{IN(HYS)} = I_{HYS}R_1 \quad (1)$$

and

$$V_{IN(UVLO, rising)} = 1.225V \times \left(\frac{R_1}{R_2} + 1 \right) \quad (2)$$

On this evaluation board $R_1 = 127k\Omega$ and $R_2 = 8.25k\Omega$, resulting in UVLO rising threshold at $V_{IN} = 20.5V$ and a hysteresis of 2.54V.

2.1 Board Connection and Start-up

The input connections are made using TP1 (V_{IN}) and TP2 (GND) terminals. The primary output appears at TP3 (V_{OUT1}) and TP4 (GND). The secondary (isolated) output is available across TP5 (V_{OUT2}) and TP6 (IGND). The input voltage should be gradually increased above UVLO set point of 20.5V. Both the outputs (V_{OUT1} and V_{OUT2}) should be close to 10V at this point. This board is designed to function with input voltage range of 20V to 100V. The minimum V_{IN} threshold can be changed by changing the UVLO resistors R_1 , R_2 . V_{IN} should not exceed 100V.

The magnetics in this design is optimized for solution size, and therefore limits the output power. **The total load at the output should not exceed 250mA, otherwise the coupled inductor will saturate/overheat, which can destroy both the coupled inductor and the regulator IC U1.** If a sustained over-current situation is to be tolerated, a coupled inductor with higher saturation and rms ratings should be used.

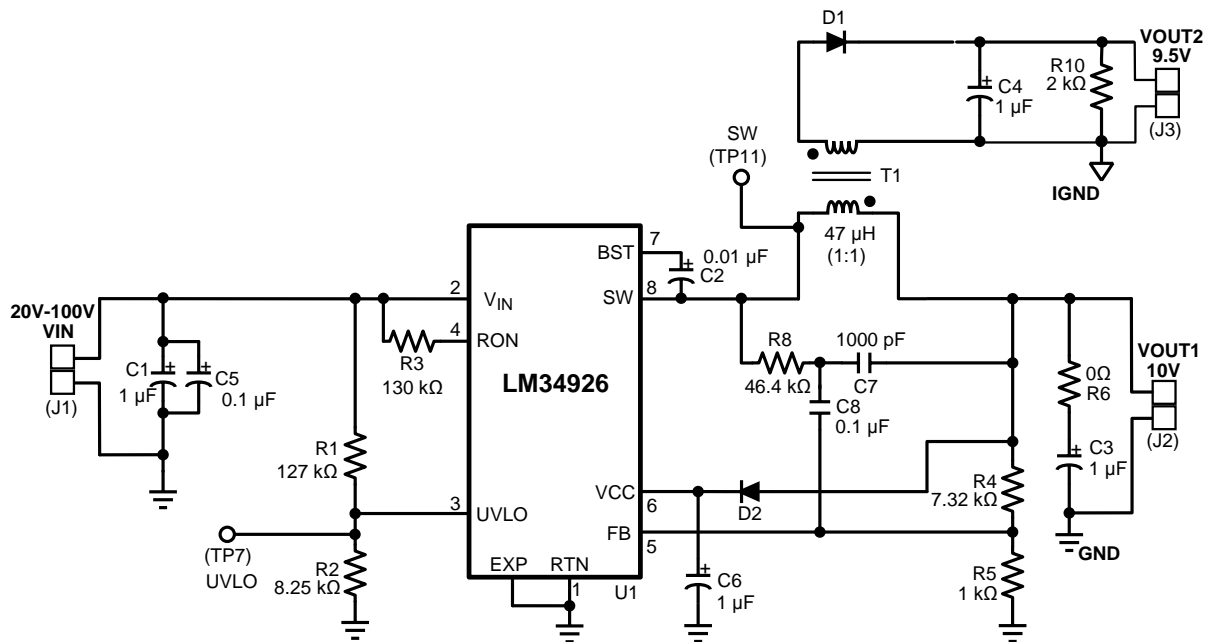


Figure 2. Complete Evaluation Board Schematic

3 Bill of Materials

Table 1. Bill of Materials

| Item | Description | Mfg., Part Number | Package | Value |
|--------|----------------------------|-------------------------------|-----------------|------------------|
| U1 | Sync Switching Regulator | Texas Instruments, LM34926 | WSON-8 | 100V, 300mA |
| T1 | Coupled Inductor, 1500 VDC | Coilcraft, LPD5030V-473ME | 5mm x 5mm | 47uH, 0.47A |
| | Alternate Part | Würth, 750312750 | 8.26mm x 6.60mm | 22uH, 0.76A |
| D1 | Schottky Diode | Diodes Inc., DFSL1100-7 | Pwr-DI123 | 100V, 1A |
| D2 | Schottky Diode | Diodes Inc., SDM10U45-7 | SOD-523 | 40V, 100mA |
| C1 | Ceramic Capacitor | MuRata, GRM32CR72A105KA35L | 1210 | 1uF, 100V, X7R |
| C2 | Ceramic Capacitor | TDK, C1608X7R1C103K | 0603 | 0.01uF, 16V, X7R |
| C3, C4 | Ceramic Capacitor | TDK, C2012X7R1E105K | 0805 | 1uF, 25V, X7R |
| C5 | Ceramic Capacitor | Kemet, C0805C104K1RACTU | 0805 | 0.1uF, 100V, X7R |
| C6 | Ceramic Capacitor | TDK, C1608X7R1C105K | 0603 | 1uF, 16V, X7R |
| C7 | Ceramic Capacitor | Murata, GRM188R71E102KA01D | 0603 | 1000pF, 25V, X7R |
| C8 | Ceramic Capacitor | AVX, 0603YC104KAT2A | 0603 | 0.1uF, 16V, X7R |
| R1 | Resistor | Vishay/Dale, CRCW0805127KFKEA | 0805 | 127kΩ, 1% |
| R2 | Resistor | Vishay/Dale, CRCW08058K25FKEA | 0805 | 8.25kΩ, 1% |
| R3 | Resistor | Vishay/Dale, CRCW0805130KFKEA | 0805 | 130kΩ, 1% |
| R4 | Resistor | Panasonic, ERJ-3EKF7321V | 0603 | 7.32kΩ, 1% |
| R5 | Resistor | Panasonic, ERJ-3EKF1001V | 0603 | 1.0kΩ, 1% |
| R6 | Resistor | Yageo, RC0603JR-070RL | 0603 | 0Ω |
| R8 | Resistor | Panasonic, ERJ-3EKF4642V | 0603 | 46.4kΩ, 1% |
| R10 | Resistor | Panasonic, ERJ-6GEYJ202V | 0805 | 2kΩ, 5% |

4 Performance Curves

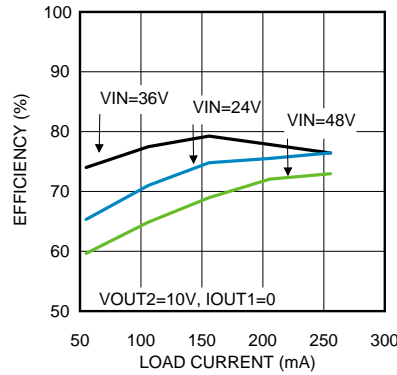


Figure 3. Efficiency at 750kHz, VOUT1=10V

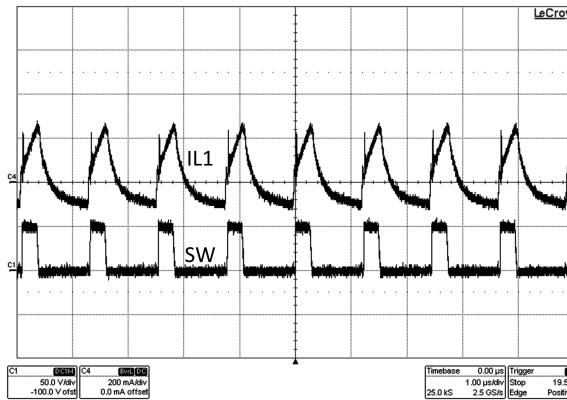


Figure 4. Steady State Waveform (VIN=48V, IOUT1=0mA, IOUT2= 100mA)

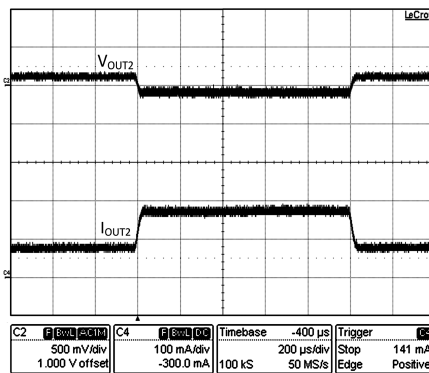


Figure 5. Step Load Response (VIN=48V, IOUT1=0, Step Load on IOUT2=80mA-180mA)

5 PC Board Layout

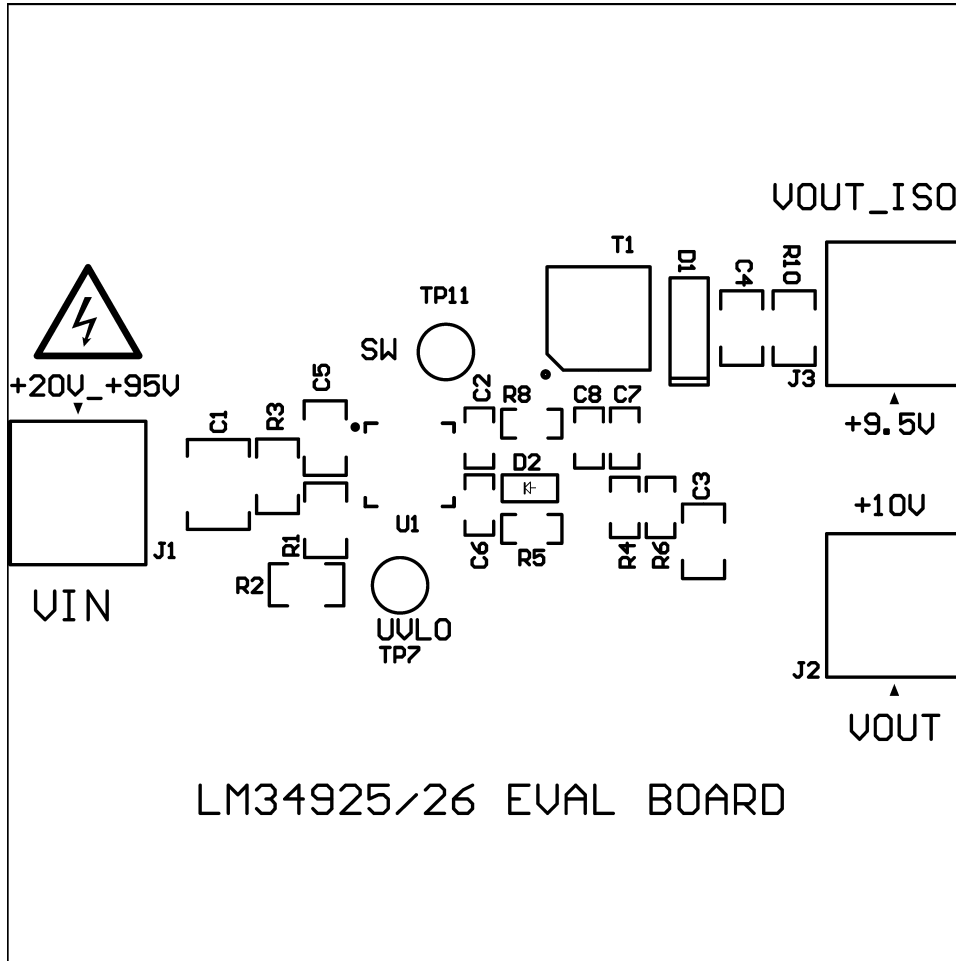


Figure 6. Board Silkscreen

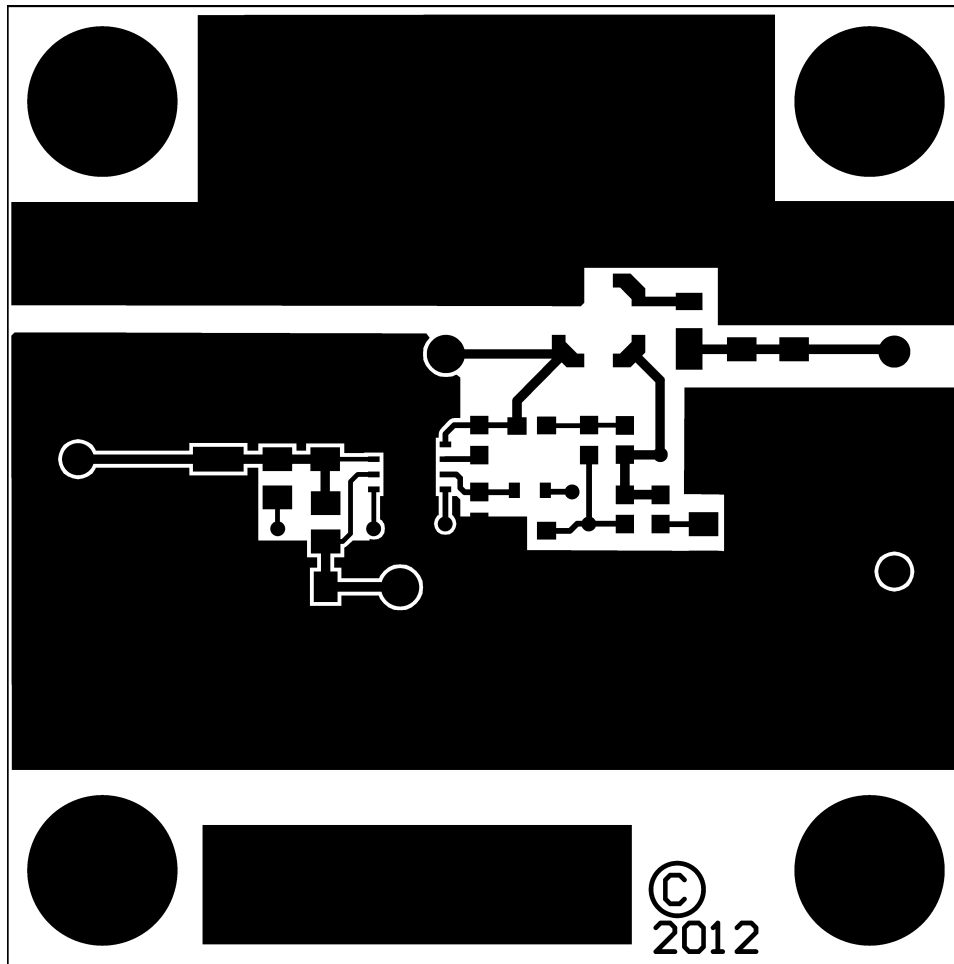


Figure 7. Board Top Layer

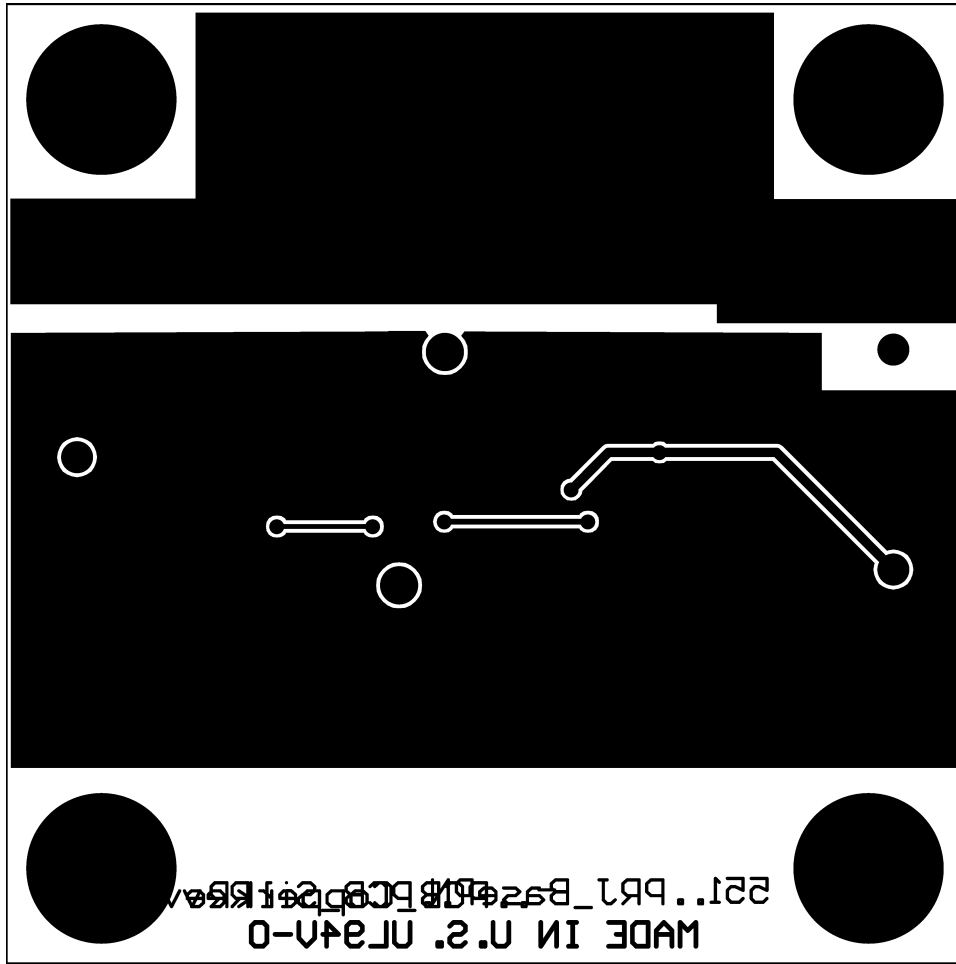


Figure 8. Board Bottom Layer

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