Using The Manual Reset On Voltage Supervisors to Debounce a Pushbutton Switch

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There are many applications that utilize a pushbutton switch to force a system reset. A typical voltage supervisor with a manual reset ($\overline{MR}$) pin is shown in Figure 1. The $\overline{MR}$ pin is typically connected to a GPIO from a MCU or directly to a pushbutton switch for forcing a reset. Issues arise when the pushbutton switch has parasitic transients as shown in Figure 2 that can cause the output to falsely reset or function improperly.

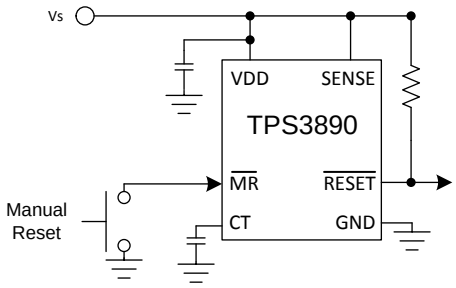

Figure 1. Pushbutton Switch Debounce Circuit Using Manual Reset on TPS3890

Normally, when a pushbutton switch is pressed or released, the electrical signal is noisy and if the output responds directly to the pushbutton switch, the noise will propagate through directly to the output. Using voltage supervisors that feature the manual reset ($\overline{MR}$) pin, the pushbutton switch can be debounced such that the first falling transition on the $\overline{MR}$ pin caused by pressing the pushbutton switch will cause the output to reset regardless of how much noise there is on the pushbutton switch. The device keeps the output in the reset condition until the pushbutton switch is released long enough so that the $\overline{MR}$ pin is inactive and thus settled for the duration of the reset delay ($t_{d(RST)}$). Once the $\overline{MR}$ pin is inactive for the reset delay set by the CT capacitor, the device will release the reset back to the inactive state. The timing diagram in Figure 2 shows the benefit of using manual reset to debounce a pushbutton switch.

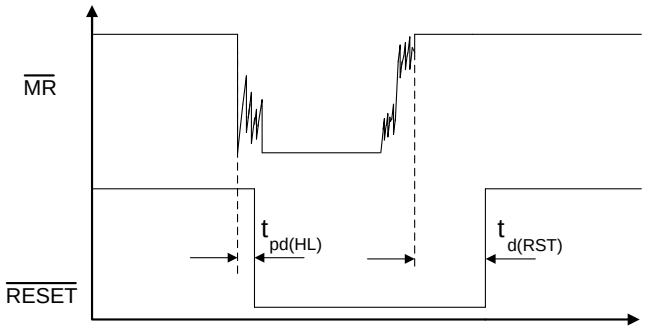

Figure 2. Timing Diagram of Manual Reset Debounce

In addition to pushbutton switch debouncing, the $\overline{MR}$ pin also includes high frequency noise filtering. Every device that has the manual reset feature has a minimum pulse width for the $\overline{MR}$ pin to be triggered. This means if a very fast high frequency pulse arrives on the $\overline{MR}$ pin, the signal will be ignored unless the duration of the pulse meets the specification required for the minimum pulse width.

Table 1 notes that the $\overline{MR}$ pin glitch immunity specification can also be defined as $\overline{MR}$ pin minimum pulse width which is an inversely related. A pulse that is ignored because it transitions too fast can also be defined as not meeting the minimum pulse width to cause a trigger.

Table 1. Alternative Device Recommendations

Device	$\overline{MR}$ Glitch Immunity	$\overline{MR}$ Pulse Width (Minimum)
TPS3890	100 ns	x
TPS3895, TPS3896, TPS3897, TPS3898	1 us	1 ns
TPS3808	x	1 ns
TPS3840	x	300 ns

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