

Using a TPSM265R1 in an Inverting Buck-Boost Topology

Alejandro Iraheta

ABSTRACT

The TPSM265R1 is a 2.8 × 3.7 mm², 100-mA rated, synchronous step-down power module that features a wide operating input range from 3 V to 65 V, and an adjustable output voltage range from 1.223 V to 15 V. The TPSM265R1 can be configured in an inverting buck-boost (IBB) topology with the output voltage inverted or negative (with respect to the input voltage). This application report demonstrates how the conventional, non-inverting evaluation board for the TPSM265R1 can be configured for an inverting application, and provides the additional level-shifter circuitry for the enable (EN) and power good (PGOOD) pins (if the feature is required).

Contents

1	Inverting Buck-Boost Topology	2
2	Design Considerations	4
3	External Components	5
4	Typical Performance	6
5	Digital Pin Configurations	7
6	Conclusion	8
7	References	8

List of Figures

1	Converting From Buck to Inverting Buck Boost Topology.....	2
2	EVM User Interface in IBB Configuration.....	2
3	Recommended Maximum Output Current for the TPSM265R1	4
4	TPSM265R1 Inverting Buck-Boost Schematic With Schottky Diode	5
5	SW Node Voltage During Start Up	5
6	Efficiency at $V_{IN} = 24\text{ V}$	6
7	Load Regulation at $V_{IN} = 24\text{ V}$	6
8	Enable Turn-On on $V_{IN} = 24\text{ V}$, $V_{OUT} = -5\text{ V}$ With 50-mA Load	6
9	Enable Turn-Off on $V_{IN} = 24\text{ V}$, $V_{OUT} = -5\text{ V}$ With 50-mA Load	6
10	Load Regulation at $V_{IN} = 24\text{ V}$, $V_{OUT} = -5\text{ V}$	6
11	Output Voltage Ripple, $V_{IN} = 24\text{ V}$, $V_{OUT} = -5\text{ V}$ With 50-mA Load	6
12	EN Pin Level Shifter	7
13	PG Pin Level-Shifter	8

List of Tables

1	Maximum Output Current Calculation for IBB TPSM265R1	3
---	--	---

Trademarks

All trademarks are the property of their respective owners.

1 Inverting Buck-Boost Topology

1.1 Concept

In a standard buck configuration, the positive output connection (V_{OUT}) is connected to the internal inductor, and the return connection is connected to the device ground (GND).

In the IBB configuration, the system ground (SYS_GND) is connected to V_{OUT} of the device, and the device return path is now the negative output voltage ($-V_{OUT}$). Therefore, the buck output is now the system ground, and the buck "ground" becomes the negative output voltage. This shift in topology allows the output voltage to be inverted (with respect to the input voltage). Figure 1 shows the connections for taking the buck regulator and converting it into an IBB.

The connection changes are detailed in the following list:

1. Reassign the buck positive output as system ground.
2. Reassign the buck regulator ground nodes as the negative output voltage node.
3. Positive input remains the same.

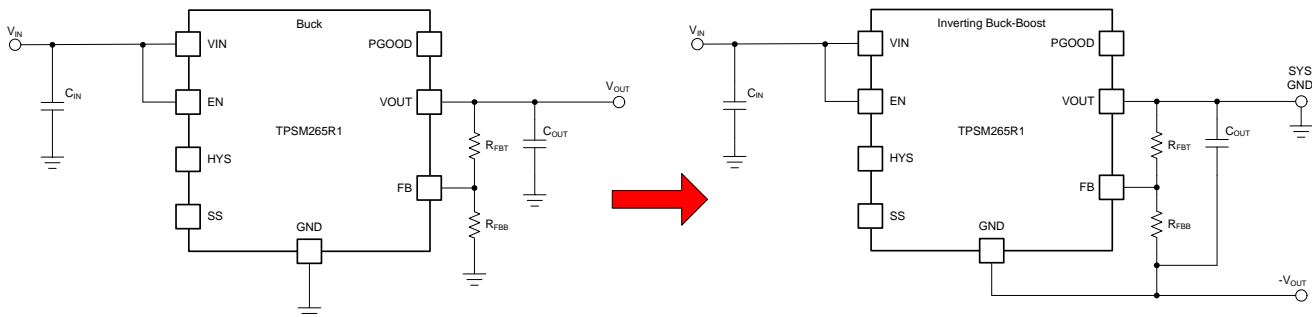


Figure 1. Converting From Buck to Inverting Buck Boost Topology

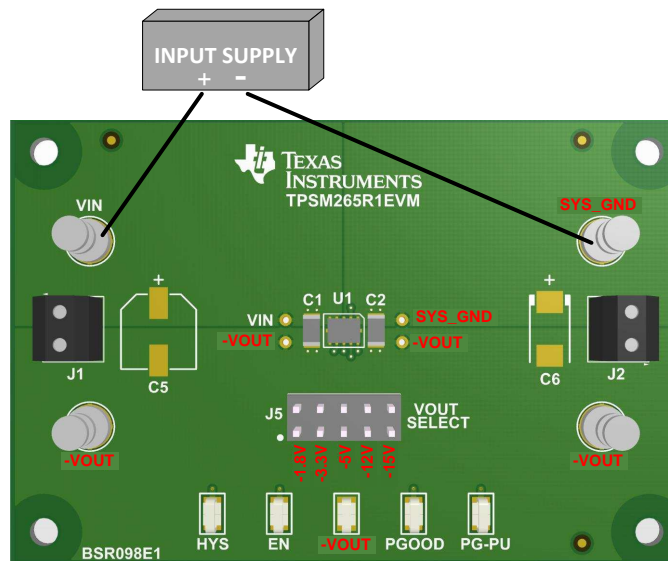


Figure 2. EVM User Interface in IBB Configuration

1.2 Output Current Calculations

The peak current limit of the converter indicates the maximum inductor current and, therefore, the maximum load current that can be supplied. In an IBB configuration, the inductor current and peak switching currents are larger than in the equivalent buck converter. Consequently, the output current capability in the IBB topology is less than the buck configuration. The maximum achievable current can be calculated using Equation 1.

$$I_{OUT}(IBB) = I_{L_MAX} \times (1 - D)$$

where

- I_{L_MAX} is the maximum-rated inductor current
 - D is the operating duty cycle
- (1)

The operating duty cycle for an inverting buck-boost converter can be calculated using Equation 2:

$$D = \frac{|V_{OUT}|}{|V_{OUT}| + \eta \times V_{IN}}$$

where

- η = Efficiency
- (2)

The efficiency term in Equation 2 adjusts the equations in this section for power conversion losses, and yields a more accurate maximum output current result. Given that the IBB configuration yields different efficiency values in regard to operating conditions, use a conservative value, or see Table 1 for typical efficiency values. Use Equation 1 to calculate the recommended maximum output current. For example, in a 24-V input voltage, -5-V output voltage system, the duty cycle is:

$$D = \frac{|-5|}{|-5| + 0.74 \times 24} = 0.220$$
(3)

The result of Equation 3 is then used to calculate the maximum achievable output current:

$$I_{OUT}(IBB) = 0.1 \times (1 - 0.220) = 78 \text{ mA}$$
(4)

Table 1 and Figure 3 provide a general idea of the maximum output current allowed from the TPSM265R1 in an inverting configuration with given typical efficiency values.

Table 1. Maximum Output Current Calculation for IBB TPSM265R1

V_{OUT} (V)	V_{IN} (V)	I_{L_MAX} (mA)	η	D	I_{OUT} (mA)
-1.8	24	100	0.60	0.011	89
-3.3	24	100	0.69	0.166	83
-5	24	100	0.74	0.220	78
-12	24	100	0.78	0.391	61
-15	24	100	0.78	0.445	56

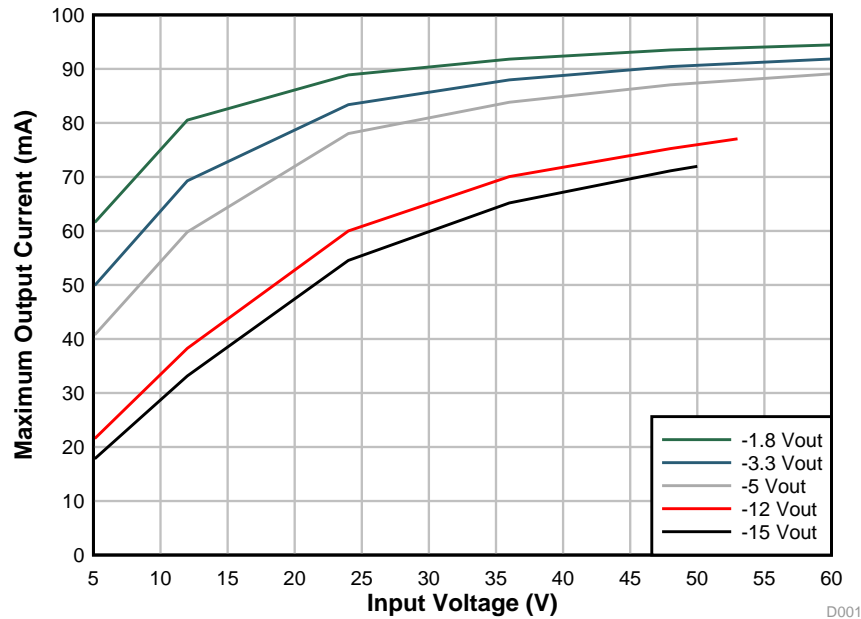


Figure 3. Recommended Maximum Output Current for the TPSM265R1

1.3 V_{IN} and V_{OUT} Range In a Inverting Configuration

When configured in an IBB topology, the voltage across the device is equal to the input voltage minus the output voltage (where the output voltage is a negative value). The voltage across the device must be kept less than the specified maximum input voltage (V_{IN_MAX}) of the device. The maximum input voltage in an IBB configuration can be calculated using Equation 5.

$$V_{IN_MAX}(IBB) = V_{IN_MAX} - |V_{OUT}|$$

where

- V_{OUT} is the negative output voltage (5)

As a result, the input voltage range in an IBB configuration is reduced. For example, the TPSM265R1 has an input voltage range of 3 V to 65 V. Therefore, for a desired output voltage of -5 V, the input voltage now has an operating range of 3 V to 60 V.

2 Design Considerations

2.1 Additional Bypass Capacitor and Schottky Diode

Use a ceramic bypass capacitor, C_{BYP} , with a minimum capacitance of 10 μ F. The voltage rating of the capacitor must be taken into consideration because it experiences stress equal to the full voltage range between V_{IN} and V_{OUT} .

To keep the system stable, a capacitor must be placed at the input power supply to help dampen the high-frequency noise that can couple onto the circuit. An electrolytic capacitor with moderate ESR helps dampen any input supply ringing caused by long power leads. When using the TPSM265R1EVM, a C_{BULK} capacitor must be added across V_{IN} and SYS_GND .

The inclusion of the bypass capacitor introduces an AC path from V_{IN} to V_{OUT} , and may worsen the transient response. When V_{IN} is applied to the circuit, this dV/dt across C_{BYP} creates a current that must return to ground to complete the loop. This current may flow through the internal low-side body diode of the MOSFET, and the inductor, to return to ground. In this case, it is recommended to have a Schottky diode between $-V_{OUT}$ and SYS_GND . If large-line transients are expected, increase the output capacitance to keep the output voltage within acceptable levels.

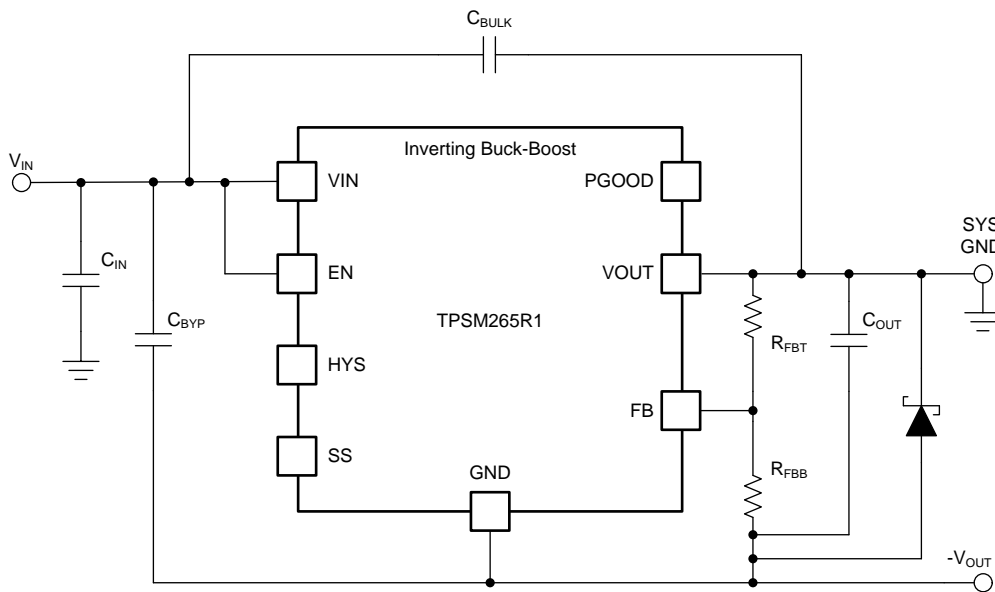


Figure 4. TPSM265R1 Inverting Buck-Boost Schematic With Schottky Diode

2.2 Start-up Behavior and Switching Node Consideration

The voltage on the switch node changes from V_{IN} to V_{OUT} in an inverting topology, instead of V_{IN} to GND as in a buck topology. When the high-side MOSFET turns on, the SW node detects the input voltage. When the low-side MOSFET turns on, the SW node detects the device return, which is the output voltage. During start up, V_{IN} rises to achieve the desired input voltage. Then, after the EN pin voltage exceeds its threshold level and V_{IN} exceeds its UVLO threshold, V_{OUT} starts ramping down. As V_{OUT} continues to ramp down, the SW low-level node follows it down. Figure 5 shows the resulting normal and smooth output voltage start up.

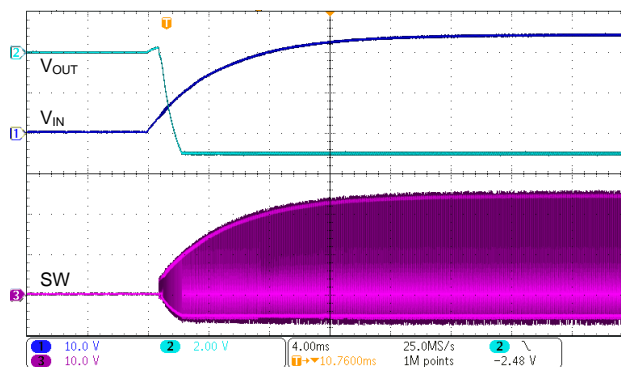


Figure 5. SW Node Voltage During Start Up

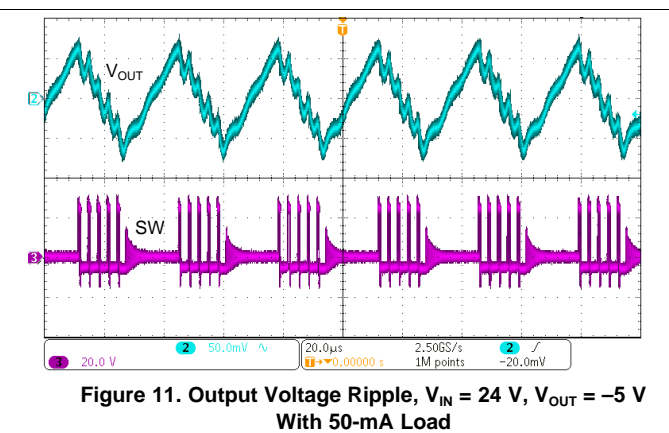
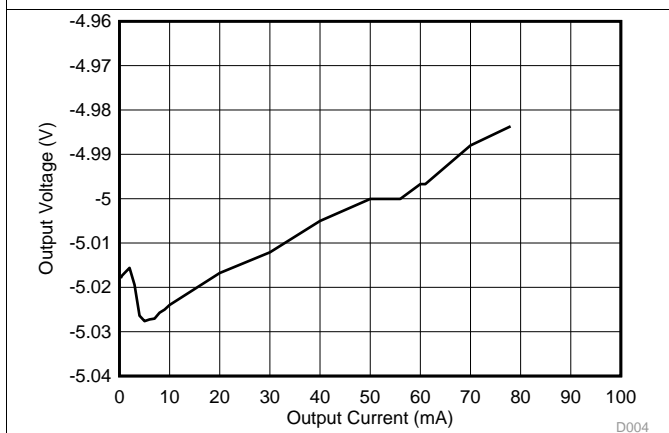
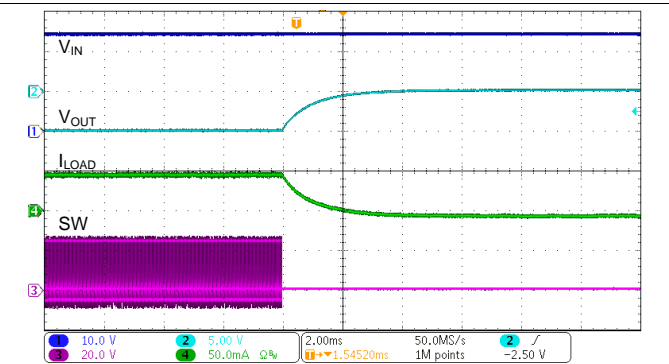
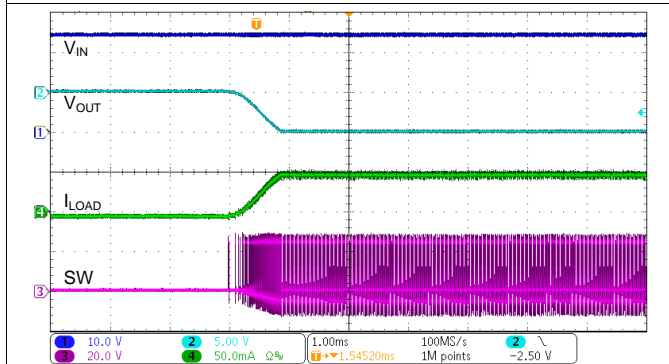
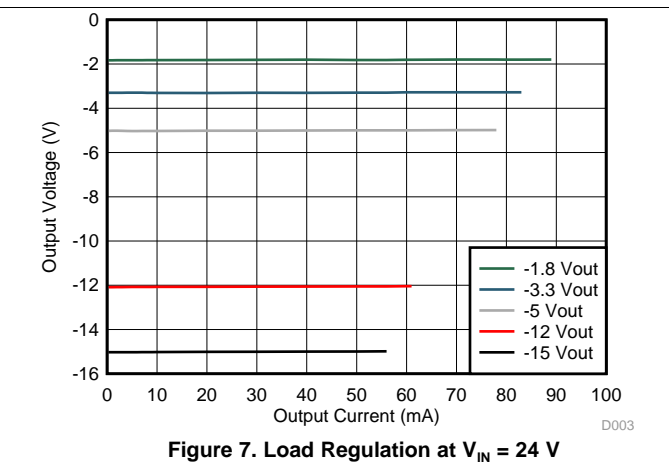
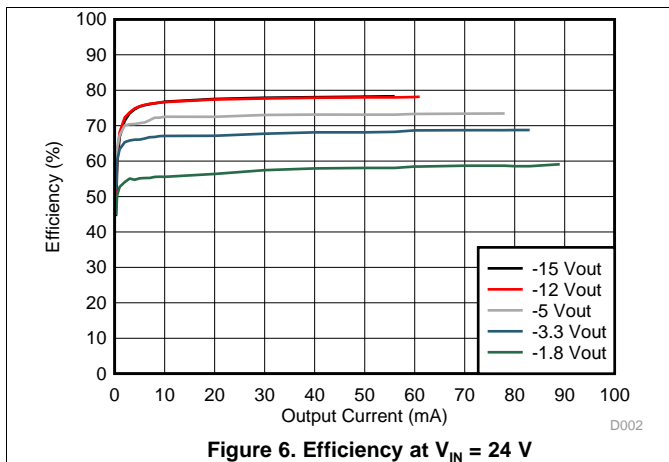
3 External Components

The TPSM265R1 power module integrates power MOSFETs and a shielded inductor. As a result, this application only requires as few as four external components. Performing a load-transient test and frequency sweep is recommended to evaluate stability.

3.1 Capacitor Selection

Ceramic capacitors with low equivalent series resistance (ESR) are recommended to achieve low output-voltage ripple. X5R or X7R-type dielectrics are recommended for the stable capacitance versus temperature characteristics and DC bias. The higher the DC voltage applied to the ceramic capacitor, the lower the capacitance is. Use a minimum of 1- μF capacitance for both C_{BYP} and C_{IN} . Making this capacitor value too large can prevent proper start-up operations.

4 Typical Performance



5 Digital Pin Configurations

5.1 Enable Pin (EN)

In an IBB configuration, because the EN pin is referenced to V_{OUT} instead of 0 V, the EN voltage thresholds are affected. In a buck configuration, the specified typical threshold voltage for the EN pin, with respect to the return path of the IC, is considered high at 1.2 V, and low at 1.14 V. In the inverting buck-boost configuration, however, V_{OUT} is the reference. Therefore, the device is further pushed into an enabled state. The high EN threshold remains the same, but the low threshold is determined by $1.14\text{ V} + V_{OUT}$. For example, if $V_{OUT} = -5\text{ V}$, V_{EN} is high for voltages above 1.2 V, and low for voltages below -3.86 V .

This behavior can cause difficulties enabling or disabling the device. The level shifter alleviates any problems associated with the offset EN threshold voltages by eliminating the need for negative EN signals.

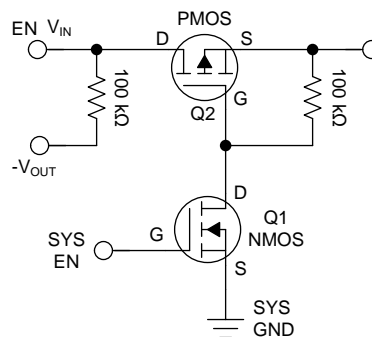


Figure 12. EN Pin Level Shifter

The positive signal (SYS_EN) that originally drove EN is instead tied to the gate of Q1 (SYS_EN). When Q1 is off (SYS_EN is grounded), Q2 detects 0 V across the V_{GS} , and also remains off. In this state, the EN pin detects V_{OUT} , which is below the low-level threshold, and disables the device.

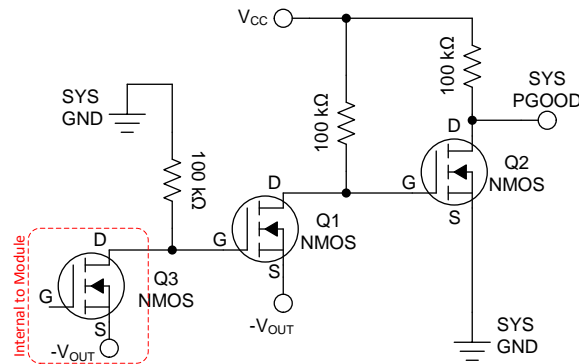
When SYS_EN provides enough positive voltage to turn Q1 on (minimum V_{GS} as specified in the MOSFET data sheet), the Q2 gate is pulled low through Q1. This drives the V_{GS} of Q2 negative, and turns Q2 on. As a consequence, V_{IN} ties to EN through Q2, and the pin is above the high-level threshold, which causes the device to turn on. Ensure that the V_{GD} of Q2 remains within the MOSFET ratings during both enabled and disabled states. Also ensure that V_{GS} and V_{DS} ratings are not exceeded. Failing to adhere to these constraints can result in damaged MOSFETs.

The SYS_EN signal activates the enable circuit, and the G/D NODE signal represents the shared node between Q1 and Q2. The EN signal is the circuit output, and goes from V_{IN} to $-V_{OUT}$, therefore properly enabling and disabling the device.

5.2 Power-Good Pin (PGOOD)

The TPSM265R1 has a built-in power-good (PGOOD) function to indicate whether the output voltage has reached the appropriate level or not. The PGOOD pin is an open-drain output that requires a pull-up resistor. Because V_{OUT} is the return path of the IC in this configuration, the PGOOD pin is referenced to V_{OUT} instead of ground. This means that the device pulls PGOOD to V_{OUT} when it is low.

This behavior can cause difficulties in reading the state of the PGOOD pin because, in some applications, the IC detecting the polarity of the PGOOD pin may not be able to withstand negative voltages. The level-shifter circuit alleviates any difficulties associated with the offset PGOOD pin voltages by eliminating the negative output signals of the PGOOD pin. If the PGOOD pin functionality is not needed, it can be left floating, or connected to V_{OUT} , without this circuit. Note that to avoid violating the absolute maximum rating of the PGOOD pin, it must not be driven more than 12 V above the negative output voltage (IC return).


Figure 13. PG Pin Level-Shifter

Inside these devices, the PGOOD pin is connected to an N-channel MOSFET (Q3). By tying the PGOOD pin to the gate of Q1, when the PGOOD pin is pulled low, Q1 is off and Q2 is on because the V_{GS} detects V_{CC} . SYS_PGOOD is then pulled to ground.

When Q3 turns off, the gate of Q1 is pulled to ground, which potentially turns it on. This pulls the gate of Q2 below ground, which turns it off. SYS_PGOOD is then pulled up to the V_{CC} voltage. Note that the V_{CC} voltage must be at an appropriate logic level for the circuitry connected to the SYS_PGOOD net.

Figure 13 illustrates this PGOOD pin level-shifter sequence. The PGOOD signal activates the PGOOD pin level-shifter circuit, and the G/D Node signal represents the shared node between Q1 and Q2. This circuit was tested with a V_{CC} of 1.8 V, and FemtoFET CSD15830F3. The SYS_PGOOD net is the output of the circuit that transitions between ground and 1.8 V, and is easily read by a separate device.

6 Conclusion

The TPSM265R1 step-down power module can be configured in an IBB topology to generate a negative output voltage by switching the output and ground connection. Converting an original buck topology into an IBB topology reduces the input voltage range and maximum output current. The input voltage range is reduced because the device now has a reference point set to the negative output voltage, rather than ground. Additionally, the inductor peak current is much higher, which effectively lowers the recommended operating maximum output current range. If EN and PGOOD pin usage is required, additional level-shifting circuitry is required to invert the negative output signal.

7 References

The following documents are available for download from TI.com:

1. Texas Instruments, [TPSM265R1 65-V Input, 100-mA Power Module with Ultra-Low \$I_Q\$ Data Sheet](#)
2. Texas Instruments, [TPSM265R1EVM 3-V to 65-V Input Voltage 100-mA Output Current User's Guide](#)
3. Texas Instruments, [Basic Calculation of an Inverting Buck-Boost Power Stage Application Report](#)
4. Texas Instruments, [Creating an Inverting Power Supply Using a Synchronous Step-Down Regulator Application Report](#)
5. Texas Instruments, [Using a buck converter in an inverting buck-boost topology Technical Brief](#)
6. Texas Instruments, [Working with inverting buck-boost converters Application Report](#)

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2022, Texas Instruments Incorporated