Radiation Report

TPS7H4010-SEP Total Ionizing Dose (TID) Radiation Report

ABSTRACT

This report discusses the results of the Total Ionizing Dose (TID) testing for the Texas Instruments 3.5V to 32V, 6A synchronous step-down voltage converter TPS7H4010-SEP. The study was done to determine TID effects under low dose rate (LDR) and high dose rate (HDR) up to 30krad(Si). The results show that all samples passed within the specified limits up to 30krad(Si) and Radiation Lot Acceptance Testing (RLAT) will be performed using 22 units at 30krad(Si) for future wafer lots.

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Trademarks

1 Device Information

1.1 Product Description

The TPS7H4010-SEP is a 3.5V to 32V, 6A synchronous step-down voltage converter capable of driving up to 6A of load current. The TPS7H4010-SEP provides exceptional efficiency and output accuracy in a very small solution size.

1.2 Device Details

Table 1-1 lists the device information used in the TID HDR and LDR characterization.

Table 1-1. Device and Exposure Details

TID HDR and LDR Details: 20krad(Si) and 30krad(Si)	
Package	30-pin WQFN (RNP)
Quantity Tested	HDR and LDR: 22 bias and 5 unbiased units at 20krad(Si) levels; 5 bias and 5 unbiased units at 30krad(Si) levels
HDR and LDR Radiation Facility	Radiation Test Solutions, Colorado Springs, Colorado
HDR and LDR Dose Level	20krad(Si), 30krad(Si)
HDR Dose Rate	59.16rad(Si)/s ionizing radiation with increments
LDR Dose Rate	10mrad(Si)/s ionizing radiation with increments
HDR Radiation Source	Gamma rays provided by JLSA 81-24 Co60 source. Dosimetry performed by Air Ionization Chamber (AIC) traceable to NIST.
LDR Radiation Source	Gamma rays provided by JLSA 81-22 or JLSA 81-23 Co60 LDR source. Dosimetry performed by AIC traceable to NIST.
Irradiation and Test Temperature	Ambient, room temperature controlled to 24°C±6°C per MIL-STD-883 and MIL-STD-750.

Figure 1-1. TPS7H4010-SEP Devices Used in Exposure

2 Total Dose Test Setup

2.1 Test Overview

The TPS7H4010-SEP was tested according to MIL-STD-883, Test Method 1019.9. For this testing, Conditions A and D were used. For this test, the product was irradiated up to the target radiation level, and then put through full electrical parametric testing on the production Automated Test Equipment (ATE). All devices remained functional passing all parametric test limits.

2.2 Test Description and Facilities

The TPS7H4010-SEP HDR and LDR exposures were performed on biased and unbiased devices in gamma rays provided by JLSA 81-24 Co60 source and by JLSA 81-22 or JLSA 81-23 Co60 LDR source, respectively, at *Radiation Test Solutions, Inc.* facility in Colorado Springs, Colorado. Dosimetry performed by Air Ionization Chamber (AIC) traceable to NIST. Radiation Test Solutions's dosimetry has been audited by DLA. After exposure, the devices were packed in dry ice (per MIL-STD-883 Method 1019.9 section 3.10) and returned to TI Dallas for a full post-radiation electrical evaluation using Texas Instruments Automated Test Equipment (ATE). ATE guard band test limits are set within VID electrical limits to ensure robust Cpk and test error margin based on qualification and characterization data. Post-radiation measurements were taken on the same test setup where initial, pre-exposure testing done, within 30 minutes of removing the devices from the dry ice container. The devices were allowed to reach room temperature prior to electrical post-radiation measurements.

2.3 Test Setup Details

The devices under HDR and LDR exposure were tested in two conditions, biased and unbiased, as described in the following sections.

2.3.1 Unbiased

For the unbiased HDR and LDR conditions, the exposure was performed with all pins grounded.

2.3.2 Biased

Figure 2-1 shows the diagram for HDR and LDR exposure with biased condition.

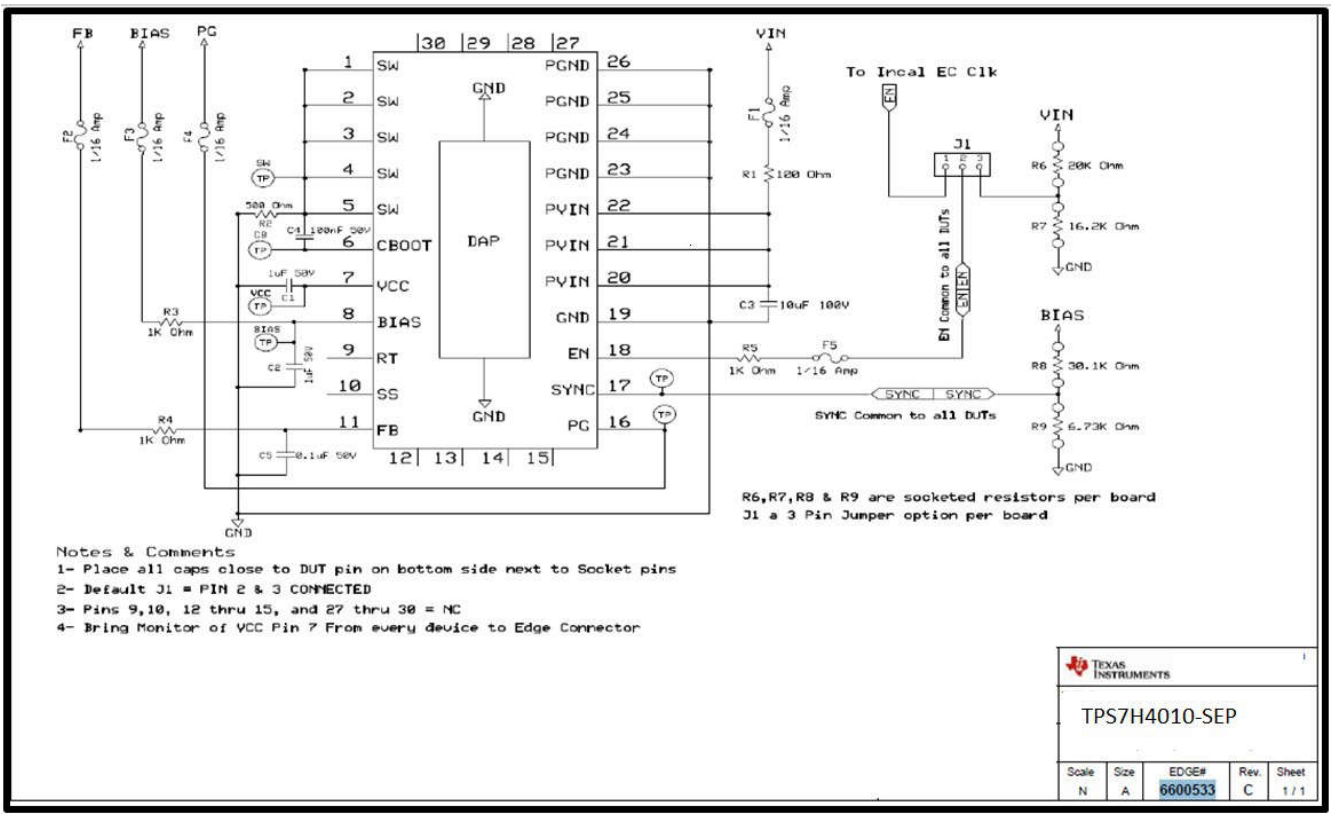

Figure 2-1. Bias Diagram Used in TID Exposure

2.4 Test Configuration and Condition

HDR and LDR devices were stressed at 20krad(Si) and 30krad(Si) for biased and unbiased conditions.

Table 2-1. HDR ≥ 50–300rad(Si)/s Biased Device Information (HDR)

Total Samples: 27	
Exposure Levels:	
20krad(Si) (22 samples)	30krad(Si) (5 samples)
61, 62, 63, 64, 65, 67, 68, 69, 70, 71, 72, 73, 74, 75, 76, 77, 78, 79, 80, 81, 82, 83	89, 90, 91, 92, 93

Table 2-2. HDR ≥ 50–300rad(Si)/s Unbiased Device Information (HDR)

Total Samples: 10	
Exposure Levels:	
20krad(Si) (5 samples)	30krad(Si) (5 samples)
84, 85, 86, 87, 88	94, 95, 96, 97, 98

Table 2-3. LDR ≤ 10 mrad(Si)/s Biased Device Information (LDR)

Total Samples: 27	
Exposure Levels:	
20krad(Si) (22 samples)	30krad(Si) (5 samples)
6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27	33, 34, 35, 36, 37

Table 2-4. LDR ≤ 10 mrad(Si)/s Unbiased Device Information (LDR)

Total Samples: 10	
Exposure Levels:	
20krad(Si) (5 samples)	30krad(Si) (5 samples)
1, 2, 3, 4, 5	28, 29, 30, 31, 32

3 TID Characterization Test Results

3.1 TID Characterization Summary Results

The parametric data for the TPS7H4010-SEP passes up to 30krad(Si) HDR and LDR TID. The drift of VID electrical parameters through HDR and LDR were within the pre-radiation limits.

Overall, the TPS7H4010-SEP showed a strong degree of hardness to HDR and LDR TID irradiation up to 30krad(Si) for both biased and unbiased exposure conditions. The measurements taken post-irradiation for each sample set showed a marginal shift for most parameters at each dose level for both biased and unbiased. The parameters that did show a greater degree of change between pre- and post-irradiation were still within the data sheet electrical specifications (see Section 3.2 for Specification Compliance Matrix).

Please see Appendix A for HDR report up to 30krad(Si).

Please see Appendix B for LDR report up to 30krad(Si).

3.2 Specification Compliance Matrix

The TPS7H4010-SEP Specification Compliance Matrix is comprised of electrical, timing, and switching characteristics lists as shown in the following tables.

Table 3-1. Electrical Characteristics

PARAMETER		TEST CONDITIONS	TPS7H4010-SEP Data Sheet				Test#
			MIN	TYP	MAX	UNIT	
SUPPLY VOLTAGE (PVIN PINS)							
PVIN	Operating input voltage		3.5		32	V	
I_{SD}	Shutdown quiescent current; measured at PVIN pin(1)	V_{EN} = AGND, T_J = 25°C		0.8	10	µA	2.1, 2.2, 2.3, 2.4
I_{Q_NONSW}	Operating quiescent current from PVIN (non-switching)	V_{EN} = 2V, V_{FB} = 1.5V, V_{BIAS} = 3.3V external		0.6	12	µA	25.5
ENABLE (EN PIN)							
$V_{EN\_VCC\_H}$	Enable input high-level for VCC output	V_{EN} rising			1.15	V	30.1
$V_{EN\_VCC\_L}$	Enable input low-level for VCC output	V_{EN} falling	0.3			V	30.2
$V_{EN\_VOUT\_H}$	Enable input high-level for VOUT	V_{EN} rising	1.14	1.196	1.25	V	30.4
$V_{EN\_VOUT\_HYS}$	Enable input hysteresis for VOUT	V_{EN} falling hysteresis		100		mV	30.6
I_{LKG_EN}	Enable input leakage current	V_{EN} = 2V		1.4	200	nA	25.3
INTERNAL LDO (VCC PIN, BIAS PIN)							
VCC	Internal VCC voltage	PWM operation		3.27		V	12.6, 12.7, 12.8
		PFM operation		3.1		V	29.4, 29.5, 29.6
V_{CC_UVLO}	Internal VCC undervoltage lockout	VCC rising	2.96	3.14	3.27	V	29.2
		VCC falling hysteresis		605		mV	29.3
V_{BIAS_ON}	Input changeover	VBIAS rising		3.09	3.25	V	29.9
		VBIAS falling hysteresis		63		mV	29.10
I_{BIAS_NONSW}	Operating quiescent current from external VBIAS (non-switching)	VEN = 2V, VFB = 1.5V, VBIAS = 3.3V external		21	50	µA	29.16
VOLTAGE REFERENCE (FB PIN)							
V_{FB}	Feedback voltage	PWM mode	0.987	1.006	1.017	V	28.1, 28.3, 28.5
I_{LKG_FB}	Input leakage current at FB pin	VFB = 1V		0.2	60	nA	25.4
HIGH SIDE DRIVER (CBOOT PIN)							
V_{CBOOT_UVLO}	CBOOT - SW undervoltage lockout		1.6	2.2	2.7	V	38.2
CURRENT LIMITS AND HICCUP							
I_{HS_LIMIT}	Short-circuit, high-side current limit(2)		7.4	8.7	9.85	A	20.5
I_{LS_LIMIT}	Low-side current limit(2)		5.8	6.6	7.25	A	22.5
I_{NEG_LIMIT}	Negative current limit			–6		A	22.7

Table 3-1. Electrical Characteristics (continued)

PARAMETER		TEST CONDITIONS	TPS7H4010-SEP Data Sheet				Test#
			MIN	TYP	MAX	UNIT	
V_{HICCUP}	Hiccup threshold on FB pin		0.36	0.4	0.44	V	37.17, 37.18
I_{L_ZC}	Zero cross-current limit			0.06		A	22.6
SOFT START (SS/TRK PIN)							
I_{SSC}	Soft-start charge current		1.8	2	2.2	µA	25.6, 32.4
R_{SSD}	Soft-start discharge resistance	UVLO, TSD, OCP, or EN = AGND		1		kΩ	32.3
POWER GOOD (PGOOD PIN) and OVERVOLTAGE PROTECTION							
V_{PGOOD_OV}	Power-good overvoltage threshold	% of FB voltage	106%	110%	113%		37.5,37.6
V_{PGOOD_UV}	Power-good undervoltage threshold	% of FB voltage	86%	90%	93%		37.8, 37.9
V_{PGOOD_HYS}	Power-good hysteresis	% of FB voltage		1.2%			37.7, 37.10
V_{PGOOD_VALID}	Minimum input voltage for proper PGOOD function	50µA pullup to PGOOD pin, V_{EN} = AGND, T_J = 25℃		1.3	2	V	37.1
R_{PGOOD}	Power-good ON-resistance	VEN = 2.5V		40	100	Ω	37.2, 37.4
		VEN = AGND		30	90		37.3
MOSFETS							
$R_{DS\_ON\_HS}$ (3)	High-side MOSFET ON-resistance	IOUT = 1A, VBIAS = VOUT = 3.3V		53	90	mΩ	18.1
$R_{DS\_ON\_LS}$ (3)	Low-side MOSFET ON-resistance	IOUT = 1A, VBIAS = VOUT = 3.3V		31	55	mΩ	18.2

(1) Shutdown current includes leakage current of the switching transistors.
(2) This current limit was measured as the internal comparator trip point. Due to inherent delays in the current limit comparator and drivers, the peak current limit measured in closed loop with faster slew rate will be larger, and valley current limit will be lower.
(3) Measured at pins.

Table 3-2. Timing Characteristics

PARAMETER		TEST CONDITIONS	TPS7H4010-SEP Data Sheet				Test #
			MIN	TYP	MAX	UNIT	
CURRENT LIMITS AND HICCUP							
t_{OC}	Overcurrent hiccup retry delay time			46		ms	32.2
SOFT START (SS/TRK PIN)							
t_{SS}	Internal soft-start time	CSS = OPEN, from EN rising edge to PGOOD rising edge	3.5	6.3		ms	32.1, 32.5
POWER GOOD (PGOOD PIN) and OVERVOLTAGE PROTECTION							
t_{PGOOD_RISE}	PGOOD rising edge deglitch delay		80	140	200	µs	37.15
t_{PGOOD_FALL}	PGOOD falling edge deglitch delay		80	140	200	µs	37.16

Table 3-3. Switching Characteristics

PARAMETER		TEST CONDITIONS	TPS7H4010-SEP Data Sheet				Test #
			MIN	TYP	MAX	UNIT	
PWM LIMITS (SW PINS)							
$t_{ON\text{-}MIN}$	Minimum switch on-time			60	82	ns	36.2
$t_{OFF\text{-}MIN}$	Minimum switch off-time			70	120	ns	36.5
$t_{ON\text{-}MAX}$	Maximum switch on-time	HS timeout in dropout	3	6	9	µs	36.7
OSCILLATOR (RT and SYNC PINS)							
f_{OSC}	Internal oscillator frequency	RT = Open	440	500	560	kHz	36.1
f_{ADJ}	Minimum adjustable frequency by RT or SYNC	RT = 115kΩ, 0.1%	315	350	385	kHz	36.9
	Maximum adjustable frequency by RT or SYNC	RT = 17.4kΩ, 0.1%	1980	2200	2420		36.3, 36.4
V_{SYNC_HIGH}	Sync input high-level threshold				2	V	34.1
V_{SYNC_LOW}	Sync input low-level threshold		0.4			V	34.2
V_{MODE_HIGH}	Mode input high-level threshold for FPWM			0.42		V	34.7
V_{MODE_LOW}	Mode input low-level threshold for AUTO mode			0.4		V	34.8
t_{SYNC_MIN}	Sync input minimum ON and OFF time			80		ns	34.5, 34.6

4 Applicable and Reference Documents

4.1 Applicable Documents

- *TPS7H4010-SEP Radiation Hardened 3.5-V to 32-V, 6-A Synchronous Step-Down Voltage Converter in Space Enhanced Plastic* data sheet
- *TPS7H4010-SEP Production Flow and Reliability Report*
- *TPS7H4010-SEP EVM User's Guide*

4.2 Reference Documents

Texas Instruments total ionizing dose radiation (total dose) test procedure follows the standards put forth in MIL-STD-883 TM 1019. The document can be found at the DLA website.

5 Revision History

Changes from Revision * (November 2020) to Revision A (June 2024)	Page
• Updated the production flow from 20krad RLAT to 30krad RLAT and added RLAT statement	1

A Appendix A: HDR TID Report

This appendix contains the HDR TID report data.

B Appendix B: LDR TID Report

This appendix contains the LDR TID report data.

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