LP87702-Q1 Technical Reference Manual

This document provides the values for the OTP register bits of following part numbers: LP87702DRHBRQ1 and LP87702KRHBRQ1.

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Trademarks

1 Introduction

This Technical Reference Manual can be used as a reference for the LP87702-Q1 default register bits after OTP memory download. This Technical Reference Manual does not provide information about the electrical characteristics, external components, package, or the functionality of the device. For this information and the full register map, refer to the *LP87702-Q1 Dual Buck Converter and 5-V Boost With Diagnostic Functions* data sheet

Main OTP settings for power rails are listed in Table 1. Full list of register bits loaded from OTP memory is shown in Section 2.

Table 1. Main OTP Settings for Power Rails

	DESCRIPTION	BIT NAME	LP87702D	LP87702K
Device Identification	OTP configuration	OTP_ID	2D	23
	Revision for OTP_ID	OTP_REV	2	0
BUCK0	Output voltage	BUCK0_VSET	1.8 V	1.8 V
	Enable, EN-pin or I^2C register	BUCK0_EN_PIN_CTRL, BUCK0_EN	EN1	EN1
	Force PWM	BUCK0_FPWM	Yes	Yes
	Peak current limit	BUCK0_ILIM	4 A	4 A
	Maximum load current	N/A	3 A	3 A
BUCK1	Output voltage	BUCK1_VSET	1.24 V	1.01 V
	Enable, EN-pin or I^2C register	BUCK1_EN_PIN_CTRL, BUCK1_EN	EN1	EN1
	Force PWM	BUCK1_FPWM	Yes	Yes
	Peak current limit	BUCK1_ILIM	4.5 A	4.5 A
	Maximum load current	N/A	3.5 A	3.5 A
BOOST	Mode, boost or bypass	Mode control bit is not in customer register space	Boost	Boost
	Output voltage	BOOST_VSET	5 V	5 V
	Enable, EN-pin or I^2C register	BOOST_EN_PIN_CTRL, BOOST_EN	EN1	EN1
	Peak current limit	BOOST_ILIM0, BOOST_ILIM1	1.4 A	1.4 A
	Maximum load current	N/A	0.6 A	0.6 A

Table 1. Main OTP Settings for Power Rails (continued)

	DESCRIPTION	BIT NAME	LP87702D	LP87702K
VANA	VANA over-voltage threshold	VANA_OVP_SEL (selection bit is not in customer register space)	4.3 V rising	4.3 V rising

There are a few important connections to ensure the LP87702D-Q1 and LP87702K-Q1 is configured correctly, each of which are described in this section. Good examples of how to connect the radar devices to the LP87702D-Q1 and LP87702K-Q1 PMIC are shown in Figure 1 and Figure 2.

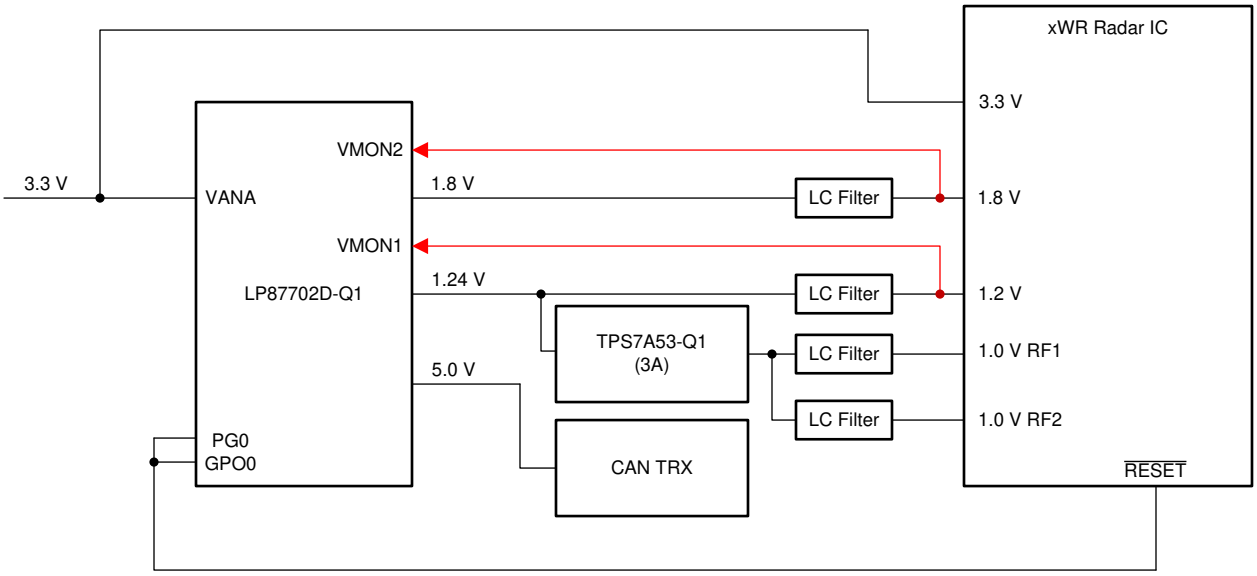

Figure 1. Typical Connection to LP87702D-Q1

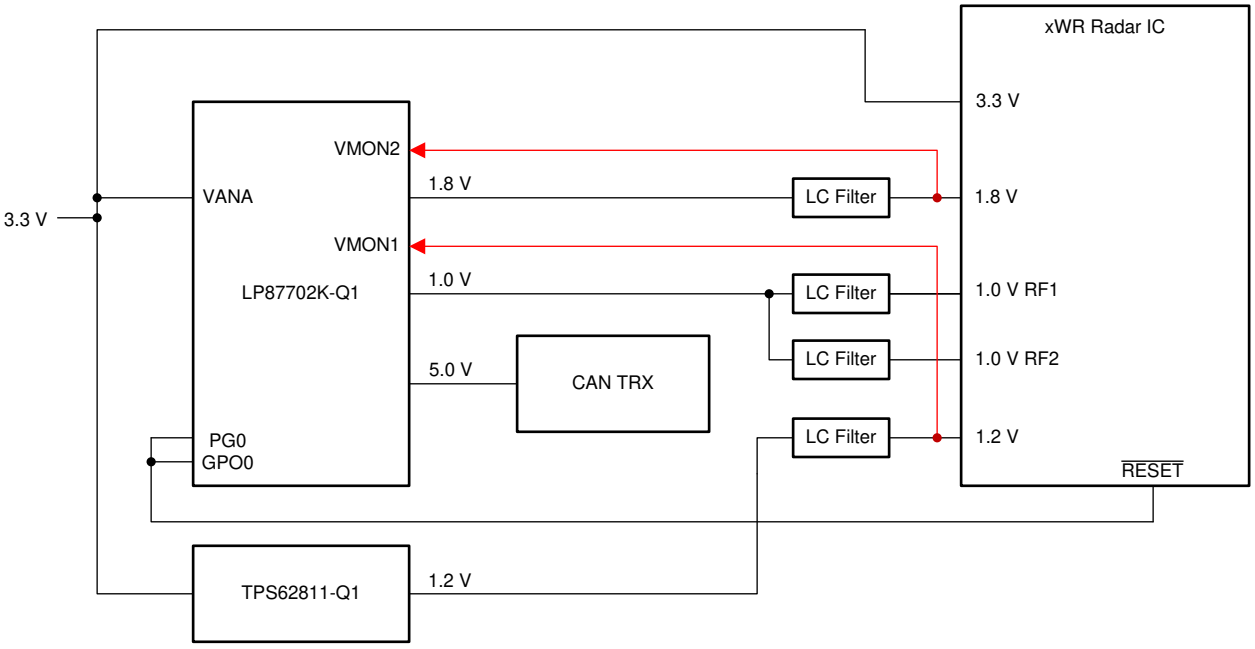

Figure 2. Typical Connection to LP87702K-Q1

2 Register Bits Loaded From OTP Memory

LP87702-Q1 device includes OTP memory. Table 2 lists the register bits that are loaded from the memory during device startup.

Table 2. Summary of Registers Bits

Address	Register Name	Bit	LP87702D	LP87702K
0x00	DEV_REV	DEVICE_ID[2:0]	0x0	0x0
0x01	OTP_CODE	OTP_ID[5:0]	0x2D	0x23
0x01	OTP_CODE	OTP_REV[1:0]	2	0
BUCK CONTROL				
0x02	BUCK0_CTRL_1	BUCK0_FPWM_MP	Auto	Auto
0x02	BUCK0_CTRL_1	BUCK0_FPWM	PWM	PWM
0x02	BUCK0_CTRL_1	BUCK0_EN_PIN_CTRL[1:0]	BUCK0_EN bit *and* EN1 pin	BUCK0_EN bit *and* EN1 pin
0x02	BUCK0_CTRL_1	BUCK0_EN	Enabled	Enabled
0x03	BUCK0_CTRL_2	BUCK0_ILIM[2:0]	4.0 A	4.0 A
0x03	BUCK0_CTRL_2	BUCK0_SLEW_RATE[2:0]	3.8 mV/µs	1.9 mV/µs
0x04	BUCK1_CTRL_1	BUCK1_FPWM	PWM	PWM
0x04	BUCK1_CTRL_1	BUCK1_EN_PIN_CTRL[1:0]	BUCK1_EN bit *and* EN1 pin	BUCK1_EN bit *and* EN1 pin
0x04	BUCK1_CTRL_1	BUCK1_EN	Enabled	Enabled
0x05	BUCK1_CTRL_2	BUCK1_ILIM[2:0]	4.5 A	4.5 A
0x05	BUCK1_CTRL_2	BUCK1_SLEW_RATE[2:0]	3.8 mV/µs	1.9 mV/µs
0x06	BUCK0_VOUT	BUCK0_VSET[7:0]	1800 mV	1800 mV
0x07	BUCK1_VOUT	BUCK1_VSET[7:0]	1240 mV	1010 mV
BOOST CONTROL				
0x08	BOOST_CTRL	BOOST_VSET[1:0]	5.0 V	5.0 V
0x08	BOOST_CTRL	BOOST_FPWM	PWM	PWM
0x08	BOOST_CTRL	BOOST_EN_PIN_CTRL[1:0]	BOOST_EN bit *and* EN1 pin	BOOST_EN bit *and* EN1 pin
0x08	BOOST_CTRL	BOOST_EN	Enabled	Enabled
STARTUP AND SHUTDOWN DELAYS				
0x09	BUCK0_DELAY	BUCK0_SHUTDOWN_DELAY[3:0]	3.0 ms	3.0 ms
0x09	BUCK0_DELAY	BUCK0_STARTUP_DELAY[3:0]	2.0 ms	2.0 ms
0x0A	BUCK1_DELAY	BUCK1_SHUTDOWN_DELAY[3:0]	2.0 ms	2.0 ms
0x0A	BUCK1_DELAY	BUCK1_STARTUP_DELAY[3:0]	3.0 ms	3.0 ms
0x0B	BOOST_DELAY	BOOST_SHUTDOWN_DELAY[3:0]	1.0 ms	1.0 ms
0x0B	BOOST_DELAY	BOOST_STARTUP_DELAY[3:0]	4.0 ms	4.0 ms
0x0C	GPO0_DELAY	GPO0_SHUTDOWN_DELAY[3:0]	0.0 ms	0.0 ms
0x0C	GPO0_DELAY	GPO0_STARTUP_DELAY[3:0]	5.0 ms	5.0 ms
0x0D	GPO1_DELAY	GPO1_SHUTDOWN_DELAY[3:0]	0.0 ms	0.0 ms
0x0D	GPO1_DELAY	GPO1_STARTUP_DELAY[3:0]	0.0 ms	0.0 ms
0x0E	GPO2_DELAY	GPO2_SHUTDOWN_DELAY[3:0]	0.0 ms	0.0 ms
0x0E	GPO2_DELAY	GPO2_STARTUP_DELAY[3:0]	0.0 ms	0.0 ms
GPO				
0x0F	GPO_CONTROL_1	GPO1_PG1_OD	OD	OD
0x0F	GPO_CONTROL_1	GPO1_EN_PIN_CTRL[1:0]	GPO1_OUT bit	GPO1_OUT bit
0x0F	GPO_CONTROL_1	GPO1_OUT	Low	Low
0x0F	GPO_CONTROL_1	GPO0_OD	OD	OD
0x0F	GPO_CONTROL_1	GPO0_EN_PIN_CTRL[1:0]	GPO0_OUT bit *and* EN1 pin	GPO0_OUT bit *and* EN1 pin
0x0F	GPO_CONTROL_1	GPO0_OUT	High	High
0x10	GPO_CONTROL_2	GPO2_SEL	CLKIN	CLKIN
0x10	GPO_CONTROL_2	GPO1_SEL	PG1	PG1
0x10	GPO_CONTROL_2	GPO2_OD	OD	OD
0x10	GPO_CONTROL_2	GPO2_EN_PIN_CTRL[1:0]	GPO2_OUT bit	GPO2_OUT bit
0x10	GPO_CONTROL_2	GPO2_OUT	Low	Low
0x11	CONFIG	STARTUP_DELAY_SEL	0 - 15 ms with 1 ms steps	0 - 15 ms with 1 ms steps

Table 2. Summary of Registers Bits (continued)

Address	Register Name	Bit	LP87702D	LP87702K
0x11	CONFIG	SHUTDOWN_DELAY_SEL	0 - 15 ms with 1 ms steps	0 - 15 ms with 1 ms steps
0x11	CONFIG	CLKIN_PD	Disabled	Disabled
0x11	CONFIG	EN3_PD	Disabled	Disabled
0x11	CONFIG	EN2_PD	Disabled	Disabled
0x11	CONFIG	EN1_PD	Enabled	Enabled
0x11	CONFIG	TDIE_WARN_LEVEL	125 °C	125 °C
0x11	CONFIG	EN_SPREAD_SPEC	Disabled	Disabled
EXTERNAL SYNC CLOCK				
0x12	PLL_CTRL	EN_PLL	Enabled	Enabled
0x12	PLL_CTRL	EXT_CLK_FREQ[4:0]	2 MHz	2 MHz
POWERGOOD AND MONITORINGS				
0x13	PGOOD_CTRL	PGOOD_WINDOW	Undervoltage	Window
0x13	PGOOD_CTRL	EN_PGOOD_VANA	Enabled	Enabled
0x13	PGOOD_CTRL	EN_PGOOD_VMON2	Enabled	Enabled
0x13	PGOOD_CTRL	EN_PGOOD_VMON1	Enabled	Enabled
0x13	PGOOD_CTRL	EN_PGOOD_BOOST	Enabled	Enabled
0x13	PGOOD_CTRL	EN_PGOOD_BUCK1	Enabled	Enabled
0x13	PGOOD_CTRL	EN_PGOOD_BUCK0	Enabled	Enabled
0x14	PGOOD_LEVEL_1	VMON1_WINDOW[1:0]	±6 %	±4 %
0x14	PGOOD_LEVEL_1	VMON1_THRESHOLD[2:0]	0.65 V	1.20 V
0x15	PGOOD_LEVEL_2	VMON2_WINDOW[1:0]	±6 %	±4 %
0x15	PGOOD_LEVEL_2	VMON2_THRESHOLD[2:0]	1.80 V	1.80 V
0x15	PGOOD_LEVEL_2	VANA_WINDOW[1:0]	±10 %	±4 %
0x15	PGOOD_LEVEL_2	VANA_THRESHOLD	3.3 V	3.3 V
0x16	PGOOD_LEVEL_3	BOOST_WINDOW[1:0]	±6 %	±6 %
0x16	PGOOD_LEVEL_3	BUCK1_WINDOW[1:0]	±90 mV	±90 mV
0x16	PGOOD_LEVEL_3	BUCK0_WINDOW[1:0]	±90 mV	±90 mV
0x17	PG_CTRL	PG1_MODE	Invalid	Invalid
0x17	PG_CTRL	PGOOD_FAULT_GATES_PG1	Status	Status
0x17	PG_CTRL	PG1_POL	High	High
0x17	PG_CTRL	PG0_MODE	Invalid	Invalid
0x17	PG_CTRL	PGOOD_FAULT_GATES_PG0	Status	Status
0x17	PG_CTRL	PG0_OD	OD	OD
0x17	PG_CTRL	PG0_POL	High	High
0x18	PG0_CTRL	PG0_RISE_DELAY	11 ms	11 ms
0x18	PG0_CTRL	SEL_PG0_TWARN	No	No
0x18	PG0_CTRL	SEL_PG0_VANA	Yes	Yes
0x18	PG0_CTRL	SEL_PG0_VMON2	No	Yes
0x18	PG0_CTRL	SEL_PG0_VMON1	No	Yes
0x18	PG0_CTRL	SEL_PG0_BOOST	No	Yes
0x18	PG0_CTRL	SEL_PG0_BUCK1	Yes	No
0x18	PG0_CTRL	SEL_PG0_BUCK0	Yes	No
0x1A	PG1_CTRL	PG1_RISE_DELAY	11 ms	11 ms
0x1A	PG1_CTRL	SEL_PG1_TWARN	No	No
0x1A	PG1_CTRL	SEL_PG1_VANA	Yes	Yes
0x1A	PG1_CTRL	SEL_PG1_VMON2	Yes	Yes
0x1A	PG1_CTRL	SEL_PG1_VMON1	Yes	Yes
0x1A	PG1_CTRL	SEL_PG1_BOOST	Yes	Yes
0x1A	PG1_CTRL	SEL_PG1_BUCK1	Yes	Yes
0x1A	PG1_CTRL	SEL_PG1_BUCK0	Yes	Yes

Table 2. Summary of Registers Bits (continued)

Address	Register Name	Bit	LP87702D	LP87702K
WATCHDOG				
0x1C	WD_CTRL_1	WD_CLOSE_TIME[1:0]	100 ms	100 ms
0x1C	WD_CTRL_1	WD_OPEN_TIME[1:0]	100 ms	100 ms
0x1C	WD_CTRL_1	WD_LONG_OPEN_TIME[1:0]	5000 ms	5000 ms
0x1C	WD_CTRL_1	WD_RESET_CNTR_SEL[1:0]	Disabled	Disabled
0x1D	WD_CTRL_2	WD_SYS_RESTART_FLAG_MODE	Status	Status
0x1D	WD_CTRL_2	WD_EN_OTP_READ	Enabled	Enabled
0x1D	WD_CTRL_2	WDI_PD	Enabled	Enabled
0x1D	WD_CTRL_2	WDR_POL	Active low	Active low
0x1D	WD_CTRL_2	WDR_OD	OD	OD
0x35	WD_DIS_CONTROL	WD_DIS_CTRL	Enabled	Enabled
INTERRUPT MASKS				
0x29	TOP_MASK_1	I_MEAS_MASK	Masked	Masked
0x29	TOP_MASK_1	SYNC_CLK_MASK	Masked	Masked
0x29	TOP_MASK_1	TDIE_WARN_MASK	Unmasked	Unmasked
0x2A	TOP_MASK_2	RESET_REG_MASK	Masked	Masked
0x2B	BUCK_MASK	BUCK1_PGF_MASK	Masked	Masked
0x2B	BUCK_MASK	BUCK1_PGR_MASK	Masked	Masked
0x2B	BUCK_MASK	BUCK1_ILIM_MASK	Masked	Masked
0x2B	BUCK_MASK	BUCK0_PGF_MASK	Masked	Masked
0x2B	BUCK_MASK	BUCK0_PGR_MASK	Masked	Masked
0x2B	BUCK_MASK	BUCK0_ILIM_MASK	Masked	Masked
0x2C	BOOST_MASK	BOOST_PGF_MASK	Masked	Masked
0x2C	BOOST_MASK	BOOST_PGR_MASK	Masked	Masked
0x2C	BOOST_MASK	BOOST_ILIM_MASK	Masked	Masked
0x2D	DIAG_MASK	VMON2_PGF_MASK	Masked	Masked
0x2D	DIAG_MASK	VMON2_PGR_MASK	Masked	Masked
0x2D	DIAG_MASK	VMON1_PGF_MASK	Masked	Masked
0x2D	DIAG_MASK	VMON1_PGR_MASK	Masked	Masked
0x2D	DIAG_MASK	VANA_PGF_MASK	Masked	Masked
0x2D	DIAG_MASK	VANA_PGR_MASK	Masked	Masked
BUCK AND BOOST SWITCHING FREQUENCY				
0x31	FREQ_SEL	BOOST_FREQ_SEL	4 MHz	4 MHz
0x31	FREQ_SEL	BUCK_FREQ_SEL[1:0]	4 MHz	4 MHz
BOOST CURRENT LIMIT				
0x32	BOOST_ILIM_CTRL	BOOST_ILIM	1.4 A	1.4 A

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (January, 2018) to A Revision **Page**

- Updated Table 1 1

Changes from A Revision (June, 2018) to B Revision **Page**

- Updated Table 1 1
- Added LP87702K to Table 1 1

Changes from B Revision (November, 2019) to C Revision **Page**

- Added Figure 2 *Typical Connection to LP87702K-Q1* 2

Changes from C Revision (February, 2020) to D Revision **Page**

- Changed BOOST Bit Name From: *BUCK1_EN_PIN_CTRL, BUCK1_EN* To: *BOOST_EN_PIN_CTRL, BOOST_EN* 1

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