

TMS320C64x DSP Reference Design

Todd Hiers
DSP Applications

ABSTRACT

TI provides a reference design with commonly used configurations that allow customers to get maximum performance effortlessly from TMS320C64x™ DSP based systems. For extreme high performance, an SDRAM only interface is designed to run at speeds up to 150 MHz. The reference design also includes a USB bridge and other common DSP attach circuitry. The designs are suitable for simple modular drop-in use, allowing the use of some, many, or all parts of the design.

This reference design can be downloaded from this link.
<http://www-s.ti.com/sc/psheets/sprc137/sprc137.zip>

Contents

1	C64x Reference Design	1
2	C6414, C6415, and C6416 150 MHz EMIFA SDRAM Reference Design	2
	2.1 Clocking	2
	2.2 EMIF A: 150 MHz SDRAM	2
	2.3 EMIF B: USB Device Bridge	2
	2.4 PCI: PCI Expansion Card Edge Connector	3
	2.5 McBSP: McBSP-to-McBSP Communication	3
	2.6 McBSP: McBSP-to-RS232 for UART Communication	3
	2.7 Emulation: Advanced 60-pin Header	3
	2.8 Power: Switching Supplies	3
	2.9 Board Testing	4
	2.10 Distributed Files	4

1 C64x Reference Design

This reference design is intended to be used as a design aid for custom systems using C64x™ DSPs. The primary goal is to demonstrate proper printed circuit board (PCB) construction for DSP use and proper interfacing of the DSP to common external peripherals. Other factors such as cost, flexibility, and ease of manufacture were secondary design goals. The design expertise represented here is DSP-centric. These designs used best design practices at the time of their creation. However, users should ensure that the analog subsystems or other subsystems removed from the DSP are suitable for their use. In addition, system-level issues (e.g., EMI and thermal performance) must be addressed by the user, because they can not be fully addressed in the reference designs.

Fully functional boards can be manufactured based solely on the design files included with the reference design; however, the boards are not intended to be fabricated as-is for customer use. It was not designed with a particular application in mind, so some features might not be suitable or necessary for certain applications. Rather, this design should be seen as a conglomeration of different subsystems that can be copied as a starting point for a custom board.

Trademarks are the property of their respective owners.

TI recommends using the reference schematic as a starting point. Portions of the design can be copied in or cut out as desired. Similarly, the layout database can be used as a starting point for the layout work on the custom board. Using these examples can significantly speed up some of the complicated work in making a custom PCB, while significantly reducing the potential for error.

2 C6414, C6415, and C6416 150 MHz EMIFA SDRAM Reference Design

This reference design features the following subsystems:

- Clocking: 720 MHz (adjustable) DSP, 150 MHz (adjustable) EMIFA
- EMIFA: 128 MB of SDRAM operating at 150 MHz (4 256Mb x16 chips)
- EMIFB: USB device bridge (Cypress CY7C68001)
- PCI: PCI expansion card edge connector
- McBSP: McBSP-to-McBSP communication
- McBSP: McBSP-to-RS232 for UART communication
- Emulation: Advanced 60-pin emulation header
- Power: Switched 1.4v (adjustable) and 3.3v (fixed) supplies

2.1 Clocking

ICST501/ICST501A PLL clock generator chips are used to generate clocks from low cost and low speed crystals. DSPCLKIN is nominally 60 MHz (producing a 720 MHz CPU clock), but can be reduced to 50 MHz (for 600 MHz CPU clock) by populating/depopping some control resistors. Other DSP speeds can be achieved by choosing a different base crystal frequency, a different PLL mode on the ICST501, and/or a different PLL mode on the DSP. AECLKIN is nominally 150 MHz, and can be adjusted by changing the base crystal frequency or the ICST PLL mode.

2.2 EMIF A: 150 MHz SDRAM

EMIF A is connected to 128 MB of SDRAM running at 150 MHz. Four Micron MT48LC16M16A2-6 SDRAM chips are used, though any commodity 256Mb x16 166MHz speed-grade SDRAM should work. Other densities of SDRAM may be substituted, if they have the same physical address pinout. Any substituted part must meet or exceed the AC performance of the specified part.

NOTE: The reference design (four x16 SDRAM chips and NO other loads) is the ONLY supported 150 MHz EMIFA configuration. You must use the reference layout for the EMIFA traces exactly as they are in the design database. Due to the extreme performance, margins are very tight, and TI will not support other configurations or layouts at 150 MHz. 133 MHz or slower can be achieved by following methodologies laid out in the device data sheets or other TI application reports.

2.3 EMIF B: USB Device Bridge

A Cypress CY7C68001 is used to interface a USB slave device port to the EMIFB on the DSP. In addition, some of the status signals from the USB bridge are connected to GPIO pins on the DSP. The specifics of this interface and use of the device are described in application report *TMS320C6000 EMIF to USB Interfacing Using Cypress EZ-USB SX2™* (SPRAA13).

2.4 PCI: PCI Expansion Card Edge Connector

The reference design demonstrates the proper way to connect the DSP to a PCI-compliant expansion card edge connector. This edge connector is PCI v2.2 compliant. The edge connector is 3.3v-only, as the DSP is not 5v tolerant.

2.5 McBSP: McBSP-to-McBSP Communication

In the TMS320C64x DSP Reference Design, a McBSP-to-McBSP is a loopback link because there is only one DSP on the board. In practice, this type of connection is useful as an inter-DSP connection, and the example is useful in showing how to use the McBSP that way, too.

2.6 McBSP: McBSP-to-RS232 for UART Communication

A McBSP is connected to a DB9 socket through an RS232 line driver. The DB9 connector is pinned out as DTE. DCE wiring is possible, but not shown. Sideband RS232 signals (DTR, RTS, CTS, DSR, and DCD) are connected to timer pins on the DSP. These signals are optional for basic UART functionality, and could be connected to any GPIO pins on the DSP as desired.

For more detail on McBSP-to-UART communication, see *TMS320C6000 McBSP: UART* (SPRA633).

2.7 Emulation: Advanced 60-pin Header

The DSP Emulation port is connected to the new 60-pin emulation header. This header allows for advanced emulators to take full advantage of the emulation features built in to the DSP. An adapter is available to connect 14-pin emulation pods to the new 60-pin header. Contact the Product Information Center for details.

In addition, the emulation pod presence detect line is connected to a GPIO input.

For more detail on the new emulation header, see *60-Pin Emulation Header Technical Reference* (SPRU655).

2.8 Power: Switching Supplies

Power is regulated on board by a pair of integrated switching regulators. These are used because they are highly efficient and can accommodate a range of input voltages. 3.3v power is regulated by a TPS62007, which is capable of sourcing up to 600mA @ 3.3v. 1.4v power is regulated by a TPS54310, which is capable of sourcing up to 3A. The voltage produced by the TPS54310 is also adjustable by changing two resistors in the feedback net. The startup ordering of the power supplies is controlled and 3.3v-first by default. It can be reversed by populating/depopulating the appropriate control resistors.

In addition to the power supplies, a power supervisor is used to generate system reset. The TPS3106K33 monitors both supplies and provides the master reset signal to the board. Adjusting the 1.4v supply requires a similar adjustment in the sense line of the supervisor.

2.9 Board Testing

The design was put through rigorous pre-fabrication simulation and post-manufacturing sanity checks. Timings and signal integrity analyses were done according to *Using IBIS Models for Timing Analysis* (SPRA839). EMIF timings were verified and extremely tight. Manufactured boards were tested at high temperature as a verification of the simulation work.

On-board power regulation was evaluated to ensure compliance with the DSP CVDD and DVDD specification. Power was observed directly on the BGA vias furthest from the power regulators with a 100-MHz bandlimited probe.

In addition, EMI tests were performed. While running a random-data memory test, the board was well within FCC class 'A' limits.

2.10 Distributed Files

- Fast13.pdf – Schematics in PDF format
- Fast_release.dsn – schematics in OrCAD design format
- Fast_bom.xls – Bill of materials in Excel format
- Fast_pads2k.asc – Netlist in PADS 2000 format
- Fast_wirelist.txt – Netlist in ASCII wirelist format
- Fast_pcb.zip – Layout database in various formats, zipped
- Fast_gerber.zip – Layout in Gerber format, zipped

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265