TMS320DM643x Power Consumption Summary

Jacqui A. Swift

ABSTRACT

NOTE: PRELIMINARY DATA FOR TMX DEVICES. INFORMATION SUBJECT TO CHANGE.

This application report discusses power consumption of the Texas Instruments TMS320DM643x Digital Media Processor (DMP). Power consumption is highly application-dependent, so a spreadsheet is provided to model power consumption for your applications.

This application report contains a spreadsheet that can be downloaded from http://www.ti.com/lit/zip/SPRAAO6.

NOTE: TMX devices are experimental devices that are not necessarily representative of the final device's electrical specifications.

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1 Introduction

To achieve good results from the spreadsheet, realistic usage parameters must be entered. The low-core voltage and other power design optimizations allow these devices to operate with industry-leading performance, while maintaining a low power-to-performance ratio.

The DM643x devices are offered into basic options: lower power option and high performance option. Low power devices offer lower power consumption across temperature and voltage when compared with high performance devices. However, high performance devices offer higher operating speeds. Low power devices can be identified by the use of an –L in their part numbers.

The accompanying spreadsheet gives you the capability to estimate power consumption on high-performance and low-power devices. The data presented in the accompanying spreadsheet was measured from units representative of the high-end of power consumption for production units; no production units have average power consumption that exceeds the spreadsheet values. Therefore, the spreadsheet values can be used for board thermal analysis and power supply design as a maximum long-term average.

> **NOTE:** All power measurements were taken from silicon revision 1.1 units of the TMX320DM6437.

Typical production units will have lower power consumption than high-performance devices and even low power devices. Table 1 shows the power consumption at a given configuration for worst-case high-performance and low-power devices as well as a typical device.

Table 1. Typical Activity

Core Voltage	CPU Frequency	Device Type [2]	Power at Frequency (W) [1]			
			Internal Logic	IO18	IO33	Total
1.2 V	702 MHz	HIGH PERF	991	169	42	1202
		TYPICAL UNITS	716	169	42	927
1.2 V	594 MHz	HIGH PERF	889	167	42	1098
		LOW POWER	732	167	42	941
		TYPICAL UNITS	628	167	42	838
1.2 V	459 MHz	HIGH PERF	760	165	42	967
		LOW POWER	603	165	42	810
		TYPICAL UNITS	519	165	42	726
1.05 V	459 MHz	HIGH PERF	511	131	42	683
		LOW POWER	407	131	42	580
		TYPICAL UNITS	397	131	42	870

[1] Assumes the following conditions: 60% DSP CPU utilization; (peripheral configurations, other housekeeping activities) DDR2 at 50% utilization (135 MHz), 50% writes, 32 bits, 50% bit switching, 2-MHz McBSP0 at 100% utilization; Timer0 at 100% utilization at room temp (25°C) using ZWT package.

[2] The difference in power consumption between high-performance, low-power, and typical units is essentially due to the difference in static current that varies with process, temperature, and voltage. The static current consumption for typical process was determined by averaging measured data from multiple units. See Section 2.1 for more details.

2 Activity-Based Models

TMS320DM643x power consumption can vary widely depending on how the on-chip resources are used. Thus, power consumption cannot be estimated accurately without an understanding of the components in use and the usage patterns for those components. By providing the usage parameters that describe how and what is being used, accurate consumption numbers can be obtained for power-supply and thermal analysis.

The power consumption is broken down into two major components in this application report: baseline power and activity power. This document shows you how to obtain accurate predictions through different applications with varying system requirements.

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2.1 *Baseline Power*

Baseline power describes power that is independent of any chip activity. This includes things like static power (leakage), phased-locked loop (PLL) power, oscillator power, DDR2 DLL power, and clock tree power to various subsystem components (e.g., SCR) that cannot be turned off via the on chip power management module. While independent of activity, baseline power is dependent on the device operating frequency, voltage, and temperature, see Figure 1 and Figure 2. Thus, you can affect baseline power only by changing the PLL(s) output frequency, the core voltage, or the operating temperature.
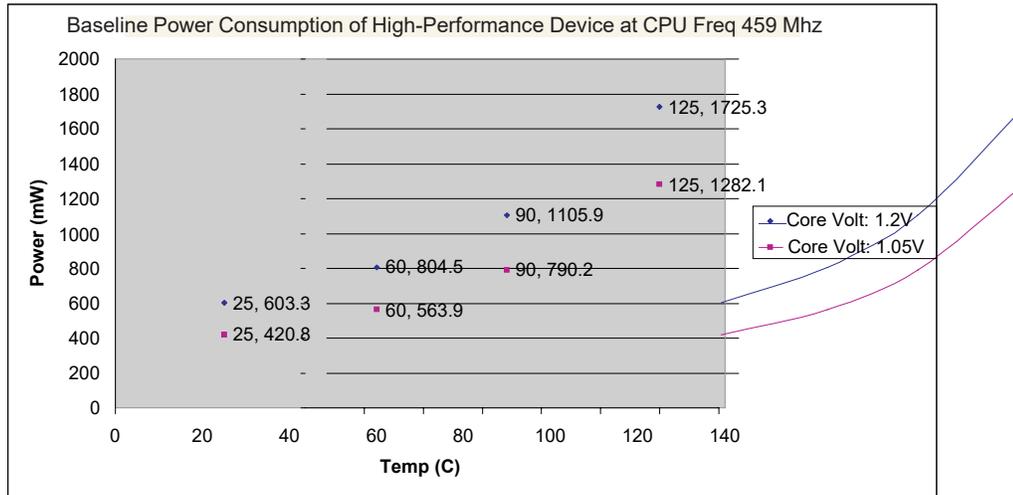

Figure 1. Baseline Power Consumption Across Voltage and Temperature: High-Performance
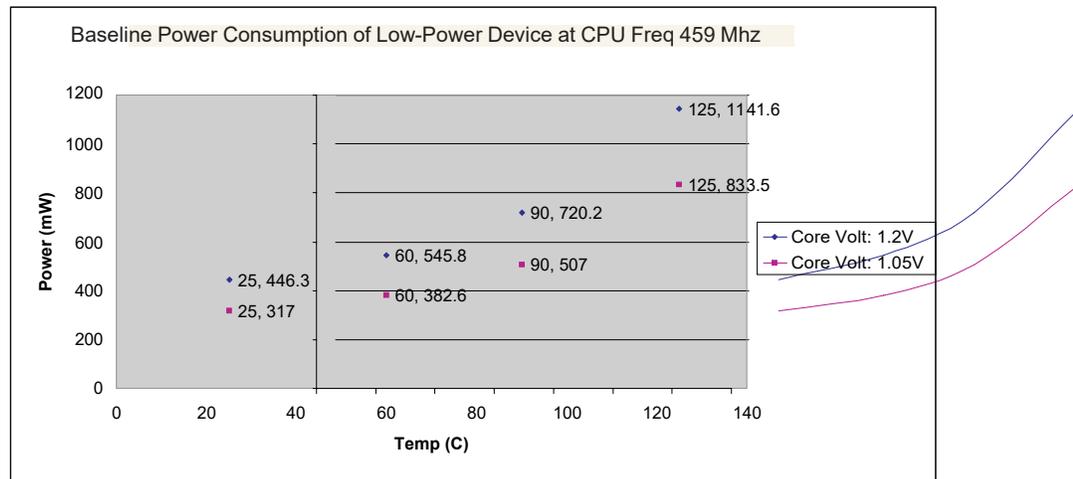

Figure 2. Baseline Power Consumption Across Voltage and Temperature: Low-Power

2.2 *Activity Power*

Activity power describes power that is consumed by the active modules of the DMP (i.e, the CPU(s), external memory interfaces (EMIFs), peripherals, etc.). Activity power is independent of temperature, but dependent on voltage and activity levels. Activity power is separated by the major modules of the device, so their contribution can be measured independent of each other which helps tailoring power consumption to specific applications. The parameters used to determine the activity level of a module are frequency, utilization, read/write balance, bus size, and switching probability.

NOTE: Not all parameters apply to all modules.

- Frequency is the operating frequency of a module or the frequency of external interface to that module.
- Status indicates whether the module is in an enabled or disabled state.
- % utilization is the relative amount of time the module is active or in use vs off or idled.
- % write is the relative amount of time (active time only) the module is sending data out of the device vs reading data into the device.
- Bits is the number of data bits being used in a selectable-width interface.
- % switch is the probability that any one data bit changes state from one cycle to the next.

2.3 Modules

The DM643x power estimation spreadsheet contains the following modules with adjustable parameters:
- Phase Locked Loop 1 (PLL1)
- Digital signal processor (DSP)
- Video processing front end (VPFE)
- Video processing back end (VPBE)
- DDR2 memory controller
- Asynchronous EMIF (EMIFA)
- Enhanced direct memory access (EDMA3)
- Ethernet MAC (EMAC)
- VLYNQ™
- Host-port interface (HPI)
- Multichannel buffered serial port (McBSP0/1)
- Multichannel audio serial port (McASP0/1)
- Inter-integrated circuit (I2C)
- Timer 0/1
- Watchdog Timer (WDT)
- Pulse width modulation (PWM 0/1/2)
- Peripheral component interconnect (PCI)
- High-end CAN controller (HECC)
- Universal asynchronous receiver/transmitter 0/1 (UART 0/1)
- General-purpose input/output (GPIO)

Although EDMA3 is listed as a separate module, the row essentially provides the power consumption for turning on the clock to the channel controller and the transfer controller(s) for a particular device frequency and voltage. The EDMA3 activity power is included in the module/peripheral serviced by the EDMA3 (this includes McBSP, McASP, DDR2). Therefore, in estimating power for peripherals that typically use EDMA3 for their transfers, the EDMA3 should be kept enabled. For available peripherals and peripheral configuration, please see the device-specific data manual.

3   Using the Power Estimation Spreadsheet

3.1   *Choosing Appropriate Values*

The *Frequency* and *Bits* values are determined by design and it is clear what the correct values to enter are. For some modules, the *Frequency* field is used to input the data rates (i.e., ethernet media access controller (EMAC)). The utilization, read/write balance, and bit switching values require estimation and a good understanding of the end application; avoid enabling peripherals whose configurations are mutually exclusive due to pin multiplexing. For available peripherals and peripheral configuration, please see the device-specific data manual.

Using the power estimation spreadsheet involves simply entering the appropriate usage parameters. Cells that are designed for you to input information are white in color. To use the spreadsheet, simply:

1. Select the voltage, junction temperature, package type designator, and airflow for which you want to estimate power
2. Fill in the appropriate module use parameters

The spreadsheet takes the provided information and displays the details of power consumption for that configuration.

As the spreadsheet is being configured, the settings are checked for conflicts, (for example, peripheral clock frequency out of allowed range, etc.). For best results, the information should be entered from left to right starting at the top and moving downward.

3.1.1   % Utilization

For most modules, except DSP (C64x+), *% Utilization* is simply the percentage of time the module spends doing something useful, as opposed to being unused or idle. There are not varying degrees of use; the value should reflect an average over time. An example would be an EMIF performing reads and writes one-quarter of the time and having no data to move for the remaining three-quarters of time (though it continues to perform background tasks like refresh). In this case, the *% Utilization* would be quantified as 25%.

For peripherals with IO, *% Utilization* can be estimated by comparing used bandwidth with theoretical maximum bandwidth. For example, for an application that must transfer 160 Kb/s via the inter-integrated circuit (I2C) port, whose theoretical maximum is 400 Kb/s, then the I2C port utilization would be about 40%. This type of activity reduces overall utilization and renders a utilization designation of 100% as impractical. If estimating across different frequencies, this must be taken into consideration.

The CPU utilization isn't as straightforward, because there are varying degrees of use. In this instance, a 0% utilization designation means that the CPU is active, but is not performing useful tasks (i.e., NOP execution). A 100% utilization designation represents a high activity condition with all eight functional units being active every cycle, while making use of the software pipelined (SPLOOP) buffer hardware where the maximum amount of data is brought in from L1P and L1D every cycle. Few DSP algorithms achieve 100% utilization because this requires everything to be used every cycle, with no stalls. Even intense applications do not spend all of the time in such highly paralleled loops. Typically, some time is allocated to executing control code or less demanding algorithms where only a few instructions operate in parallel and IO usage is significantly reduced. This type of activity reduces the overall utilization and renders 100% utilization designation as impractical. Therefore, the balance of CPU use for the duration of the application must be considered.

For example, consider an application that executes very dense CPU code (estimated at 90% of CPU capability) for half of the time, and executes low activity code along with some other house keeping activities (estimated at 10% of CPU capability) for the other half of time. This application would yield an average utilization of about 50% (10% × 50% + 90% × 50%). If the balance were changed to 25% low activity code and 75% DSP code, the weighted average would be about 70% utilization (25% × 10% + 90% × 75%). If the 25%/75% ratio is kept, but the DSP code does not fully use all the CPU resources (estimate now at 75% of CPU capability), then the overall utilization returns to about 59% (25% × 10% + 75% × 75%). By using estimates of intensity and duration of blocks of code in the application, an estimate of the overall CPU utilization can be obtained.

System level issues may reduce peripheral *% Utilization*. Though the spreadsheet accepts 100% utilization for all peripherals, generally this is not realistic for the duration of the application. As concurrency in data movement increases and/or throughput requirements on high bandwidth modules (system direct memory access (DMA), VPSS, etc.) increases, overall peripheral activity is decreased due to bottlenecks created at various common end points. In such cases, peripherals will probably not achieve 100% utilization; individual module utilization numbers should be entered keeping this overall limitation in mind.

3.1.2   % Writes

Peripherals that move data out of the device as much as they move data into the device have 50% writes (the spreadsheet assumes the remaining 50% of the time is spent on reads). In some applications, peripherals only move data in one direction, or may have a known balance of data movement. In these cases, *% Writes* should be changed as appropriate. Otherwise, a designation of 50% writes is recommended.

3.1.3   % Switching

Random data has a 50% chance any bit changes from one cycle to the next. Some applications may be able to predict this chance using some prior information about the data set. If there is an ability to predict bit changes, the application-specific probability can be used. All other applications should use the default number of 50%.

3.2   *Peripheral Enabling and Disabling*

As mentioned earlier, the DM643x devices provide the capability to disable modules that are not being used via the power sleep controller (PSC). When a peripheral is disabled, its clock is turned off thereby reducing the power consumption of the device.

The spreadsheet accommodates this power saving feature by including fields in which a peripheral can be specified as disabled or enabled.

If a module is not used in a given application, then it is recommended to keep it in disabled state.

It is plausible that the module is kept enabled but has no activity. This can be appropriately programmed by setting the *% Utilization* and/or the *Frequency* fields to a value of 0, in which case the numbers in the module's row are indicative of the power consumed by clocking the module.

For VPFE and VPBE, the enable/disable functionality is controlled by the video processing sub system (VPSS) enable/disable switch in the spreadsheet. If the application requires the use of VPFE and/or VPBE, you should implement it by *enabling* the VPSS.

If an application requires the use of VPFE and VPBE in the system, this automatically implies that the DDR2 is also enabled and active in the system. To estimate power for such scenarios, you need to make sure that the DDR2 fields are programmed with the appropriate frequency, utilization percentage, read/write percentage, etc., required by the VPFE and/or VPBE.

In the current implementation of the spreadsheet, if the DDR2 is disabled, it also assumes that the PLL2 is powered down and is operating in bypass mode with the DDR2 clock being directly fed by the input reference clock (27 MHz CLKIN).

4   Using the Results

The results presented by the spreadsheet are based on measured data for revision 1.1 silicon of the TMX320DM6437 (see the device-specific datasheet for the Device and Development-Support Tool Nomenclature).

The intent of the power estimation spreadsheet is to provide estimates of the upper bounds in an application-specific loading and peripheral utilization scenario. Therefore, the measured devices were selected at the maximum end of power consumption for production units; no production units have average power consumption that exceeds the spreadsheet values. The spreadsheet data can be considered maximum average power consumption; the actual observed power may vary. That is, transient currents may cause power to spike above the spreadsheet value for a small amount of time, but over a long period of time, the observed average consumption is below the spreadsheet value. Thus, the spreadsheet value can be used for board thermal analysis and power supply design as a maximum long-term average.

5   Thermal Considerations

As integrated circuit (IC) components become more complex, the challenge of producing an end equipment product with good thermal performance also increases. Thermal performance is a system level concern, impacted by IC packaging as well as printed circuit board (PCB) design, PCB characteristics, PCB layout, ambient temperature, and chassis configuration.

In the *TMS320DM6437 Digital Media Processor* (SPRS345) (referred to throughout the remainder of the document as the DM643x data manual) TI specifies not to exceed the maximum operating junction temperature so that device reliability and/or proper operation can be maintained. To meet this requirement, it is important to understand the contribution of the other system characteristics (mentioned above) and design accordingly. Before finalizing system layout and PCB design, verify that the maximum operating junction temperature documented in the DM643x data manual is met.

This section addresses the thermal considerations specific to the DM643x devices and should be used in conjunction with the *Thermal Considerations for TMS320DM64xx, TMS320DM64x, and TMS320C6000 Devices* (SPRAAL9). The *Thermal Considerations for TMS320DM64xx, TMS320DM64x, and TMS320C6000 Devices* (SPRAAL9) discusses many general thermal considerations that apply to DM64xx, DM64x, and C6000™ DSP devices. For more information regarding definitions of thermal terms, methods for calculating case temperature, recommendations for system thermal improvements, heat sink recommendations, and heat sink attachment methods, see the *Thermal Considerations for TMS320DM64xx, TMS320DM64x, and TMS320C6000 Devices* (SPRAAL9).

One of the most commonly considered thermal improvement methods is the heat sink. A numerical approach that estimates the thermal impact of adding an off the shelf heat sink purchased from a vendor is shown below. This method requires ambient temperature, case temperature, and DM643x power to be either measured or estimated without a heat sink in the real system. To be consistent with JEDEC measurement techniques, as well as to reference the most independent and static temperature point, TI recommends measuring the final system ambient temperature outside the enclosure; the inside the enclosure may be influenced by heating from other parts.

The spreadsheet that accompanies this application report includes a worksheet that performs the calculations described in the following heat dissipation examples. You must enter values for the following fields in the worksheet: package type, ambient temperature, case temperature, total power, and θ_{CA} from a heat sink data sheet. All of the remaining fields in the worksheet are calculated based on your inputs.

5.1   *Thermal Heat Dissipation Example for the ZWT Package*

Numbers for an actual application need to be calculated. From system analysis, suppose you determine:

- Ambient temperature: T_A = 45°C
- Case temperature: T_C = 85°C
- Device power = 1.5 W

NOTE: This is a reasonable example, but your specific information is required.

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1. Calculate an estimate of $\theta_{JA,effective}$ using the following equation. Plug in values for ambient temperature, case temperature and device power from the list above. This example assumes junction temperature and case temperature are approximately equal, therefore T_J = 85°C.

$$\theta_{JA, effective} = \frac{T_J - T_A}{Power} = \frac{85 - 45}{1.5} = 26.7 \frac{C}{W}$$

2. Estimate the percentage of heat flowing through the PCB vs. the top of the device. Based on experience with typical systems, TI estimates 80% of the heat flow is through the PCB, without a heat sink attached. The thermal resistance through the top and bottom of the device are two parallel resistances that equal $\theta_{JA,effective}$ (see Figure 4). Therefore, θ_{top} and θ_{bot} can be defined as follows:

$$\frac{80\%}{20\%} = 4 \text{ therefore, } \theta_{top} = 4 \cdot \theta_{bot}$$

$$\theta_{JA,\ effective} = \frac{1}{\frac{1}{\theta_{top}} + \frac{1}{\theta_{bpt}}} = \frac{1}{\frac{1}{4\theta_{bot}} + \frac{1}{\theta_{bot}}}$$

$$1.25 \cdot \theta_{JA,\ effective} = \theta_{bot} = \frac{1}{4} \cdot \theta_{top}$$

$$5 \cdot \theta_{JA,\ effective} = \theta_{top}$$

Use the following equations to calculate θ_{top} and θ_{bot}:

$$\theta_{top} = \theta_{JA,\ effective} \times 5 = 26.7 \times 5 = 133.5 \frac{C}{W}$$

$$\theta_{bot} = \theta_{JA,\ effective} \times 1.25 = 26.7 \times 1.25 = 33.4 \frac{C}{W}$$

Check by calculating the parallel resistance of θ_{top} and θ_{bot}.

$$\theta_{JA,\ effective} \frac{1}{\frac{1}{\theta_{top}} + \frac{1}{\theta_{bot}}} \frac{1}{\frac{1}{133.5} + \frac{1}{33.4}} 26.7 \frac{C}{W}$$

3. Use the following equation to estimate the thermal resistance from the top of the DM643x to the environment, for a reference. This thermal resistance is called θ_{CA} (see Figure 4). For DM643x, θ_{JC} = 5.4°C/W. θ_{JC} is documented in the DM643x data manual.

$$\theta_{CA} = \theta_{top}(\text{step2}) - \theta_{JC} = 133.5 - 5.4 = 128.1 \frac{^{\circ}C}{W}$$

4. Replace θ_{CA} calculated in step 3, with θ_{CA} specified from a heat sink data sheet and recalculate heat flow through the top of the device with a heat sink added. Note that θ_{CA} and θ_{top} should be reduced with the addition of a heat sink.

For this example we chose a heat sink with θ_{CA} = 62.5°C/W (for example heat sink search for part number: 375424B00034G).

Width	Length	Height	Fin Thickness Across Width	Fin Thickness Across Length	Base Thickness	# of Fins Across Width	# of Fins Across Length
15.20 mm	15.20 mm	6.35 mm	0.89 mm	0.89 mm	1.52 mm	8	8

Figure 3. Heat Sink Example Information

$$\theta_{top}(w/HS)\theta_{CA}(\text{from HS}) + \theta_{JC} = 62.5 + 5.4 = 67.9 \frac{^{\circ}C}{W}$$

5. Calculate the new $\theta_{JA,effective}$ with a heat sink as well as the improved T_C.

$$\theta_{JA,\ effective} = \frac{1}{\frac{1}{\theta_{top}} + \frac{1}{\theta_{bot}}}$$

$$\theta_{JA,\ effective\ (w/HS)} = \frac{1}{\frac{1}{67.9} + \frac{1}{33.4}} = 22.4 \frac{C}{W}$$

Therefore, the new T_C with heat sink can be calculated as follows:

$$T_J = T_A + \left(\text{Power} \times \theta_{JA, \text{effective}}\right) = 45 + \left(1.5 \times 22.4\right) = 78.6 \ °C$$

The heat sink in this application is estimated to improve the junction temperature from a value of 85°C, considered marginal with respect to the data sheet T_J spec, to a value of 78.6°C.

NOTE: This example uses published data from a heat sink that is currently available. The same type of method can be used to estimate the impact of using a chassis as a heat sink, but the calculation is more difficult because this is not published data.

5.2   *Thermal Heat Dissipation Example for the ZDU Package*

Numbers for an actual application need to be calculated. From system analysis, suppose you determine:

- Ambient temperature: $T_A = 45°C$
- Case temperature: $T_C = 70°C$
- Device power = 1.5 W

This is a reasonable example, but your specific information is required.

1. Calculate an estimate of $\theta_{JA,\text{effective}}$ using the following equation. Plug in values for ambient temperature, case temperature and device power from the list above. For the DM643x, $\Psi_{JT} = 4.9°C/W$. Ψ_{JT} is documented in the DM643x data manual.

$$T_J = T_C + \left(\text{Power} \times \Psi_{JT}\right) = 70 + \left(1.5W \times 4.9 \frac{°C}{W}\right) = 77.35 \ °C$$

$$\theta_{JA, \text{effective}} = \frac{T_J - T_A}{\text{Power}} = \frac{77.35 - 45}{1.5} = 21.6 \frac{°C}{W}$$

2. Estimate the percentage of heat flowing through the PCB vs. the top of the device. Based on experience with typical systems, TI estimates 80% of the heat flow is through the PCB, without a heat sink attached. The thermal resistance through the top and bottom of the device are two parallel resistances that equal $\theta_{JA,\text{effective}}$ (see Figure 4). Therefore, θ_{top} and θ_{bot} can be defined as follows:

$$\frac{80\%}{20\%} = 4 \text{ therefore, } \theta_{top} = 4 \times \theta_{bot}$$

$$\theta_{JA, \text{effective}} = \frac{1}{\frac{1}{\theta_{top}} + \frac{1}{\theta_{bpt}}} = \frac{1}{\frac{1}{4\theta_{bot}} + \frac{1}{\theta_{bot}}}$$

$$1.25 \times \theta_{JA, \text{effective}} = \theta_{bot} = \frac{1}{4} \times \theta_{top}$$

$$5 \times \theta_{JA, \text{effective}} = \theta_{top}$$

Use the following equations to calculate θ_{top} and θ_{bot}:

$$\theta_{top} = \theta_{JA, \text{effective}} \times 5 = 21.6 \times 5 = 108 \frac{°C}{W}$$

$$\theta_{bot} = \theta_{JA, \text{effective}} \times 1.25 = 21.6 \times 1.25 = 27 \frac{°C}{W}$$

Check by calculating the parallel resistance of θ_{top} and θ_{bot}.

$$\theta_{JA, \text{effective}} = \frac{1}{\frac{1}{\theta_{top}} + \frac{1}{\theta_{bot}}} = \frac{1}{\frac{1}{108} + \frac{1}{27}} = 21.6 \frac{°C}{W}$$

3. Use the following equation to estimate the thermal resistance from the top of the DM643x to the environment. This thermal resistance is called θ_{CA} (see Figure 4). For DM643x, $\theta_{JC} = 7.7°C/W$. θ_{JC} is documented in the DM643x data manual.

$$\theta_{CA} = \theta_{top} \left(\text{step2}\right) - \theta_{JC} = 108 - 7.7 = 100.3 \frac{°C}{W}$$

4. Replace θ_{CA} calculated in step 3, with θ_{CA} specified from a heat sink data sheet and then recalculate the heat flow through the top of the device with a heat sink added. Note that θ_{CA} and θ_{top} should be reduced with the addition of a heat sink.

For this example we chose a heat sink with θ_{CA} = 62.5°C/W (for example heat sink search for part number: 375424B00034G).

	Width	Length	Height	Fin Thickness Across Width	Fin Thickness Across Length	Base Thickness	# of Fins Across Width	# of Fins Across Length
	15.20 mm	15.20 mm	6.35 mm	0.89 mm	0.89 mm	1.52 mm	8	8

Figure 4. Heat Sink Example Information

$$\theta_{top}(w/HS) = \theta_{CA}(from\,HS) + \theta_{JC} = 62.5 + 7.7 = 70.2\, \frac{^\circ C}{W}$$

5. Calculate the new $\theta_{JA,effective}$ with a heat sink as well as the improved T_C.

$$\theta_{JA, effective} = \frac{1}{\frac{1}{\theta_{top}} + \frac{1}{\theta_{bot}}}$$

$$\theta_{JA, effective}(w/HS) = \frac{1}{\frac{1}{70.2} + \frac{1}{27}} = 19.5\, \frac{^\circ C}{W}$$

The new TC with heat sink can be calculated as follows:

$$T_J = T_A + \left(Power \times \theta_{JA, effective} \right) = 45 + (1.5 \times 19.5) = 74.25\ ^\circ C$$

The heat sink in this application is estimated to improve the junction temperature from a value of 77.35°C to a value of 74.25°C.

> **NOTE:** This example uses published data from an off the shelf heat sink. The same type of method can be used to estimate the impact of using a chassis as a heat sink, but the calculation is more difficult because this is not published data.

6   Limitations

The power estimation spreadsheet has the following limitations:

*   All measurements have been performed with a 27 MHz CLKIN provided by an external oscillator. The spreadsheet does not provide a capability of estimating power based on a different CLKIN value.

7   References

*   *Thermal Considerations for TMS320DM64xx, TMS320DM64x, and TMS320C6000 Devices* (SPRAAL9)
*   *TMS320DM6437 Digital Media Processor* (SPRS345)
*   *TMS320DM6435 Digital Media Processor* (SPRS344)
*   *TMS320DM6433 Digital Media Processor* (SPRS343)
*   *TMS320DM6431 Digital Media Processor* (SPRS342)
*   *TMS320DM643x DMP DSP Subsystem Reference Guide* (SPRU978)
*   *TMS320C64x+ Megamodule Reference Guide* (SPRU871)
*   *TMS320DM644x Power Consumption Summary* (SPRAAD6)