TMS320C6457 Power Consumption Summary

High-Performance and Multicore Processors

Abstract

This document discusses the power consumption of the Texas Instruments TMS320C6457 digital signal processor (DSP). The power consumption of the device is highly application-dependent. Therefore, a power spreadsheet that estimates power consumption is provided along with this application report. This spreadsheet can be used to model power consumption for user applications such as power supply design, thermal design, etc. To obtain good results from the spreadsheet, realistic usage parameters must be entered (see Section 3.1). The low core voltage and other power design optimizations allow these devices to operate with industry-leading performance, while maintaining a very good power-to-performance ratio.

The data presented in this document and in the accompanying spreadsheet were measured from devices at the maximum end of the power consumption for production devices. No production devices will have average power consumption that exceeds the spreadsheet values. Therefore, the spreadsheet values may be used for board thermal analysis and power supply design as a maximum long-term average.

The spreadsheet discussed in this application report can be downloaded from the following URL: http://www.ti.com/lit/zip/SPRAB42.

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1 Activity-Based Models

Power consumption for the TMS320C6457 DSP can vary widely depending on the use of on-chip resources. Therefore, power consumption cannot be estimated accurately without an understanding of the components of the DSP in use and the usage patterns for those components. By providing the usage parameters that describe how and what is being used on the DSP, accurate power consumption numbers can be obtained for power-supply and thermal analysis. Expected power consumption for worse case utilization can be determined by choosing the peripherals in use.

The power spreadsheet divides the power consumption into two major components: baseline power and activity power.

1.1 Baseline Power

Baseline power consumption is the power consumed that is independent of chip activity; such as static leakage power, and core power (core power includes clock tree, internal memory, on-chip module power, etc.). Baseline power is highly dependent on voltage, temperature, and CPU frequency.

1.2 Activity Power

Activity power consumption is power that is consumed by all active parts of the DSP: central processing unit (CPU), enhanced direct memory access (EDMA), peripherals, etc. The activity power is independent of temperature, but highly dependent on activity levels of the CPU, EDMA, peripherals, etc. In the power spreadsheet, activity power is separated by the major modules/peripherals within the device. Therefore, the individual module/peripheral power consumption can be estimated independently. This helps with tailoring power consumption to specific applications.

Module/peripheral activity power consumption includes some necessary EDMA and CPU activity used to transfer data on-chip and off-chip when required. The power consumption associated with EDMA and CPU activity has been minimized to show only power consumption with respect to the module/peripheral tested.

2 Spreadsheet Parameters

The spreadsheet provides configurable parameters, which allows the estimation of power consumption based on configured usage parameters. To ensure realistic results, verify that the spreadsheet is configured accurately. For more details, see Section 3.1.

The parameters are as follows:

- **Frequency:** The operating frequency of a module/peripheral or the frequency of the external interface to that module.
- **Modes:** Allows peripheral-specific configuration mode to be selected.
- **Status:** Indicates whether a peripheral is *Enabled* and configured for use, or *Disabled* and unconfigured.
- **% Utilization:** The relative amount of time the module is active or in use versus off or idle.
- **% Write:** The relative amount of time (considering active time only) the module is transmitting versus receiving.
- **Bits:** The number of data bits being used in a selectable-width interface.
- **% Switching:** The probability that any one data bit on the relative data bus will change state from one cycle to the next.

2.1 Power Domains Details

The TMS320C6457 device has the capability to power-down and clock-gate peripherals within power domains [4:1]. When the power domain for a peripheral is disabled, the peripherals' memories are put to sleep for low-leakage mode and the peripheral is held in reset and clock gated, thereby reducing the power consumption of the device. Note that the device comes out of reset with power domains [4:1] disabled.

The spreadsheet that accompanies this application report allows a power domain to be disabled by selecting *Disabled* for the peripheral in the *Status* column.

The following peripherals have power domains available for power down:

- Serial RapidIO (SRIO) - Power Domain 1
- Turbo-Decoder Coprocessor 2 (TCP2) (Instance 0) - Power Domain 2
- Turbo-Decoder Coprocessor 2 (TCP2) (Instance 1) - Power Domain 3
- Viterbi-Decoder Coprocessor 2 (VCP2) - Power Domain 4

For more information, see the *TMS320C6457 Power/Sleep Controller (PSC) User's Guide* (SPRUGL4).

2.2 Device Modules/Peripherals

The TMS320C6457 power estimation spreadsheet contains the following modules with adjustable parameters:

- CPU
- EMIFA
- DDR2
- McBSP [1:0]
- VCP2
- TCP2 [1:0]
- UTOPIA
- EMAC
- SRIO
- Timer [1:0]
- HPI
- I^2C

EDMA is not listed as a separate module because the module/peripheral activity already includes any necessary EDMA activity used for memory-to-memory transfers only. For available peripheral configurations, see the device-specific data sheet.

2.3 UTOPIA I/O Power Results

The I/O power consumption for UTOPIA was estimated using the dynamic power equation, CV^2F, instead of measured silicon results. The following parameters were used for variables within the formula for each peripheral:

- Capacitance
  - Input pins = 1 pF
  - Output pins = 10 pF
- Voltage = 3.3 V
- Frequency
  - Peripheral I/O operating frequency. Note that control and data line frequencies are scaled based on the appropriate toggling rates.

2.4 HPI Core Power Results

The core power consumption for HPI was modeled from a previous technology node, instead of using measured silicon results. The following parameters were used as inputs for the model:

- Capacitance
  - Input pins = 4-6 pF
  - Output pins = 10 pF

3 Using the Power Estimation Spreadsheet

Using the power estimation spreadsheet involves entering the appropriate usage parameters as input data in the spreadsheet. The following steps explain how to use the spreadsheet:

1. Choose the device core voltage and maximum CPU operating frequency. The four device core voltage and CPU operating frequency combinations are listed below:
   - Core voltage = 1.1 V, maximum CPU frequency = 850 MHz
   - Core voltage = 1.1 V, maximum CPU frequency = 1000 MHz
   - Core voltage = 1.2 V, maximum CPU frequency = 1000 MHz
   - Core voltage = 1.2 V, maximum CPU frequency = 1200 MHz
2. Choose the device case temperature for which to the estimate power. The allowable temperature ranges for each of the four devices are listed below:
   - Core voltage = 1.1 V, maximum CPU frequency = 850 MHz
     - Commercial: 0°C to 100°C
   - Core voltage = 1.1 V, maximum CPU frequency = 1000 MHz
     - Commercial: 0°C to 100°C
     - Extended: -40°C to 100°C
   - Core voltage = 1.2 V, maximum CPU frequency = 1000 MHz
     - Commercial: 0°C to 100°C
     - Extended: -40°C to 100°C
   - Core voltage = 1.2 V, maximum CPU frequency = 1200 MHz
     - Commercial: 0°C to 95°C
     - Extended: -40°C to 95°C
3. Enable the appropriate peripherals used for the application being estimated including the mode, frequency, and bus width for that peripheral, if necessary.
4. Fill in the appropriate peripherals or modules % utilization, % writes, and % switching.

The spreadsheet takes the provided information and displays the details of power consumption for the chosen configuration.

As the spreadsheet is being configured, the settings are checked for conflicts, i.e., the peripherals clock frequency out of allowed range, etc. For best results, the information should be entered from left to right starting at the top and moving downward.

3.1 Choosing Appropriate Values

The frequency and bit user values are determined by design and the correct values to enter will be clear. Modules that are completely unused can be disabled in the spreadsheet by selecting the *Disabled* tab in the column labeled *Status*. In order to choose the appropriate values, the utilization, read/write balance, and bit switching require estimation and a good understanding of the user application.

3.1.1 % Utilization

For modules other than the CPU, utilization is simply the percentage of the time the module spends doing something useful, versus being unused or idle. For these peripherals, there are no varying degrees of use, so the value is just the average over time. For example, if the DDR2 performs reads and writes one-quarter of the time and has no data to move for the other three-quarters of the time (though it continues to perform background tasks like refreshes), this would be considered 25% utilization.

The CPU utilization is not as straightforward, because there are varying degrees of use for the CPU. The spreadsheet estimates the CPU activity with respect to three levels of execution: % CPU Utilization, % Control Code Utilization, and % Idle Utilization. The sum of these three execution levels cannot exceed 100%, and only % CPU Utilization and % Control Code Utilization are able to be explicitly entered into the spreadsheet. If the sum of % CPU Utilization and % Control Code Utilization is less than 100%, then the spreadsheet assumes that the remaining percentage is Idle Utilization. The three levels of execution are described in more detail below:

- **% CPU Utilization** is used to represent scenarios with high levels of CPU activity. This corresponds to the case in which all eight instructions fetched by the CPU are executed in parallel each CPU clock cycle, resulting in all eight functional units being active every cycle. Few DSP algorithms will achieve 100% CPU utilization because this requires execution of all eight function units every cycle with no stalls. Even intense applications do not spend all of the time executing such highly parallel code.
- **% Control Code Utilization** is used to represent scenarios with low levels of activity. This could embody some type of task-polling loop or background task. The activity for this case represents the execution of approximately two functional units every clock cycle. This type of code typically accounts for 30% of program execution.
- **% Idle Utilization** is used to represent the case in which the CPU is active, but is not doing useful work (NOP execution). This parameter cannot be explicitly entered into the spreadsheet, and is assumed to be the remaining utilization percentage when % CPU Utilization and % Control Code do not sum to equal 100% (% Idle Utilization = 100% - % CPU Utilization - % Control Code Utilization).

  For more information about the CPU architecture, operation, or instruction set, please see the *TMS320C64x/C64x+ DSP CPU and Instruction Set Reference Guide* (SPRU732).

System level issues may also reduce utilization. Although the spreadsheet will accept 100% utilization for all peripherals, this is not possible in reality. As memory and EDMA bandwidth is consumed, peripheral activity is throttled back due to these bottlenecks, and, therefore, 100% utilization is not achievable. In applications with a lot of memory and/or EDMA usage, individual module utilization numbers should be entered, while keeping this overall limitation in mind.

3.1.2 %Writes

Peripherals that transmit as much as they receive have 50% writes (the spreadsheet will assume the remaining 50% of the time is spent on reads). In some applications, peripherals transmit in only one direction, or have a known balance of data movement. In these cases, the % writes option is not available for configuration. For the peripherals that have the % write configuration, 50% is a typical number that should be used.

3.1.3 % Switching

Random data has a 50% chance that any bit will change from one cycle to the next. Some applications may be able to predict this chance using some *a priori* information about the data set. If there is a property of the algorithm that allows prediction of the bit changes, the application-specific probability can be used. All other applications should use the default number of 50%.

3.2 Peripheral Enabling and Disabling

As mentioned previously, the TMS320C6457 device provides the capability to enable peripherals to reduce power consumption. This can be done by configuring the PSC controller. The spreadsheet also allows you to disable peripherals controlled by the PSC controller to ensure the peripherals' dynamic power is not included if the peripheral is not being used. For more information, see the *TMS320C6457 Fixed-Point Digital Signal Processor Data Manual* (SPRS582) and the *TMS320C6457 Power/Sleep Controller (PSC) User's Guide* (SPRUGL4).

A peripheral can be enabled or disabled in the spreadsheet from the column labeled *Status*. If a peripheral is disabled, the CV_{DD} and I/O power for the peripheral will be 0. If the peripheral is enabled with 0% utilization, the activity power for CV_{DD} and I/O will be 0. However, the peripheral will have baseline power consumption due to enabling/clocking the peripheral. For more information see the *TMS320C6457 Power/Sleep Controller (PSC) User's Guide* (SPRUGL4).

4 Using the Results

The power data presented in this document and the accompanying spreadsheet were collected from devices considered to be at the maximum end of power consumption for production devices. No production units will have average power consumption that exceeds the spreadsheet values. The power consumption estimated by the spreadsheet is the maximum average power consumption. While transient currents may cause power to spike above the spreadsheet values for a small amount of time, over a long period of time, the observed average power consumption will be below the spreadsheet value. Therefore, the spreadsheet values may be used for board thermal analysis and power supply design as a maximum long-term average.

5 Spreadsheet Examples

This section provides examples demonstrating how to choose appropriate values for a particular application. The values used in these examples may be imported into the spreadsheet by clicking the button in the spreadsheet for the corresponding sample application listed below.

5.1 Sample Applications

The examples below provide an estimation of power consumption when the DSP is being used to process data for a sample application. The spreadsheet will provide the estimated total power for core and I/O using the parameters defined below as input.

5.1.1 Idle Power Configuration

In the spreadsheet, there is a button labeled *Idle* that populates the spreadsheet with the following values:

- Device: core voltage = 1.1 V, maximum CPU frequency = 1000 MHz
- Case temperature: 25ºC
- CPU: 1000 MHz frequency, 0% CPU utilization, 0% Control Code utilization
- All peripherals: disabled

The Idle total power for CV_{DD} and I/O = 1.57 Watts.

6 Device: core voltage = 1.1 V, maximum CPU frequency = 1000 MHzTMS320C6457 Voltage Supply Reference List

The voltage supply reference list (Table 1) provides a description of the pins connected to each power rail for power consumption.

Table 1 Voltage Supply Reference List

Group Name	Signal Name	Description
C_CVDD	CV_{DD}	Core supply voltage
C_DVDD_1.8	DV_{DD18}	1.8-V I/O supply voltage
	$PLLV_1$	1.8-V PLL1 supply voltage
	$PLLV_2$	1.8-V PLL2 supply voltage
	V_{DDR18}	1.8-V SRIO/SGMII SerDes regulator supply voltage
C_DVDD_1.1	V_{DDD11}	VDDD: SRIO/SGMII SerDes digital supply voltage
	V_{DDA11}	VDDA: SRIO/SGMII analog supply voltage
	V_{DDT11}	VDDT: SRIO/SGMII SerDes termination supply voltage
C_DVDD_3.3	DV_{DD33}	3.3-V I/O supply voltage
End of Table 1		

7 Release History

Revisions to this document are shown in Table 1-2.

Table 1-2 Release History

Date	Revision	Description
March, 2011	A	• Added HPI core power consumption in Section 2.4. • Updated list of devices and the allowable case temperatures in Section 3.
October, 2009	Initial Release	

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