

AM574x, AM572x, and AM571x Compatibility Guide

ABSTRACT

This application report provides a summary of the differences between the AM574x (Silicon Revision (SR) 1.0), AM572x (SR 2.0 and 1.1), and AM571x (SR 2.0 and 1.0) high-performance, Arm® devices.

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1 Introduction

The AM574x, AM572x, and AM571x series is offered in a FCBGA (760), 23.0 mm × 23.0 mm package. Printed circuit boards can be designed to be compatible with the three families. This application report summarizes the differences in ball assignment, pin multiplexing, and basic features between the three families.

2 Basic Feature Comparison

Figure 1, Figure 2, and Figure 3 show top-level block diagrams of the AM571x, AM572x, and AM574x devices. Table 1 highlights the differences in features between the three devices (number of module instances, processors, accelerators, and supported interfaces).

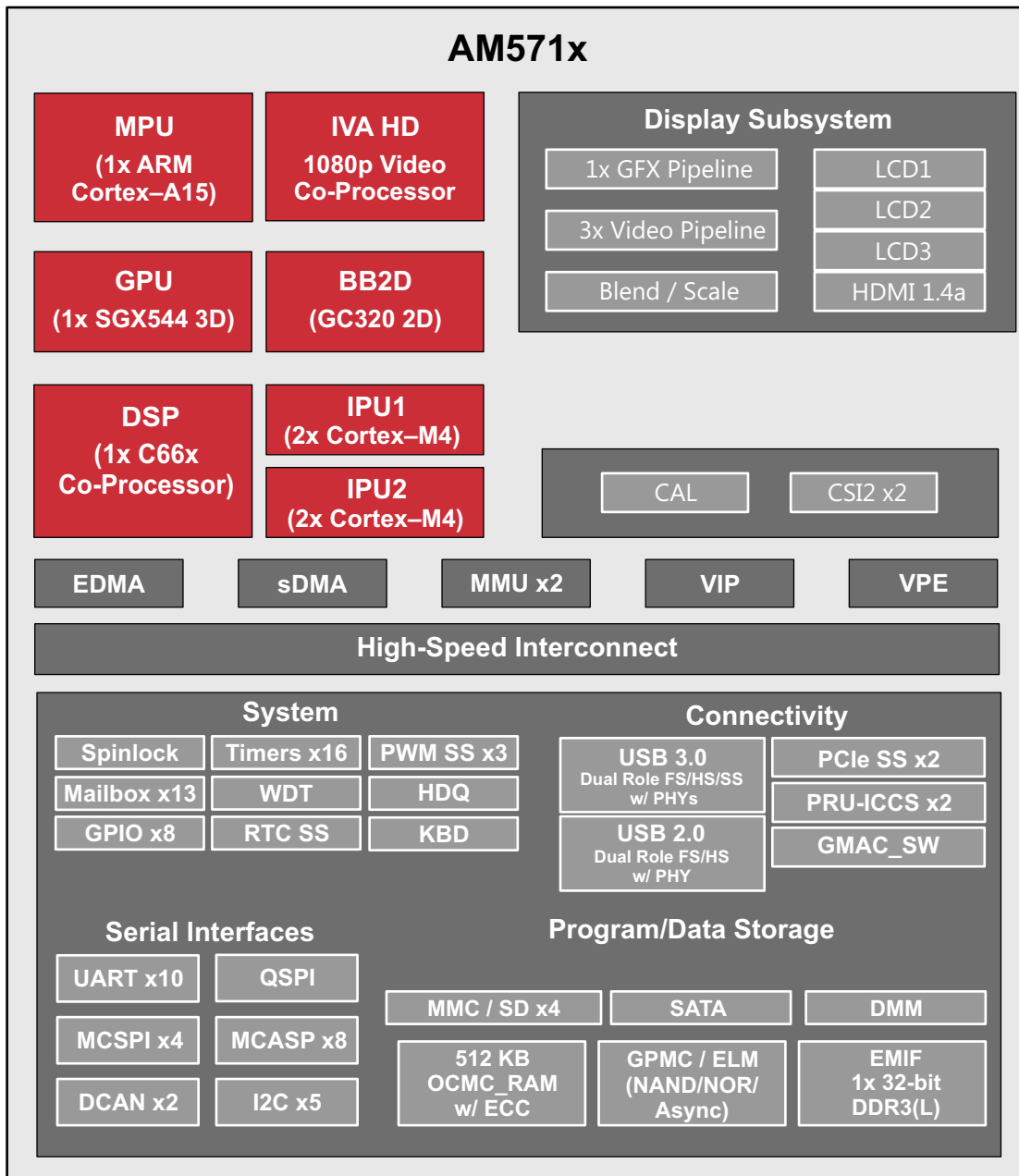


Figure 1. AM571x Block Diagram

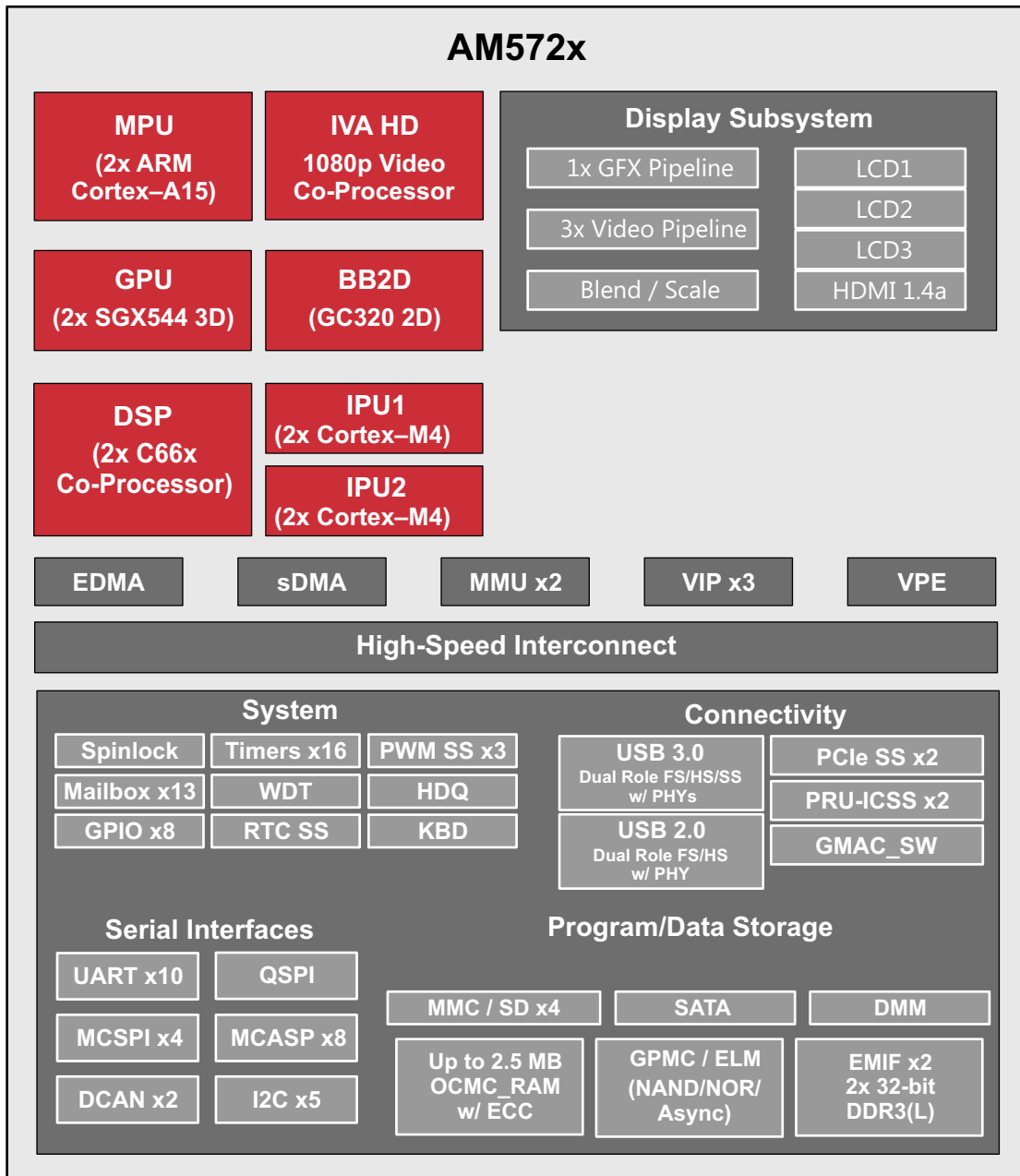
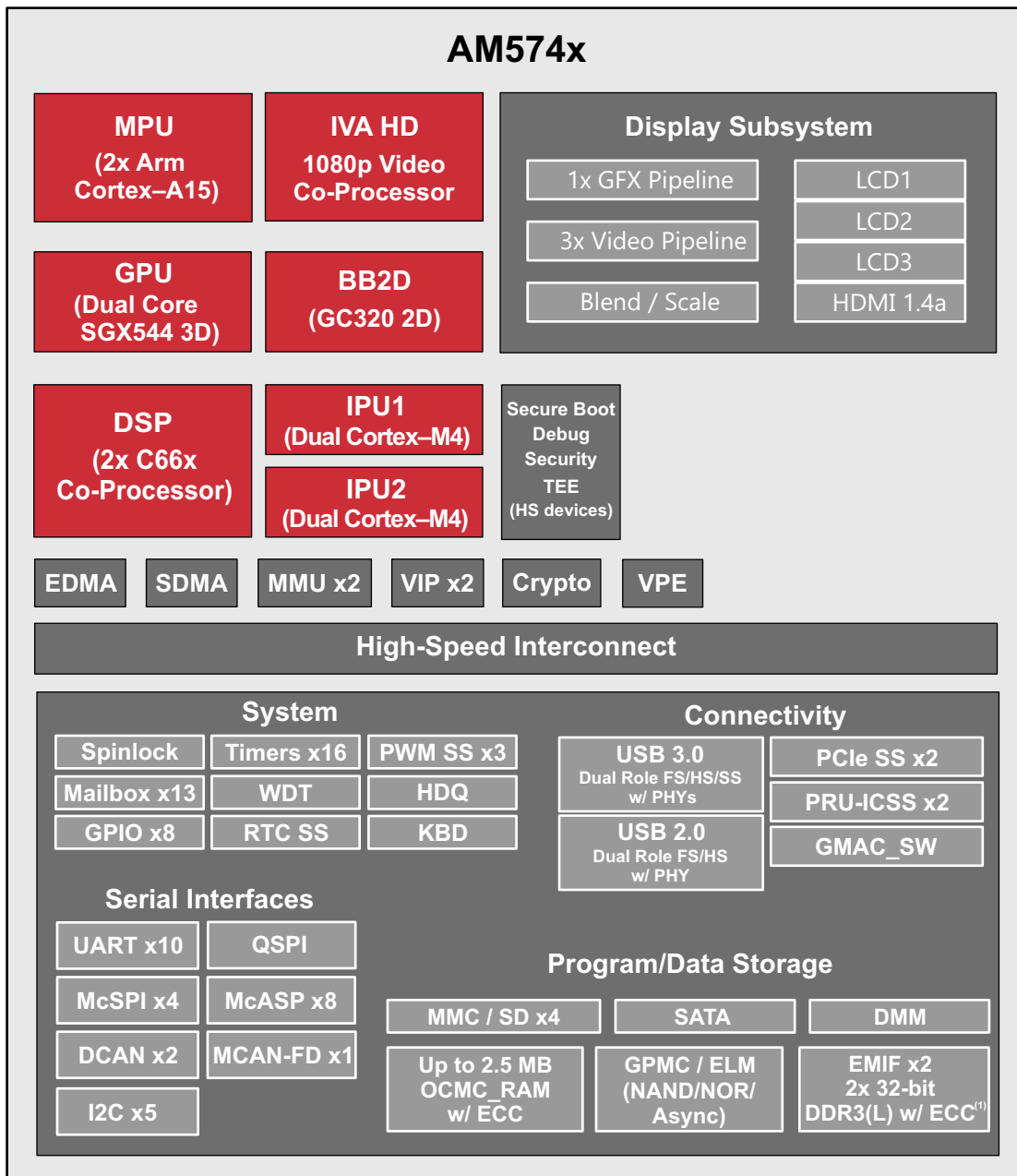


Figure 2. AM572x Block Diagram



intro-001

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(1) ECC is only available on EMIF1.

Figure 3. AM574x Block Diagram

Table 1. Device Comparison

Features		Device			Software Impact	
		AM574x	AM572x	AM571x		
Processors and Accelerators						
Speed Grades		See Section 3.3.1				
Secure Boot (HS devices)		Yes	No	No		
Dual ARM Cortex®-A15 Microprocessor Subsystem	MPU_C0	Yes	Yes	Yes	AM571x: Reduction of cache to 1MB (due to single core). Addition of ECC feature on MPU L2. Enable/disable API provided by ROM code (see Section 3.1.1).	
	MPU_C1	Yes	Yes	No		AM571x: Kernel must recognize uniprocessor.
C66x VLIW DSP	DSP1	Yes (with L1D ECC)	Yes	Yes		
	DSP2	Yes (with L1D ECC)	Yes	No		
GC320 2D Hardware Acceleration Engine	BB2D	Yes	Yes	Yes		
Display Subsystem	VOUT1	Yes	Yes	Yes		
	VOUT2	Yes	Yes	Yes		
	VOUT3	Yes	Yes	Yes		
	HDMI	Yes	Yes	Yes		
Embedded Vision Engine	EVE1	No	No	No		
	EVE2	No	No	No		
Dual ARM Cortex-M4 Image Processing Unit	IPU1	Yes	Yes	Yes		
	IPU2	Yes	Yes	Yes		
Image and Video Accelerator	IVA	Yes	Yes	Yes		
SGX544 3D Graphics Processing Unit	GPU	Dual core	Dual core	Single core		
Video Input Port	VIP1	vin1a	Yes	Yes	Yes	VIP1 primary pins are not available in the AM571x. VIP1 can use the VIP2 pin multiplexing options of the AM572x (see Section 3.4.1).
		vin1b	Yes	Yes	Yes	
		vin2a	Yes	Yes	Yes	
		vin2b	Yes	Yes	Yes	
	VIP2	vin3a	Yes	Yes	No	
		vin3b	Yes	Yes	No	
		vin4a	Yes	Yes	No	
		vin4b	Yes	Yes	No	
	VIP3	vin5a	No	Yes	No	
		vin6a	No	Yes	No	
Video Processing Engine	VPE	Yes	Yes	Yes		

Table 1. Device Comparison (continued)

Features		Device			Software Impact
		AM574x	AM572x	AM571x	
Camera Serial Interface 2 and Camera Adaptation Layer	CSI2_0	No	No	Yes	AM571x: New software development
	CSI2_1	No	No	Yes	
Memory and Storage					
On-Chip Shared Memory (RAM)	OCMC_RAM	2.5 MB	2.5 MB	512 KB	
General-Purpose Memory Controller	GPMC	Yes	Yes	Yes	
DDR3 Memory Controller	EMIF1	DDR3 up to 2 GB, with optional SECCDED	DDR3 up to 2 GB	DDR3 up to 2 GB	AM571x: Remap all memory space to single EMIF
	EMIF2	DDR3 up to 2 GB	DDR3 up to 2 GB	No	
Dynamic Memory Manager	DMM	Yes	Yes	Yes	
Serial ATA	SATA	Yes	Yes	Yes	
Peripherals and Interfaces					
Controller Area Network (CAN) Interface	DCAN1	Yes	Yes	Yes	
	DCAN2	Yes	Yes	Yes	
	MCAN with FD	Yes	No	No	
Enhanced DMA	EDMA	Yes	Yes	Yes	
System DMA	DMA_SYSTEM	Yes	Yes	Yes	
Three-port Gigabit Ethernet Switch	GMAC_SW[0]	MII, RMII, or RGMII	MII, RMII, or RGMII	MII, RMII, or RGMII	
	GMAC_SW[1]	MII, RMII, or RGMII	MII, RMII, or RGMII	MII, RMII, or RGMII	
General-Purpose IOs	GPIO	Up to 247	Up to 247	Up to 215	
Inter-Integrated Circuit Interface	I2C	5	5	5	
System Mailbox Module	MAILBOX	13	13	13	
Multi-Channel Audio Serial Port	MCASP1	16 serializers	16 serializers	16 serializers	
	MCASP2	16 serializers	16 serializers	16 serializers	
	MCASP3	4 serializers	4 serializers	4 serializers	
	MCASP4	4 serializers	4 serializers	4 serializers	
	MCASP5	4 serializers	4 serializers	4 serializers	
	MCASP6	4 serializers	4 serializers	4 serializers	
	MCASP7	4 serializers	4 serializers	4 serializers	
	MCASP8	4 serializers	4 serializers	4 serializers	
MultiMedia Card/Secure Digital/Secure Digital Input Output Interface	MMC1	1x UHSI 4b	1x UHSI 4b	1x UHSI 4b	
	MMC2	1x eMMC 8b	1x eMMC 8b	1x eMMC 8b	
	MMC3	1x SDIO 8b	1x SDIO 8b	1x SDIO 8b	
	MMC4	1x SDIO 4b	1x SDIO 4b	1x SDIO 4b	

Table 1. Device Comparison (continued)

Features		Device			Software Impact
		AM574x	AM572x	AM571x	
PCI Express 2.0 Port with Integrated PHY	PCIe_SS1	Yes	Yes	Yes	
	PCIe_SS2	Yes	Yes	Yes	
Programmable Real-time Unit and Industrial Communication Subsystem	PRU-ICSS1	Yes	Yes	Yes	New features in the AM574x and AM571x: EnDat protocol and Sigma-Delta demodulation. New features in the AM574x, AM572x SR 2.0 and AM571x: CRC support.
	PRU-ICSS2	Yes	Yes	Yes	
Real-Time Clock Subsystem	RTCSS	Yes	Yes	Yes	
Multichannel Serial Peripheral Interface	MCSPI	4	4	4	
HDQ/1-Wire	HDQ	Yes	Yes	Yes	
Quad SPI	QSPI	Yes	Yes	Yes	
Spinlock Module	SPINLOCK	Yes	Yes	Yes	
Keyboard Controller	KBD	Yes	Yes	Yes	
General-Purpose Timers	TIMER	16	16	16	
Watchdog Timer	WD_TIMER	Yes	Yes	Yes	
Pulse-Width Modulation Subsystem (PWMSS)	PWMSS1	Yes	Yes	Yes	
	PWMSS2	Yes	Yes	Yes	
	PWMSS3	Yes	Yes	Yes	
Universal Asynchronous Receiver/Transmitter	UART	10	10	10	
SuperSpeed, Dual-Role-Device Universal Serial Bus (USB3.0)	USB1	Yes	Yes	Yes	
HighSpeed, Dual-Role-Device Universal Serial Bus (USB2.0)	USB2	Yes	Yes	Yes	

3 Module Comparison

This section describes the module differences requiring software updates or development.

3.1 Processors

3.1.1 MPU

AM571x: ECC function added to the Cortex-A15 L2 cache. Device ROM code has updated APIs to allow enabling and disabling configuration of the ECC. For more information, see the *Services for HLOS Support* section in the *AM571x SR 2.0, SR 1.0, and AM570x SR 2.0 Technical Reference Manual* [2].

3.2 Memory Subsystem

3.2.1 GPMC

AM574x: Some additional options are now available for the upper GPMC address pins, at the cost of some vin2 and optional GPMC signal functions. The intention is to better enable cases of concurrent parallel NOR with QSPI and eMMC. New control module bits enable these options in groups of pins (see [Table 4](#)).

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AM571x: Single-load GPMC frequency must stay below 66 MHz (reduced from maximum of 88 MHz) at 3.3 V. The multiload GPMC maximum capacitive load must be less than or equal to 10 pF at 3.3 V for all frequencies up to 66 MHz. To avoid limitations at 3.3 V, GPMC can be used at 1.8 V.

3.2.2 EMIF

- **AM574x:** Support for 667 MHz (DDR3-1333) on two DDR channels (EMIFs). EMIF1 supports DDR ECC (optional).
- **AM572x:** Support for 532 MHz (DDR3-1066) on two DDR channels (EMIFs)
- **AM571x:** Support for 667 MHz (DDR3-1333) on one DDR channel (EMIF)

3.3 Power, Reset, and Clock Management

- **AM574x:** TPS659037 PMIC must be used.
- **AM572x:** TPS659037 PMIC must be used.
- **AM571x:** If board compatibility is desired, TPS659037 PMIC must be used for the design. The TPS65916 PMIC is another solution for the AM571x device, if board compatibility is not required (see [Section 6](#)).

3.3.1 OPPs

[Table 2](#) lists the speed grade maximum frequency.

Table 2. Speed Grade Maximum Frequency

Device Speed	Maximum Frequency (MHz)						
	MPU	DSP	IVA	GPU	IPU	L3	DDR3 and DDR3L
AM574x	1500	750	532	532	212.8	266	667 (DDR3-1333) dual-channel
AM572x	1500	750	532	532	212.8	266	532 (DDR3-1066) dual-channel
AM571x	1500	750	532	532	212.8	266	667 (DDR3-1333) single-channel

3.3.2 Power Rails

See [Table 4](#).

3.3.3 Input Clocks

No difference.

3.3.4 DPLLs

AM571x: DPLL_VIDEO2 is removed. For targets supplied by DPLL_VIDEO2 in the AM572x and AM574x, users must select other options (for example, DPLL_VIDEO1 or DPLL_HDMI). These alternative options are the same as in the AM572x. These clocks include:

- DSS clocks
- GMAC_RFT_CLK
- CLKOUT3_CLK
- TIMER1_GFCLK to TIMER16_GFCLK
- MCASP1_AUX_GFCLK to MCASP8_AUX_GFCLK

3.3.5 Sysboot Pins

- **AM574x:** SYSBOOT15 = 1 disables internal weak pull-down resistors on the MMC2 DAT[x] terminals. For more information, see the *Permanent PU/PD Disabling* section in the [AM574x Sitara™ Processors Silicon Revision 1.0 Technical Reference Manual \[3\]](#).
- **AM572x SR 2.0:** SYSBOOT15 = 1 disables internal weak pull-down resistors on the MMC2 DAT[x] terminals. For more information, see the *Permanent PU/PD Disabling (SR 2.0 only)* section in the [AM572x Sitara™ Processor Silicon Revision 2.0 and 1.1, Technical Reference Manual \[1\]](#).
- **AM571x SR 2.0:** SYSBOOT15 = 0 disables internal weak pull-down resistors on the MMC2 DAT[x] terminals. For more information, see the *Permanent PU/PD Disabling (SR 2.0 only)* section in the [AM571x \(SR2.0, SR1.0\) AM570x \(SR2.1, SR2.0\) Sitara™ Processors Technical Reference Manual \[2\]](#).

3.4 Multimedia Accelerators

3.4.1 VIP

AM574x: VIP3 ports (vin5a and vin6a) are not supported.

AM571x: VIP2 ports and VIP3 ports are not supported. The AM571x VIP1 ports (vin1a and vin1b, vin2a and vin2b) are remapped to the AM572x VIP2 ports (vin3 and vin4 ports) (see [Table 4](#)).

3.4.2 DSS

- **AM572x:** VOUT3 is only qualified for use at 1.8 V. Do not use 3.3 V on VOUT3.
- **AM571x:** VOUT1, VOUT2, and VOUT3 are only qualified for use at 1.8 V. Do not use 3.3 V on VOUT1, VOUT2, and VOUT3. VOUT2 occurs in multiple voltage domains. Do not use VOUT2 on any voltage domains at 3.3 V.

3.5 Peripherals

3.5.1 PRU-ICSS

Table 3 lists the differences between the AM574x, AM572x, and AM571x devices.

Table 3. AM57x ICSS Comparison

Feature	Device			
	AM574x	AM572x SR 2.0	AM572x SR 1.1	AM571x
Unsupported PRU-ICSS signals (compared to AM572x)	pr1_pru0_gpi[20:0] pr1_pru0_gpo[20:0]	NA	NA	pr1_pru0_gpi[20:0]
				pr1_pru0_gpo[20:0]
				pr1_edc_latch1_in
				pr1_edc_sync1_out
pr1_edio_latch_in				
Internal wrapper multiplexing ⁽¹⁾	Yes	No	No	Yes
EnDat 2.2 protocol support	Yes	No	No	Yes (pr2_pru1 only)
Sigma-delta demodulation functionality	Yes	No	No	Yes (pr2_pru0 only)
Six-port Ethernet mode support ⁽²⁾	Yes	No	No	Yes
IEP timer features	16 compare registers in the 64-bit IEP timer	16 compare registers in the 64-bit IEP timer	8 compare registers in the 32-bit IEP timer	16 compare registers in the 64-bit IEP timer
CRC16 function	Yes	Yes	No	Yes

⁽¹⁾ Some devices support an internal wrapper multiplexing that expands the top-level multiplexing of the device. For more details about the PRU-ICSS internal wrapper multiplexing, see the *Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem* chapter in the device-specific TRM.

⁽²⁾ Six-port Ethernet mode provides four, 100MB, Industrial Ethernet ports (using the PRU-ICSS MII_RT peripheral) and two Gigabit (1000 MB) Ethernet ports.

3.5.2 CSI2

- **AM571x:** New modules introduced: Camera Serial Interface 2 (CSI2) and Camera Adaptation Layer (CAL)
- **AM571x:** Optional paths are available to route the CSI2 ports as front-end directly to VIP 1a or 2a ports without passing through memory. This allows inline scaling using VIP hardware scaling, although in this case the maximum pixel clock supported is 133 MHz and 1080p is not possible for this use. This path is enabled with the new control module bit in the CTRL_CORE_VIP_MUX_SELECT register.
- **AM571x:** Optional control module bit that supports view of CAL into memory space to be tiled space. Default is non-tiled. For more information, see the CTRL_CORE_CAL_REG register in the *AM571x SR 2.0, SR 1.0 and AM570x SR 2.0 Sitara™ Processors Technical Reference Manual* [2].

3.5.3 PCIe

- **AM574x:** Dedicated PCIe lane 1 balls
- **AM572x:** Dedicated PCIe lane 1 balls
- **AM571x:** AM572x PCIe lane 1 balls are N.C. Lane 1 can be mapped on USB3.0 balls by the software. Default configuration is the USB3.0 with the same pinout as in the AM572x, that is, PCIe lane 1 is not available by default. For more information, see the *PCIe_SS Port Configuration* table in the *AM571x SR 2.0, SR 1.0 and AM570x SR 2.0 Sitara™ Processors Technical Reference Manual* [2].

3.6 GPIO

AM571x: The following GPIO channels are not supported in the AM571x device, compared to the AM572x and AM574x devices:

- gpio1_[1:0]
- gpio2_[31:30]
- gpio3_[27:0]

4 Package Comparison

The AM574x series is offered in a ABZ FCBGA (760), 23.0 mm × 23.0 mm package. The AM572x and AM571x series are offered in an ABC FCBGA (760), 23.0 mm × 23.0 mm package. The ABZ and ABC packages are pin-to-pin compatible, but mechanically different and have different maximum heights. Additionally, assignment of some of the package balls differs, as described in [Figure 4](#) and [Figure 5](#).

[Figure 4](#) shows a comparison between the AM571x and AM572x devices. The table cells of [Figure 4](#) contain the following:

- Ball name in the AM571x
- Ball name in the AM572x (in brackets)

[Figure 5](#) shows a comparison between the AM574x and AM572x devices. The table cells of [Figure 5](#) contain the following:

- Ball name in the AM574x
- Ball name in the AM572x (in brackets)

For both [Figure 4](#) and [Figure 5](#):

- Empty cells: no difference
- Highlighted cell: a difference in the ball assignment
- Non-highlighted cell: a change to not connected (N.C.)

Also, see [Table 4](#).

	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1			
AH																	NC (pcie_lxp1)	NC (pcie_rxp1)			vssa_csi (vss)	csi2_1_dx2 (vin1b_clk1)	csi2_1_dy1 (vin1a_d3)	csi2_1_dy0 (vin1a_d5)	csi2_0_dx3 (vin1a_d7)	csi2_0_dx4 (vin1a_d4)			AH		
AG																					NC (vin1a_clk0)	csi2_1_dy2 (vin1a_d2)	csi2_1_dx1 (vin1a_d6)	csi2_1_dx0 (vin1a_d11)	csi2_0_dy3 (vin1a_d8)	csi2_0_dy4 (vin1a_d10)	NC (vin1a_d9)		AG		
AF																					NC (vin1a_fld0)	NC (vin1a_eync0)		NC (vin1a_d13)	csi2_0_dy2 (vin1a_d14)	csi2_0_dx2 (vin1a_d12)	csi2_0_dx1 (vin1a_d16)		AF		
AE																					NC (vin1a_hsm0)	NC (vin1a_d0)		NC (vin1a_d21)	NC (vin1a_d18)	NC (vin1a_d17)	csi2_0_dy1 (vin1a_d20)	csi2_0_dx0 (vin1a_d19)	AE		
AD																					NC (vin1a_de0)	NC (vin1a_d1)			NC (vin1a_d15)	csi2_0_dy0 (vin1a_d22)			AD		
AC												ddr1_odt1 (Wakeup1)																		AC	
AB													ddr1_csn1 (Wakeup2)																	AB	
AA													vdda_pcie (vdda_pcie0)																	AA	
Y													NC (cap_vddam_corr0)	NC (cap_vddam_corr3)																Y	
W																														W	
V											NC (vdd_iva)	NC (vdd_iva)																		V	
U	NC (ddr2_casn)	NC (ddr2_ba1)	NC (ddr2_ba2)	NC (ddr2_wen)	NC (ddr2_cke)	NC (ddr2_ba0)	NC (ddr2_a15)				NC (vdd_iva)	NC (vdd_iva)																		U	
T	NC (ddr2_ck)	NC (ddr2_nck)		vdds_ddr1 (vdds_ddr2)	vdds_ddr1 (vdds_ddr2)	NC (ddr2_rasn)	NC (ddr2_a13)			cap_vddam_corr1 (cap_vddam_iva)																				T	
R	NC (ddr2_a2)	NC (ddr2_a3)	NC (ddr2_a1)	NC (ddr2_a0)	NC (ddr2_rst)	NC (ddr2_odt0)	NC (ddr2_a14)			NC (cap_vbbab0_iva)			vdda_ddr (vdda_iva)																	R	
P		NC (ddr2_a8)	NC (ddr2_a11)	NC (ddr2_a6)	NC (ddr2_csn0)	NC (ddr2_a4)	NC (ddr2_a5)	vdds1b_vddr1 (vdds1b_vddr2)	vdds1b_vddr1 (vdds1b_vddr2)	NC (cap_vddam_corr4)			vdda_video (vdda_ddr)	vssa_pil_spara (vssa_gmic_corr)	vdda_corr_gmic (vdda_video)															P	
N	NC (ddr2_a12)	NC (ddr2_a9)				NC (ddr2_a10)	NC (ddr2_vn0)	vdds1b_vddr1 (vdds1b_vddr2)	NC (ddr2_a7)				vdda_mpu_abe (vdda_mpu)																	N	
M	NC (ddr2_dqs3)	NC (ddr2_dqs3)	NC (ddr2_d31)	NC (ddr2_d30)	NC (ddr2_d29)	NC (ddr2_d28)	NC (vdds_ddr2)	NC (vdds_ddr2)	NC (vdds_ddr2)							vdda_par (vdda_abe_par)	vdd_iva (vdd_dspeve)	vdd_iva (vdd_dspeve)	vdd_dsp (vdd_dspeve)	vdd_dsp (vdd_dspeve)											M
L	NC (ddr2_d27)	NC (ddr2_d24)	NC (ddr2_d25)	NC (ddr2_d26)	NC (ddr2_d20)	NC (ddr2_d19)	NC (ddr2_d16)	NC (vdds_ddr2)	NC (vdds_ddr2)																						L
K	NC (ddr2_dqs2)	NC (ddr2_dqs2)				NC (ddr2_dqm2)	NC (ddr2_d22)	NC (ddr2_d18)	NC (ddr2_d17)	cap_vddam_mpu (cap_vddam_mpu2)																				K	
J		NC (vdds_ddr2)	NC (ddr2_d14)	NC (ddr2_d13)	NC (ddr2_d15)	NC (ddr2_d21)	NC (vdds1b_vddr2)	NC (vdds1b_vddr2)	NC (ddr2_d23)	cap_vddam_corr2 (cap_vddam_corr2)																					J
H	NC (ddr2_dqs1)	NC (ddr2_dqs1)	NC (ddr2_d11)	NC (ddr2_d9)	NC (ddr2_d10)	NC (ddr2_d8)	NC (vdds_ddr2)	NC (vdds_ddr2)	NC (vdds_ddr2)																						H
G	NC (ddr2_dqs0)	NC (ddr2_dqs0)	NC (ddr2_d12)	NC (ddr2_d1)	NC (ddr2_dqm1)	NC (vdds_ddr2)	NC (vdds_ddr2)																							G	
F	NC (ddr2_dqm0)	NC (ddr2_d5)	NC (ddr2_d4)	NC (ddr2_d2)	NC (ddr2_d3)																									F	
E	NC (ddr2_d7)	NC (ddr2_d6)	NC (ddr2_d0)		NC (vdds_ddr2)																									E	
D																														D	
C																														C	
B																														B	
A																														A	

Figure 4. Ballmap Differences Between AM571x and AM572x Devices

	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10
AH																			
AG																			
AF																			
AE										vss (vssa_hdmi)						vss (vssa_pcie)			vss (vssa_sata)
AD										vss (vssa_hdmi)						vss (vssa_pcie)			vss (vssa_usb3)
AC																			
AB																		vss (vssa_usb)	
AA																		vss (vssa_usb)	

Figure 5. Ballmap Differences AM574x and AM572x Devices

5 Pin Compatibility

Table 4 lists the detailed differences in ball assignment and pin multiplexing.

Table 4. Pin Compatibility

Ball	Device			PCB Impact
	AM574x	AM572x	AM571x	
Primary Signal Pins				
AH7	vin1b_clk1	vin1b_clk1	csi2_1_dx2	Use CSI2 only when AM571x is populated.
AG7	vin1a_d2	vin1a_d2	csi2_1_dy2	
AG6	vin1a_d6	vin1a_d6	csi2_1_dx1	
AH6	vin1a_d3	vin1a_d3	csi2_1_dy1	
AG5	vin1a_d11	vin1a_d11	csi2_1_dx0	
AH5	vin1a_d5	vin1a_d5	csi2_1_dy0	
AH3	vin1a_d4	vin1a_d4	csi2_0_dx4	
AG3	vin1a_d10	vin1a_d10	csi2_0_dy4	
AH4	vin1a_d7	vin1a_d7	csi2_0_dx3	
AG4	vin1a_d8	vin1a_d8	csi2_0_dy3	
AF2	vin1a_d12	vin1a_d12	csi2_0_dx2	
AF3	vin1a_d14	vin1a_d14	csi2_0_dy2	
AF1	vin1a_d16	vin1a_d16	csi2_0_dx1	
AE2	vin1a_d20	vin1a_d20	csi2_0_dy1	
AE1	vin1a_d19	vin1a_d19	csi2_0_dx0	
AD2	vin1a_d22	vin1a_d22	csi2_0_dy0	

Table 4. Pin Compatibility (continued)

Ball	Device			PCB Impact
	AM574x	AM572x	AM571x	
AG8	vin1a_clk0	vin1a_clk0	N.C.	All other vin1a_* pins: N.C. No impact, do not use the AM572x features on these balls when the AM571x is populated.
AG2	vin1a_d9	vin1a_d9	N.C.	
AF9	vin1a_fld0	vin1a_fld0	N.C.	
AF8	vin1a_vsync0	vin1a_vsync0	N.C.	
AF6	vin1a_d13	vin1a_d13	N.C.	
AF4	vin1a_d15	vin1a_d15	N.C.	
AE9	vin1a_hsync0	vin1a_hsync0	N.C.	
AE8	vin1a_d0	vin1a_d0	N.C.	
AE6	vin1a_d21	vin1a_d21	N.C.	
AE5	vin1a_d18	vin1a_d18	N.C.	
AE3	vin1a_d17	vin1a_d17	N.C.	
AD9	vin1a_de0	vin1a_de0	N.C.	
AD8	vin1a_d1	vin1a_d1	N.C.	
AD3	vin1a_d23	vin1a_d23	N.C.	
AB16	wakeup2	wakeup2	ddr1_csn1	For more information, see the <i>Multiplexed Functions</i> section in this table. Also, RTC-only mode and dual-rank DDR support are not available on the AM57x.
AC17	wakeup1	wakeup1	ddr1_odt1	
AH12	pcie_txn1	pcie_txn1	N.C.	No impact. Do not use PCIe lane 1 on these balls when the AM571x is populated. Instead, Lane 1 can be mapped on USB3.0 balls by the software on the AM571x. For more information, see the <i>PCIe_SS Port Configuration</i> table in the <i>AM571x SR 2.0, SR 1.0 and AM570x SR 2.0 Sitara™ Processors Technical Reference Manual [2]</i> .
AG12	pcie_txp1	pcie_txp1	N.C.	
AG11	pcie_rxn1	pcie_rxn1	N.C.	
AH11	pcie_rxp1	pcie_rxp1	N.C.	
Multiplexed Functions				
B11	vin3a_clk0	vin3a_clk0	vin1a_clk0	Pin muxing used for vin3 and vin4 in the AM572x is mapped on vin1 and vin2 (internal VIP1 pins) in the AM571x. For more information, see the <i>Multiplexing Characteristics</i> table in the <i>AM571x Embedded Applications Processor Data Manual [9]</i> and the <i>Pad Configuration Registers</i> section in the <i>AM571x SR 2.0, SR 1.0 and AM570x SR 2.0 Sitara™ Processors Technical Reference Manual [2]</i> .
B10	vin3a_de0	vin3a_de0	vin1a_de0	
D11	vin3a_fld0	vin3a_fld0	vin1a_fld0	
C11	vin3a_hsync0	vin3a_hsync0	vin1a_hsync0	
E11	vin3a_vsync0	vin3a_vsync0	vin1a_vsync0	
B7	vin3a_d0	vin3a_d0	vin1a_d0	
B8	vin3a_d1	vin3a_d1	vin1a_d1	
A7	vin3a_d2	vin3a_d2	vin1a_d2	
A8	vin3a_d3	vin3a_d3	vin1a_d3	

Table 4. Pin Compatibility (continued)

Ball	Device			PCB Impact
	AM574x	AM572x	AM571x	
C9	vin3a_d4	vin3a_d4	vin1a_d4	
A9	vin3a_d5	vin3a_d5	vin1a_d5	
B9	vin3a_d6	vin3a_d6	vin1a_d6	
A10	vin3a_d7	vin3a_d7	vin1a_d7	
E8	vin3a_d8	vin3a_d8	vin1a_d8	
D9	vin3a_d9	vin3a_d9	vin1a_d9	
D7	vin3a_d10	vin3a_d10	vin1a_d10	
D8	vin3a_d11	vin3a_d11	vin1a_d11	
A5	vin3a_d12	vin3a_d12	vin1a_d12	
C6	vin3a_d13	vin3a_d13	vin1a_d13	
C8	vin3a_d14	vin3a_d14	vin1a_d14	
C7	vin3a_d15	vin3a_d15	vin1a_d15	
F11	vin3a_d16	vin3a_d16	vin1a_d16	
G10	vin3a_d17	vin3a_d17	vin1a_d17	
F10	vin3a_d18	vin3a_d18	vin1a_d18	
G11	vin3a_d19	vin3a_d19	vin1a_d19	
E9	vin3a_d20	vin3a_d20	vin1a_d20	
F9	vin3a_d21	vin3a_d21	vin1a_d21	
F8	vin3a_d22	vin3a_d22	vin1a_d22	
E7	vin3a_d23	vin3a_d23	vin1a_d23	
P7	vin3b_clk1	vin3b_clk1	vin1b_clk1/vin2b_clk1	
N6	vin3b_de1	vin3b_de1	vin1b_de1/vin2b_de1	
M4	vin3b_fld1	vin3b_fld1	vin1b_fld1/vin2b_fld1	
H5	vin3b_hsync1	vin3b_hsync1	vin1b_hsync1/vin2b_hsync1	
H6	vin3b_vsync1	vin3b_vsync1	vin1b_vsync1/vin2b_vsync1	
K7	vin3b_d0	vin3b_d0	vin1b_d0/vin2b_d0	
M7	vin3b_d1	vin3b_d1	vin1b_d1/vin2b_d1	
J5	vin3b_d2	vin3b_d2	vin1b_d2/vin2b_d2	
K6	vin3b_d3	vin3b_d3	vin1b_d3/vin2b_d3	
J7	vin3b_d4	vin3b_d4	vin1b_d4/vin2b_d4	
J4	vin3b_d5	vin3b_d5	vin1b_d5/vin2b_d5	
J6	vin3b_d6	vin3b_d6	vin1b_d6/vin2b_d6	
H4	vin3b_d7	vin3b_d7	vin1b_d7/vin2b_d7	

Table 4. Pin Compatibility (continued)

Ball	Device			PCB Impact
	AM574x	AM572x	AM571x	
D11	vin4a_clk0	vin4a_clk0	vin1a_clk0/vin2a_clk0	
B10	vin4a_de0	vin4a_de0	vin1a_de0/vin2a_de0	
B11	vin4a_fld0	vin4a_fld0	vin1a_fld0/vin2a_fld0	
C11	vin4a_hsync0	vin4a_hsync0	vin1a_hsync0/vin2a_hsync0	
E11	vin4a_vsync0	vin4a_vsync0	vin1a_vsync0/vin2a_vsync0	
B7	vin4a_d0	vin4a_d0	vin1a_d0/vin2a_d0	
B8	vin4a_d1	vin4a_d1	vin1a_d1/vin2a_d1	
A7	vin4a_d2	vin4a_d2	vin1a_d2/vin2a_d2	
A8	vin4a_d3	vin4a_d3	vin1a_d3/vin2a_d3	
C9	vin4a_d4	vin4a_d4	vin1a_d4/vin2a_d4	
A9	vin4a_d5	vin4a_d5	vin1a_d5/vin2a_d5	
B9	vin4a_d6	vin4a_d6	vin1a_d6/vin2a_d6	
A10	vin4a_d7	vin4a_d7	vin1a_d7/vin2a_d7	
E8	vin4a_d8	vin4a_d8	vin1a_d8/vin2a_d8	
D9	vin4a_d9	vin4a_d9	vin1a_d9/vin2a_d9	
D7	vin4a_d10	vin4a_d10	vin1a_d10/vin2a_d10	
D8	vin4a_d11	vin4a_d11	vin1a_d11/vin2a_d11	
A5	vin4a_d12	vin4a_d12	vin1a_d12/vin2a_d12	
C6	vin4a_d13	vin4a_d13	vin1a_d13/vin2a_d13	
C8	vin4a_d14	vin4a_d14	vin1a_d14/vin2a_d14	
C7	vin4a_d15	vin4a_d15	vin1a_d15/vin2a_d15	
F11	vin4a_d16	vin4a_d16	vin1a_d16/vin2a_d16	
G10	vin4a_d17	vin4a_d17	vin1a_d17/vin2a_d17	
F10	vin4a_d18	vin4a_d18	vin1a_d18/vin2a_d18	
G11	vin4a_d19	vin4a_d19	vin1a_d19/vin2a_d19	
E9	vin4a_d20	vin4a_d20	vin1a_d20/vin2a_d20	
F9	vin4a_d21	vin4a_d21	vin1a_d21/vin2a_d21	
F8	vin4a_d22	vin4a_d22	vin1a_d22/vin2a_d22	
E7	vin4a_d23	vin4a_d23	vin1a_d23/vin2a_d23	
V1	vin4b_clk1	vin4b_clk1	vin1b_clk1	
V7	vin4b_de1	vin4b_de1	vin1b_de1	
W2	vin4b_fld1	vin4b_fld1	vin1b_fld1	
U7	vin4b_hsync1	vin4b_hsync1	vin1b_hsync1	

Table 4. Pin Compatibility (continued)

Ball	Device			PCB Impact	
	AM574x	AM572x	AM571x		
V6	vin4b_vsync1	vin4b_vsync1	vin1b_vsync1		
U4	vin4b_d0	vin4b_d0	vin1b_d0		
V2	vin4b_d1	vin4b_d1	vin1b_d1		
Y1	vin4b_d2	vin4b_d2	vin1b_d2		
W9	vin4b_d3	vin4b_d3	vin1b_d3		
V9	vin4b_d4	vin4b_d4	vin1b_d4		
U5	vin4b_d5	vin4b_d5	vin1b_d5		
V5	vin4b_d6	vin4b_d6	vin1b_d6		
V4	vin4b_d7	vin4b_d7	vin1b_d7		
P2	gpio2_20/gpmc_a13/gpmc_a23	gpio2_20	gpio2_20/gpmc_a13/gpmc_a23	<p>New feature in the AM574 and AM571x devices. Enables concurrent parallel NOR with QSPI and eMMC. Alternate mux behind GPMC optional controls and vin2a. For more information, see the <i>Pads Having Capability for Additional Signal Mapping</i> table in the <i>AM574x Sitara™ Processors Silicon Revision 1.0 Technical Reference Manual</i> and <i>AM571x SR 2.0, SR 1.0 and AM570x SR 2.0 Sitara™ Processors Technical Reference Manual</i> [2].</p>	
P1	gpio2_21/gpmc_a14/gpmc_a24	gpio2_21	gpio2_21/gpmc_a14/gpmc_a24		
N2	gpio2_28/gpmc_a15/gpmc_a25	gpio2_28	gpio2_28/gpmc_a15/gpmc_a25		
R6	gpio7_3/gpmc_a16/gpmc_a26	gpio7_3	gpio7_3/gpmc_a16/gpmc_a26		
E1	gpio3_28/gpmc_a17/gpmc_a27	gpio3_28	gpio3_28/gpmc_a17/gpmc_a27		
H7	gpio3_30/gpmc_a18/gpmc_a27	gpio3_30	gpio3_30/gpmc_a18/gpmc_a27		
N1	gpio2_23/gpmc_a19	gpio2_23	gpio2_23/gpmc_a19		
P7	gpio2_22/gpmc_a20	gpio2_22	gpio2_22/gpmc_a20		
N6	gpio2_26/gpmc_a21	gpio2_26	gpio2_26/gpmc_a21		
M4	gpio2_27/gpmc_a22	gpio2_27	gpio2_27/gpmc_a22		
F6	gpio4_12/gpmc_a23	gpio4_12	gpio4_12/gpmc_a23		
D3	gpio4_11/gpmc_a24	gpio4_11	gpio4_11/gpmc_a24		
E6	gpio4_10/gpmc_a25	gpio4_10	gpio4_10/gpmc_a25		
F5	gpio4_9/gpmc_a26	gpio4_9	gpio4_9/gpmc_a26		
G1	gpio3_31/gpmc_a27	gpio3_31	gpio3_31/gpmc_a27		
AD17	wakeup0	wakeup0	new mux option sys_nirq2 behind wakeup0		<p>The sys_nirq2 mux option is not available because the wakeup2 ball has a new function. sys_nirq2 can be muxed (using the new control module bit) to the wakeup0 ball. For more information, see the CTRL_CORE_ALT_SELECT_MUX register in the <i>AM571x SR 2.0, SR 1.0 and AM570x SR 2.0 Sitara™ Processors Technical Reference Manual</i> [2].</p>

Table 4. Pin Compatibility (continued)

Ball	Device			PCB Impact
	AM574x	AM572x	AM571x	
AC16	wakeup3	wakeup3	new mux option dcan2_rx behind wakeup3	The dcan2_rx mux option is not available because the wakeup1 ball has a new function. dcan2_rx can be muxed (using the new control module bit) to the wakeup3 ball. For more information, see the CTRL_CORE_ALT_SELECT_MUX register in the AM571x SR 2.0, SR 1.0 and AM570x SR 2.0 Sitara™ Processors Technical Reference Manual [2].
Power				
G19	dcan1_rx/mcan_rx	dcan1_rx	dcan1_rx	New feature in the AM574x to support MCAN with FD. Alternate mux behind dcan1 and gpio6. For more information, see the <i>Pads Having Capability for Additional Signal Mapping</i> table in the AM574x Sitara™ Processors Silicon Revision 1.0 Technical Reference Manual.
G20	dcan1_tx/mcan_tx	dcan1_tx	dcan1_tx	
E21	dcan2_tx/mcan_tx	dcan2_tx	dcan2_tx	
F20	dcan2_rx/mcan_rx	dcan2_rx	dcan2_rx	
U18, U19, V18, V19	vdd_iva	vdd_iva	N.C.	This supply becomes unused when the AM571x is populated. However, it should still be connected to be compatible with the AM572x and AM574x devices.
J13, K12, K13, L12, M12, M13	vdd_dspeve	vdd_dspeve	vdd_iva	Run IVA at the same OPP as DSP, and the power supply must support sufficient capacity. If a different OPP is desired, plan to isolate onboard (AM572x-only board would not).
K10, K11, L10, L11, M10, M11	vdd_dspeve	vdd_dspeve	vdd_dsp	
AA21, AA22, AB21, AB22, AB24, AB25, AC22, AD26, AG20, AG28, AH27, W16, W27	vdds_dds1	vdds_dds1	vdds_dds1	AM571x: Drive both ddr1 and ddr2 rails with common supply.
T24, T25	vdds_dds2	vdds_dds2	vdds_dds1	
E24, G22, G23, H20, H21, H22, J27, L20, L21, M20, M21	vdds_dds2	vdds_dds2	N.C.	
P20, P21, N21	vdds18v_dds2	vdds18v_dds2	vdds18v_dds1	
J21, J22	vdds18v_dds2	vdds18v_dds2	N.C.	

Table 4. Pin Compatibility (continued)

Ball	Device			PCB Impact	
	AM574x	AM572x	AM571x		
W12	vdda_usb3	vdda_usb3	vdda_csi	Treat 1.8-V analog supplies the same, so that they are interchangeable. If special filtering and handling is desired, apply on both.	
W14	vdda_pcie	vdda_pcie	vdda_usb3		
AA17	vdda_pcie0	vdda_pcie0	vdda_pcie		
AA16	vdda_pcie1	vdda_pcie1	vdda_pcie0		
P15	vdda_gmac_core	vdda_gmac_core	vdda_pll_spare		
P14	vdda_video	vdda_video	vdda_core_gmac		
P16	vdda_ddr	vdda_ddr	vdda_video		
R17	vdda_iva	vdda_iva	vdda_ddr		
N12	vdda_dsp_eve	vdda_dsp_eve	vdda_dsp_iva		
M14	vdda_abe_per	vdda_abe_per	vdda_per		
N16	vdda_mpu	vdda_mpu	vdda_mpu_abe		
U14	vss	vssa_video	vss		Treat grounds the same, so that they are interchangeable. If special filtering and handling is desired, apply on both.
AA10, AH8	vss	vss	vssa_csi		
R15	vss	vss	vssa_video		
AD19, AE19	vss	vssa_hdmi	vssa_hdmi		
AD13, AE13	vss	vssa_pcie	vssa_pcie		
AE10	vss	vssa_sata	vssa_sata		
AA11, AAB11	vss	vssa_usb	vssa_usb		
AD10	vss	vssa_usb3	vssa_usb3		
K19	cap_vddram_mpu2	cap_vddram_mpu2	cap_vddram_mpu	Treat all LDO filter caps the same (cap to vss), so that they are interchangeable. Pins changed to NC on the AM571x do not need a cap, but a cap must be connected to be compatible with the AM572x device.	
L9	cap_vddram_core1	cap_vddram_core1	cap_vddram_core3		
J19	cap_vddram_core2	cap_vddram_core2	cap_vddram_core4		
Y15	cap_vddram_core3	cap_vddram_core3	N.C.		
P19	cap_vddram_core4	cap_vddram_core4	N.C.		
Y16	cap_vddram_core5	cap_vddram_core5	N.C.		
R20	cap_vbbldo_iva	cap_vbbldo_iva	N.C.		
J10	cap_vddram_dspeve1	cap_vddram_dspeve1	cap_vbbldo_iva		
J9	cap_vddram_dspeve2	cap_vddram_dspeve2	cap_vddram_dsp		
T20	cap_vddram_iva	cap_vddram_iva	cap_vddram_core1		
K16	cap_vddram_mpu1	cap_vddram_mpu1	cap_vddram_iva		

6 Considerations For PMIC Compatible Design

An overview of power connections in a compatible PCB is shown in as follows:

- [Figure 6](#): TPS659037x used in GP EVM
- [Figure 7](#): TPS659037x used in Industrial Development Kit

[Table 4](#) lists the ball numbers.

General conditions:

- Power connections can stay the same with the AM571x populated, connections to NC do not have to be removed.
- IVA and DSP must run at the same OPP and voltage on the AM571x device.
- Part of the AM574x and AM572x ddr2 power balls are converted to ddr1 power balls in the AM571x device. Therefore, ddr1 and ddr2 must be connected to same power supply.
- AM571x is redundant, LDO capacitors can be left on NC pins or depopulated for the AM571x device.
- There are some limited swaps between vdda* pins, cap_v* pins, as well as vss and vssa* pins. Treat these pins the same so they are interchangeable on the PCB. For example, consider desired filtering on both. [Figure 6](#) and [Figure 7](#) show an overview of these pins. [Table 4](#) provides a detailed list.

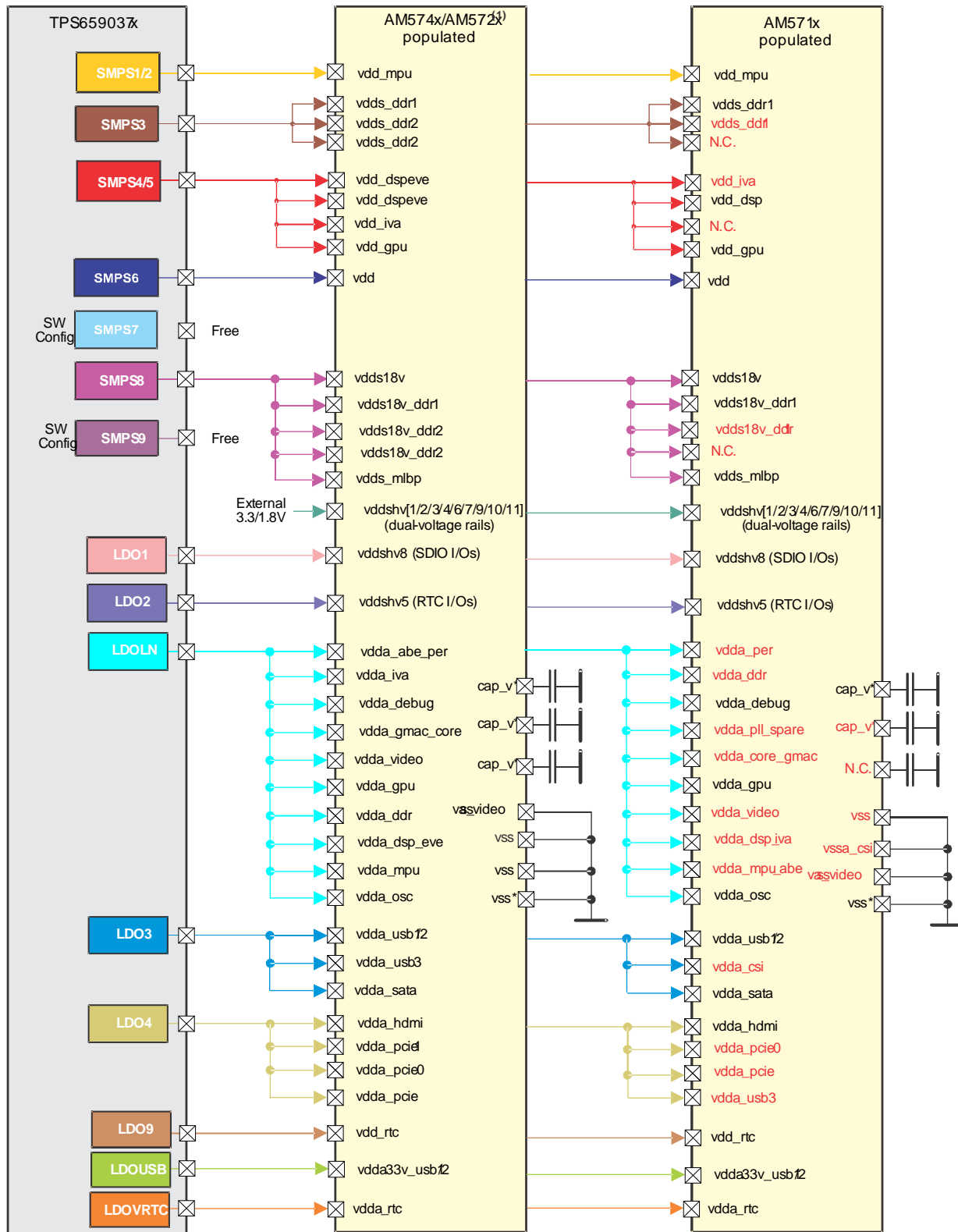
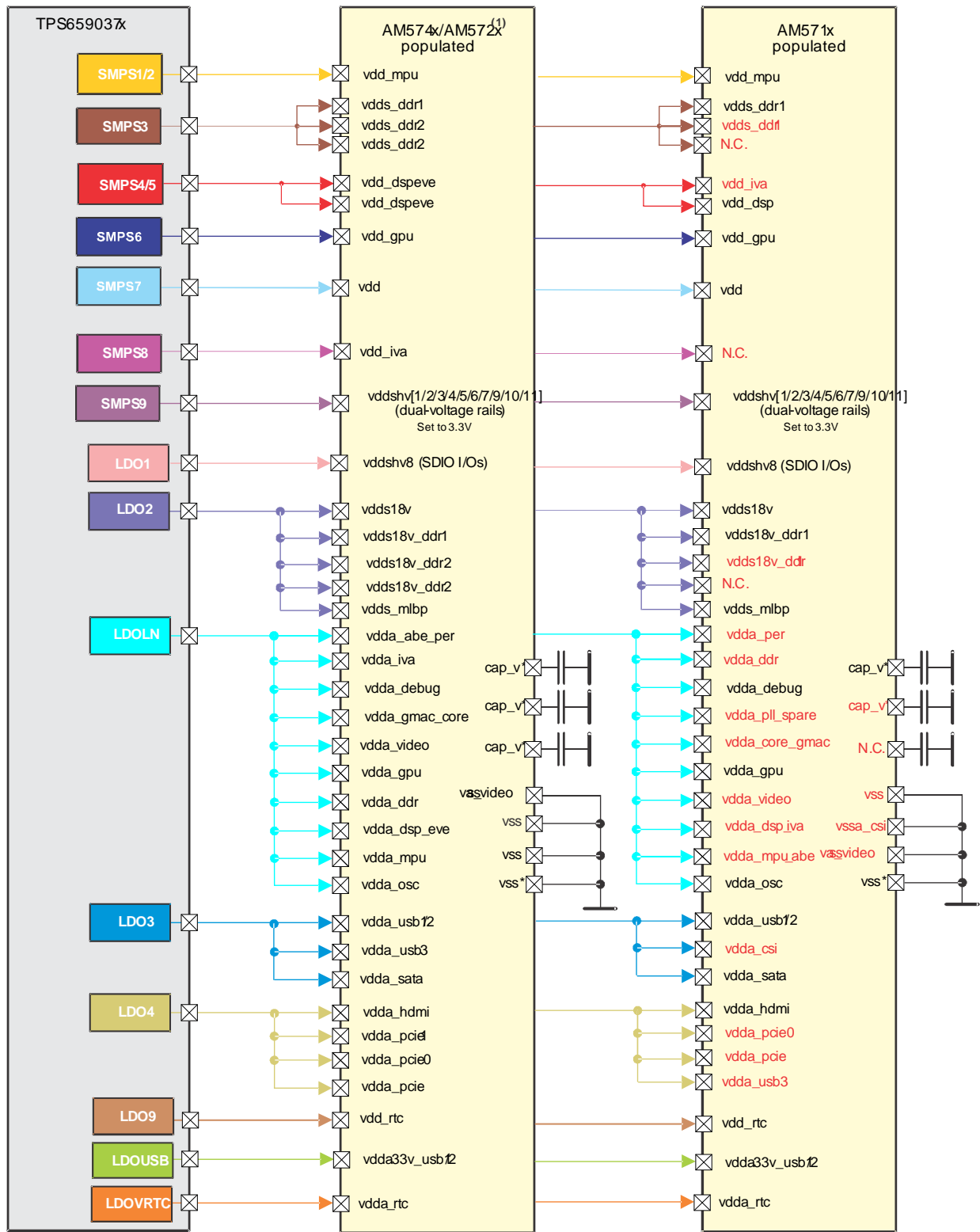


Figure 6. Power Connections For Compatible PCB (TPS659037x – GP EVM)



⊠ ball_name - Ball(s) connected to different net(s) within AM571x device compared to AM572x corresponding ball(s)

[1]: The analog IP ground signals vssa_hdmi, vssa_pcie, vssa_sata, vssa_usb, and vssa_usb3 on AM572x / AM571x have been combined to a common ground on AM574x.

Figure 7. Power Connections For Compatible PCB (TPS659037x – Industrial Development Kit)

7 References

1. Texas Instruments, [AM572x Sitara™ Processor Silicon Revision 2.0 and 1.1, Technical Reference Manual](#)
2. Texas Instruments, [AM571x \(SR2.0, SR1.0\) AM570x \(SR2.1, SR2.0\) Sitara™ Processors Technical Reference Manual](#)
3. Texas Instruments, [AM574x Sitara™ Processors Silicon Revision 1.0 Technical Reference Manual](#)
4. Texas Instruments, [AM571x Sitara™ Processors Silicon Revision 1.0 Silicon Errata](#)
5. Texas Instruments, [TPS659037 User's Guide to Power AM572x and AM571x](#)
6. Texas Instruments, [AM572x Sitara™ Processor Silicon Revision 2.0 Data Manual](#)
7. Texas Instruments, [AM572x Sitara™ Embedded Applications Processor 1.1 Data Manual](#)
8. Texas Instruments, [AM572x Sitara™ Processors Silicon Revision 2.0, 1.1 Silicon Errata](#)
9. Texas Instruments, [AM571x Sitara™ Embedded Applications Processor Data Manual](#)
10. Texas Instruments, [TPS659037 Power Management Unit \(PMU\) for Processor Data Sheet](#)

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from D Revision (January 2018) to E Revision	Page
• Updates were made in Table 1	5
• Update was made to Section 3.2.2	8
• Updates were made in Section 6	21
• Update was made in the figure and title of Figure 6	22
• Update was made in the figure and title of Figure 7	23

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