Application Report
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DRA7xx, AM57xx, TDA2x, TDA3x Spread Spectrum Clocking Configuration

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ABSTRACT

Interfaces which utilize high-frequency clocks to move data from one device to another radiate electromagnetic energy that can possibly interfere with another device in the vicinity. This radiation is called Electromagnetic Interference (EMI). In the USA, the FCC imposes legal limits on EMI emissions from devices. One way to reduce peak levels of EMI is to use spread-spectrum clocking. The basic concept is to introduce controlled variation of the frequency within just a few percent of the nominal value. What this does is to spread out the EMI across a wider range of frequencies instead of concentrating it at the nominal frequency. The key point here is to modulate the clock within the tolerance of the other circuits and devices involved without disrupting communication between those circuits and devices.

This document describes how to achieve reduction of EMI from the DRA7xx, AM57xx, TDA2x, TDA3x VOUTx interface by use of spread spectrum clocking.

The spreadsheet discussed in this application report is available upon request.

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1 About the VOUTx Interface

This section briefly describes the interface on which the Spread Spectrum Clocking (SSC) should be applied.

The SoC has up to three Video Out (VOUT) interfaces, each one of which is capable of driving a 24b LCD output. These interfaces are configured using the Display Controller (DISPC) module registers and can be clocked using one of several DPLLs namely, DPLL_VIDEO1/2, DPLL_PER, and so forth. For more details, see the device-specific technical reference manual. The DPLL is where the Spread Spectrum Clocking is configured. In the next section, the details of how to configure Spread Spectrum Clocking are discussed.

2 Spread Spectrum Clocking Details

SSC refers to the continuous variation of the clock frequency within certain limits with the overall goal of reducing EMI. To understand how SSC works, see Figure 1.

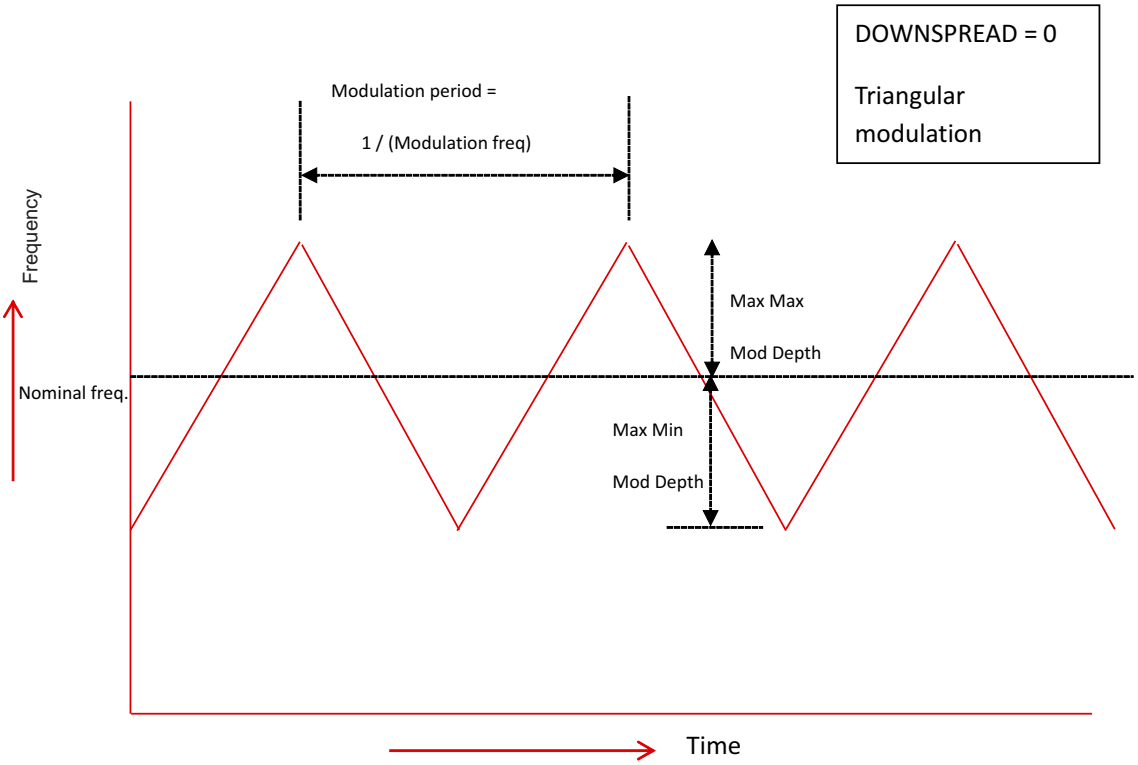

Figure 1. Spread Spectrum Clocking (Triangular profile)

In the example illustrated in Figure 1, at time 0 the frequency starts off a few percent below nominal value (more accurately the frequency difference is the Modulation Depth % x Nominal Frequency). Slowly, the frequency is increased in a linear fashion until it is equal to the same few percent above the nominal value. At this point the frequency is again decreased linearly resulting in a triangular profile of the frequency when plotted against time.

2.1 Characteristics of SSC

SSC characteristics are fully described using the following parameters: modulation rate or frequency, modulation depth, type of spread and modulation profile. Each of these characteristics is described briefly in the following sections.

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2.1.1 Modulation Rate

The modulation period as shown above is the time required to cycle the frequency from an initial value (an arbitrary point in the above curve) through all the different values along the modulation profile and finally back to the initial value. The modulation rate is the inverse of this period. Typical values range in a few tens of kHz.

For example, a modulation rate of 30 kHz implies it takes 33.3 µs for the clock frequency to start at say its original value (say 50 MHz), cycle through all the different values in the modulation profile and return to its original value of 50 MHz.

2.1.2 Modulation Depth

The modulation depth refers to the maximum variation in frequency as a percentage of the target frequency. Typical values are between 1%-3%. For example, a modulation depth of 1% refers to the fact that the frequency of a 50 MHz clock will be varied at max by 0.5 MHz. The type of spread determines how the modulation depth is applied to the baseline frequency.

2.1.3 Type of Spread

The frequency variation can be affected only on the negative side (lower frequency) or both positive (higher frequency) and negative sides. When it is varied on both sides equally it is referred to as center spread. When it is varied on the negative side only, it is referred to as down spread.

The SoC can support both center spread and down spread.

CAUTION

Center spread should be used with caution because it increases the highest frequency of the interface above the nominal value. Care should be taken that the interface is designed to handle this slightly higher frequency. On the other hand, down spread results in an average frequency that is less than the nominal frequency.

2.1.4 Modulation Profile

The modulation profile refers to the shape of the curve describing the variation of the frequency. Conventional profiles include sinusoidal, triangular, Hershey-Kiss.

The SoC supports triangular modulation.

2.2 DPLL SSC Implementation Details

NOTE: It is assumed that the reader is familiar with the configuration of the DPLL M and N values to achieve a certain output frequency. For more details, see the device-specific technical reference manual.

Figure 2 shows a highly simplified implementation diagram of DPLL_VIDEO1.

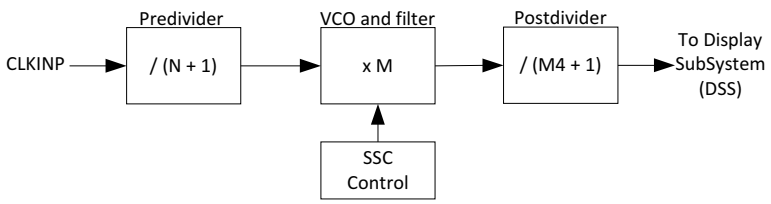

Figure 2. DPLL_VIDEO1 Clocking

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In summary, SSC is accomplished by varying M in small steps. Each step is applied at the rate of REFCLK. Since M is varied in a triangular pattern, this causes the frequency to also vary in a triangular fashion.

2.2.1 Registers Used in Configuring SSC

NOTE: Only use of DPLL_VIDEO1 is approved for use with Spread Spectrum Clocking. Use of other DPLLs is neither approved nor recommended.

Table 1 highlights the registers involved in configuration of SSC in DPLL_VIDEO1.

Table 1. SSC Related Register Fields

Register Name	Address (in the L3 view)	Description of Various Fields		
		Bit No.	Name	Description
DPLL_VIDEO1_L3_MAIN_PLL_SSC_CONFIG1	0x58004318	0	EN_SSC	Spread Spectrum Clocking enable
				0x0: Spread Spectrum Clocking disabled
				0x1: Spread Spectrum Clocking enabled
		2	DOWNSPREAD	Type of spread
				0x0: Center spread
				0x1: Down spread
		All other bits reserved		
DPLL_VIDEO1_L3_MAIN_PLL_SSC_CONFIG2	0x5800431c	19:0	DELTAM	DeltaM Control for SSC. Split into integer and fractional parts.
				- Bits [19:18] define the integer part
				- Bits [17:0] define the fractional part
		29:20	MODFREQDIVIDER	Modulation Frequency Divider (ModFreqDivider) control for SSC. The ModFreqDivider is split into Mantissa and Exponent where:
				ModFreqDivider = Mantissa *
				2^Exponent).
				- Bits [29:23] define the Mantissa
				- Bits [22:20] define the Exponent
		All other bits reserved		

2.2.2 SSC Configuration

Assume the desired modulation frequency is Fm and desired modulation depth is Md, as shown in Figure 2.

REFCLK – Pre-divided reference clock input for the DPLL.

M4 – Post divider whose output goes to the DSS module.

2.2.2.1 Configuring Modulation Frequency

The modulation frequency Fm is configured in the DPLL as a ratio of REFCLK/4 using the register field MODFREQDIVIDER.

Where,

$$MODFREQDIVIDER = REFCLK / (4 \times Fm) \quad (1)$$

MODFREQDIVIDER is split into 7b MODFREQDIVIDERMantissa and 3b MODFREQDIVIDERExponent. To describe the relationship (see Equation 2):

$$MODFREQDIVIDER = MODFREQDIVIDERMantissa * 2 \wedge MODFREQDIVIDERExponent \quad (2)$$

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As a rule, the mantissa must always be maximized and the exponent minimized in Equation 2. For example, if a value of 20 is desired, then mantissa is 20 and the exponent is 0. As another example, if a value of 150 is desired, then mantissa = 75 and the exponent = 1 (so as to maximize exponent).

If Equation 1 results in a value of MODFREQDIVIDER that cannot be expressed using Equation 2, the value must be rounded off to get the closest value possible to the desired modulation rate.

2.2.2.2 Configuring Modulation Depth

The modulation depth is configured using the register field DELTAM. The modulation depth Md can be thought of as the percentage change in M. In other words,

Md = *dM/M*, (where dM is the total change applied by the DPLL to M)

$$\Rightarrow dM = M \times Md \tag{3}$$

The DPLL applies the step change to M at the rate of REFCLK. The following equations also apply.

$$dM = MODFREQDIVIDERMantissa \times 2 \text{ ^ } MODFREQDIVIDERExponent \times dMStep \tag{4}$$

(when MODFREQDIVIDERExponent <=3)

$$dM = 8 \times MODFREQDIVIDERMantissa \times dMStep \tag{5}$$

(when MODFREQDIVIDERExponent >3)

Utilizing Equation 3,

$$dMStep = (M \times Md) / (MODFREQDIVIDERMantissa \times 2_{MODFREQDIVIDERExponent} \tag{6}$$

(when MODFREQDIVIDERExponent <=3)

$$dMStep = (M \times Md) / (8 \times MODFREQDIVIDERMantissa) \tag{7}$$

(when MODFREQDIVIDERExponent >3)

dMStep is split into an integral part and a fractional part. The integral part is controlled by a 2b value dMStepInteger. The 18b fractional part is called dMStepFraction.

Where,

$$dMStepInteger = Integral\ portion\ of\ dMStep\ (upper\ 2b\ of\ the\ 20b\ DELTAM\ field) \tag{8}$$

$$dMStepFraction = 2^{18} \times dMStepFraction\ (lower\ 18b\ of\ the\ 20b\ DELTAM\ field) \tag{9}$$

When DOWNSPREAD = ON, the actual modulation depth is twice of value configured above. There is no frequency spread on the higher side except the overshoot error as described in further sections.

2.2.2.3 Final steps

After arriving at the values of DELTAM and MODFREQDIVIDER, the final step involves writing these values into the register, choosing the type of spread and enable SSC using EN_SSC bit.

Choosing the type of spread (Down Spread or Center Spread) is really a function of the application and the maximum frequency that can be supported by the interface. Remember that the peak modulated frequency shall be higher than the nominal frequency if SSC is enabled with center spread.

CAUTION

Two things must be ensured when using center spread:

- Target device is capable of communicating with the SoC at the higher and lower peak modulation frequencies.
- Highest frequency of the clock after SSC must still be less than the maximum frequency allowed in the data sheet for this interface. The overshoot of 20% on the modulated depth must also be factored in while computing the highest possible frequency.

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SSC can be reconfigured before or after the DPLL has been previously locked with or without SSC.

However, if the SSC values are reconfigured while DPLL is locked, after writing the values and reenabling SSC, the DPLL must be relocked.

In order to check whether the SSC was correctly enabled, the following two checks must be used:

- DPLL must lock correctly which can be checked using the PLL_LOCK bit in the PLL_STATUS register.
- DPLL must acknowledge turning on SSC which can be checked using the SSC_EN_ACK bit in the PLL_STATUS register.

2.2.3 Restrictions on the SSC Configuration

2.2.3.1 Supported Configurations

As stated before, only use of DPLL_VIDEO1 for spread spectrum clocking is supported.

Table 2 lists the supported configurations.

Table 2. SSC Configurations Supported

Parameter	Min	Max	Unit
Modulation depth	0.5	3.0	%
Downspread	Both center spread and down spread are supported		
Modulation rate	30	100	kHz

2.2.3.2 Additional Requirements

- Fm must always be less than REFCLK / 70.
- There is an overshoot on the frequency spread by up to +20%. In other words, the frequency on the positive side should, in the worst case, be 20% higher than the programmed spread. For example, if modulation depth was configured to 1% while DOWNSPREAD = OFF, with nominal frequency = 50 MHz. Instead of the maximum frequency being 50.5 MHz, it will be 50.6 MHz.
- If DOWNSPREAD is OFF then the conditions below must be met:
  - M x (1 – Md) > 20
  - M x (1 + Md) < 2045
- If DOWNSPREAD is ON then the conditions below must be met:
  - M x (1 – 2 * Md) > 20
  - M < 2045
- Lower 18b of DELTAM should be configured to less than 98,000. If a value higher is needed, by reworking N (subsequently M) it may be possible to achieve the same effect by increasing the reference clock frequency.

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2.2.4 Example Application

A user has determined that she is encountering excess EMI in her 50 MHz application. She has already configured the DPLL_VIDEO1 with parameters as shown below.

- CLKINP = 20 MHz
- N = 3
- M = 200
- M4 = 19

It was decided that a modulation depth of 1% and Center Spread at a rate of 33 kHz would be sufficient to get the required EMI benefit.

Below are the steps to derive the values:

1. Is the desired modulation rate between 30 kHz and 100 kHz? - Yes.
2. Is the desired modulation depth between 0.5% and 3% (before factoring for down spread)? - Yes
3. Determine whether the desired modulation rate is even possible. Check whether 33 kHz is less than REFCLK/70, for example, 5 MHz/70 = 71.4 kHz. Yes.
4. Find out whether MODFREQDIVIDER = REFCLK / (4 x Fm), for example, 5 MHz / (4 x 33 kHz) = 37.8 rounded to 38. Therefore, MODFREQDIVIDER = (mantissa = 38, exponent = 0).
5. Find out DELTAM. Use Equation 6 since exponent = 0, for example, (200 * 0.01) / 38 = 0.05263. So integral part dMStepInteger = 0 and dMStepFraction = 2^18 x 0.05263 = 13797.05 rounded to 13797.
6. Check the constraints.
   a. Is dMStepFraction <98000. - Yes.
   b. Since DOWNSPREAD = OFF, 200 x (1 – 0.01) > 20 and 200 x (1 + 0.01) < 2045. Yes and yes.
7. All constraints appear to be satisfied. Final values are MODFREQDIVIDER = (mantissa = 38, exponent = 0) and DELTAM = 13797.

2.2.5 Spreadsheet to Configure SSC

The spreadsheet can be downloaded to automatically configure the SSC. It also checks all of the restrictions stated above to ensure the configuration is valid. The spreadsheet discussed in this application report is an excel file (contained in a zip file) that is located at the following URL **?????**.

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 2015) to A Revision	Page
• Updated Jacinto to DRA7xx, AM57xx, TDA2x, TDA3x in Title and throughout document.	1

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