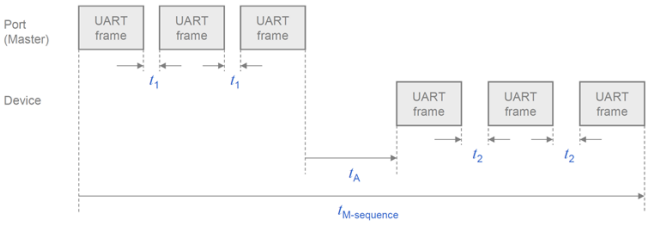
Flexible Timing Configuration with IO-Link Master Frame Handler

Thomas Schneider

IO-Link is a serial, bi-directional, point-to-point protocol and interface standard for sensors and actuators in factory automation applications. An IO-Link system consists of an IO-Link master and IO-Link devices, including sensors, actuators, RFID readers, I/O modules, and so forth. The IO-Link master enables data exchange with IO-Link devices from different manufacturers. These interactions of the master and its devices are characterized by several time constraints that apply to the UART frame and the master and device message transmission times. Communication between a master port and its associated device takes place in a fixed schedule called the M-sequence time. Figure 1 demonstrates the timings of an M-sequence consisting of a master port message and a device message. The device needs to respond to the master within the response time of the device t_A and not exceeding the maximum UART frame transmission delay t_2.

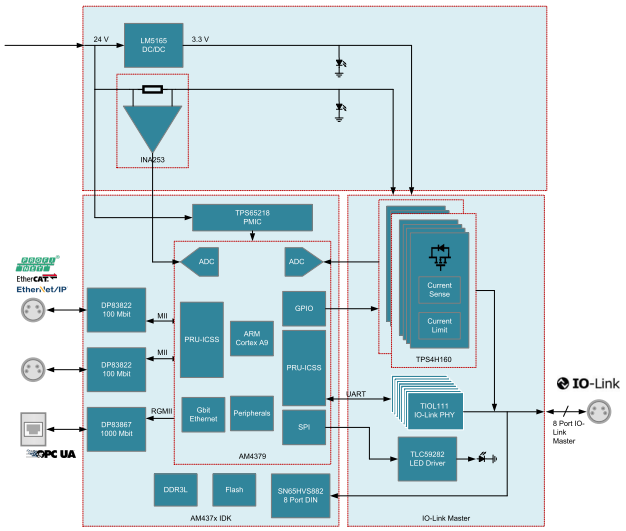
Figure 1. IO-Link Timing



Usually a frame handler is used to execute most of the low level communication tasks to decrease the load on the processor of the IO-Link master. Often, this frame handler is implemented already in a semiconductor device together with the PHY. As the frame handler implementation is fixed in this case in hardware, this makes it inflexible to react on the different timing behaviors of the IO-Link devices from different manufacturers. According to the IO-Link specification, the time t_A needs to be less than 10 T_{Bit} and t_2 needs to be less than 3 T_{Bit}, where T_{BIT} = 1 / (transmission rate). For example, this might be violated if an inductive coupler device is between the master and the device communication line and adding some delay to the communication. A frame handler with fixed timing limits might not be able to continue with the IO-Link communication in this case. TI's solution to implement the frame handler in software using the programmable real time unit and industrial communications subsystem (PRU-ICSS) of the Sitara™ processor family makes it much more flexible to react on the different timing behaviors. This flexible timing configuration makes it possible to also communicate in these special use cases. Not only can the time t_A and t_2 be adjusted during run-time, but also the delay time while establishing Master port communication T_{DMT} can be adjusted as needed.

Figure 2 shows the block diagram of an 8 Port IO-Link Master Reference Design (TIDA-010016) where the frame handler is implemented in software using the PRU.

Figure 2. TIDA-010016 Block Diagram

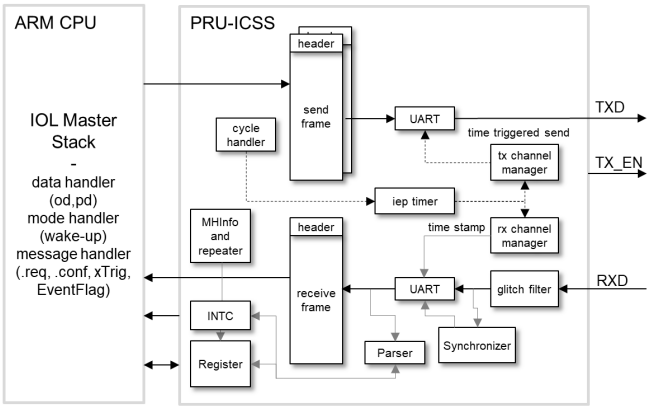


Implementation

For the IO-Link master frame handler implementation with a flexible timing configuration, one of TI's Sitara processors with the integrated PRU-ICSS has been used. The PRU-ICSS is a specialized sub-processor within some of TI's Sitara processors. It is designed to complete most instructions in a single cycle and offers deterministic behavior of those. This PRU-based frame handler enables a very flexible way of timing and time synchronization and is almost free of jitter. It replaces hardware UARTs by a software implementation and eliminates the need for external processing hardware. With one PRU up to 8 IO-Link master ports can be realized. As one ICSS module of the Sitara processor consists out of two PRUs, up to 16 IO-Link master ports can be realized with one ICSS module. All ports support independent cycle time from 400 µs up to 132 ms in 100 µs steps. At 400 µs, a maximum payload of eight bytes is supported. The double send buffer

minimizes t_{idle} time and offloads the host timing. Synchronous start of selected channels is supported without any jitter and latency between the channels. Figure 3 shows the IO-Link master PRU frame handler. The often available second ICSS module on the Sitara processor can be used to process something else, like real-time Ethernet.

Figure 3. IO-Link Master – PRU Frame Handler

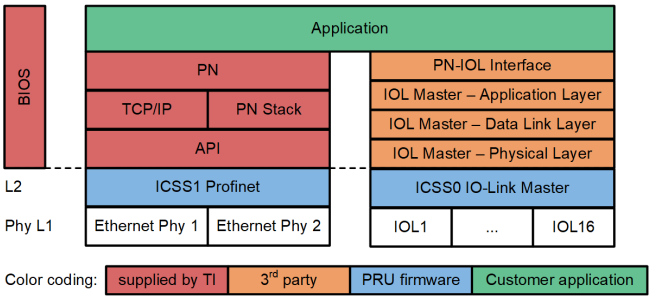


The IO-Link master PRU frame handler driver is part of the RTOS Processor SDK for Sitara AM437x and AMIC120 PROCESSOR-SDK-RTOS-AM437X. The driver supports the following major functionalities:

- Standard APIs to initialize, de-initialize, and control the common Software IP driver
- Configuration and control of the PRU frame handler firmware to handle the messages transferred between the IO-Link master and device
- Timer and interrupt driven IO-Link communication between IO-Link master and device to meet the timing requirement of IO-Link master protocol

In addition, a sample IO-Link master stack interface layer is provided in the IO-Link master demo application to provide an interface between the IO-Link master stack and the driver. Figure 4 shows an IO-Link master integration example with Profinet. ICSS0 is used for IO-Link and ICSS1 is used for Profinet.

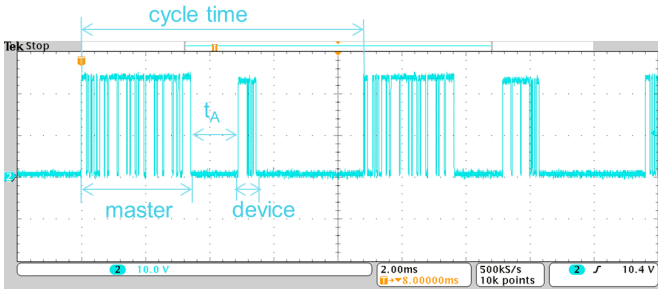
Figure 4. PRU-ICSS IO-Link Master Project Example



Test Results

For test purposes, an inductive coupler device is used. Inductive coupler devices are placed between an IO-Link master and an IO-Link device to transfer power and IO-Link data contactlessly across an air gap, adding some delay to the response time t_A of the IO-Link device. In the test case, an IO-Link device with a transmission rate of 38.4 kbit/s (COM2) is used. Figure 5 shows the measured response time t_A which is 57 T_{BIT}.

Figure 5. Measured Response Time t_A of the IO-Link Device



A standard IO-Link master frame handler implementation in hardware is not be able to communicate with an IO-Link device with a response time of 57 T_{BIT} as it is not flexible enough to adjust the timing. Only the flexible timing configuration with the IO-Link master frame handler implemented in software using the PRU makes it possible to still communicate with IO-Link devices in these special use cases.

Table 1. Alternative Device Recommendations

DEVICE	OPTIMIZED PARAMETERS	PERFORMANCE TRADE-OFF
AM4x	ARM Cortex-A9 Up to 1000 MHz; 2x PRU-ICSS	
AMIC120	2x PRU-ICSS	ARM Cortex-A9 Up to 300 MHz
AMIC110		ARM Cortex-A9 Up to 300 MHz; 1x PRU-ICSS

References

Texas Instruments, *Sitara AM4x Processors*

Texas Instruments, *8 Port IO-Link Master Reference Design (TIDA-010016)*

IO-Link, *IO-Link Interface and System Specification*

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