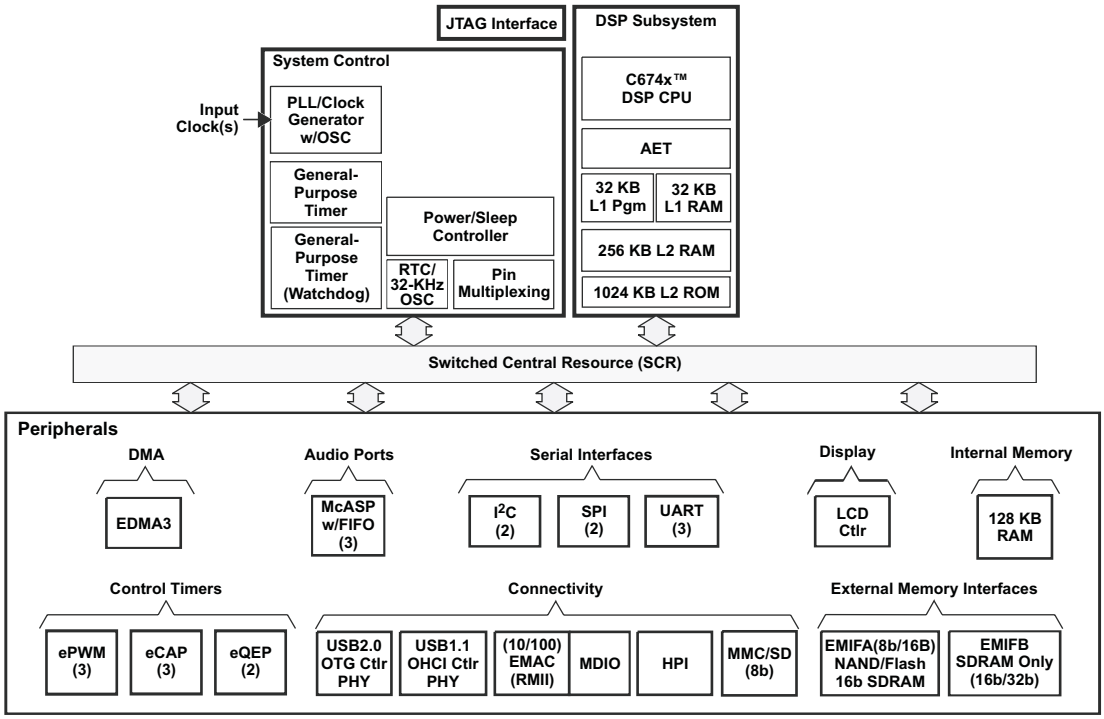
1 Key Message

The C674x Floating-point Processor generation combines a new level of performance / precision and dynamic range with high power efficiency and system integration. The C674x processors are completely code compatible with other C67x processors.

1.1 Key Features

- **Power Management / Power Savings**
  - **Supports Individual Clock Enable/Disable Control for DSP and Peripherals**
  - **Real Time Clock (RTC) With Crystal Input, Separate Clock Domain, Separate Power Supply**
- **200-, 300-MHz C674x™ Floating Point VLIW DSP Core**
  - **8 Highly Independent Functional Units**
  - **64 General-Purpose Registers (32 Bit)**
  - **Instruction Packing Reduces Code Size**
  - **Hardware Support for Modulo Loop Operation**
  - **Protected Mode Operation**
- **C674x Instruction Set Features**
  - **Superset of the C67x+™ and C64x+™ ISAs**
  - **1600/1200, 2400/1800 C674x MIPS/MFLOPS**
  - **Byte-Addressable (8-/16-/32-/64-Bit Data)**
  - **8-Bit Overflow Protection**
  - **Bit-Field Extract, Set, Clear**
  - **Normalization, Saturation, Bit-Counting**
  - **Compact 16-Bit Instructions**
- **C674x Two Level Cache Memory Architecture**
  - **Flexible RAM/Cache Partition (L1 and L2)**
- **128K-Byte Internal RAM Shared Memory**
- **Comprehensive System-Wide Security**
- **Applications: Range from Professional Audio to Audio Conferencing**

1.2 Functional Block Diagram



Note: Not all peripherals are available at the same time due to multiplexing.

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2 Peripherals

Table 2-1. Peripheral Description

Peripherals[1]	No	Description
EMIFB	1	32-Bit or 16-Bit SDRAM with 256MB address space.
EMIFA	1	NOR, NAND (8-/16-Bit-Wide Data), 16-Bit SDRAM with 128MB address space.
Flash Card Interface	1	Multi Media Cards (MMC), Secure Digital Cards (SD) and SDIO interfaces supported.
EDMA3	1	32 independent DMA channels, 8 Quick DMA (QDMA) channels, 2 Transfer controllers, Programmable transfer burst size (16/32/64 bytes).
Timers	2	64-Bit General Purpose (configurable as 2 separate 32-bit timers, 1 configurable as Watch Dog).
UART	3	One with RTS and CTS flow control
SPI	2	Each with one hardware chip select, Master/Slave. Supports 3-, 4-, and 5- pin operation.
I^2C	2	Both Master/Slave. Supports up to 400 Kbps.
Multichannel Audio Serial Port [McASP]	3	Each with transmit/receive, FIFO buffer, 16/12/4 serializers
10/100 Ethernet MAC [EMAC] with Management Data I/O [MDIO]	1	RMII Interface
Enhanced Pulse Width Modulator (ePWM)	3	6 Single Edge, 6 Dual Edge Symmetric, or 3 Dual Edge Asymmetric Outputs.
Enhanced Capture Module [eCAP]	3	32-bit capture inputs or 3 32-bit auxiliary PWM outputs.
Enhanced Quaduature Encoded Pulse Module [eQEP]	2	32-bit QEP channels with 4 inputs/channel.
Universal Host Port Interface [UHPI]	1	16-bit multiplexed address/data
USB 2.0	1	High-Speed OTG Controller with on-chip OTG PHY (supports Host, Device and OTG modes).
USB 1.1	1	Full-Speed OHCI (as host) with on-chip PHY.
General-Purpose Input/Output Port	1	Up to 128 GPIO pins
LCD Controller	1	Supports low end 8-bit character based displays, mid-range, 1/4 VGA color, rasterized graphical displays and high end LCD display
Real Time Clock [RTC]	1	32 KHz oscillator and seperate power rail. Provides time and date tracking and alarm capability.
PLL Controller 0	1	Supplies the clocks to the DSP and most of the system peripherals.

(1) Not all peripheral pins are available at the same time due to multiplexing.

3 Key Electrical Characteristics

			MIN	NOM	MAX	UNIT
CVDD	Supply voltage, Core (CVDD, RTC_CVDD, PLL0_VDDA , USB0_VDDA12, RVDD)		1.14	1.2 or 1.26	1.32	V
DVDD	Supply voltage, I/O, 1.8V (USB0_VDDA18, USB1_VDDA18)		1.71	1.8	1.89	V
	Supply voltage, I/O, 3.3V (DVDD, USB0_VDDA33, USB1_VDDA33)		3.15	3.3	3.45	V
VSS	Supply ground (VSS, USB0_VSSA33, USB0_VSSA, PLL0_VSSA, OSCVSS)		0	0	0	V
P_{Typ}	Typical Power Consumption. Includes static and active power for both Core and I/O supplies	Use Case 1 : 300 MHz; DSP at 1.2 CVDD.		483(1)		mW
T_A	Operating ambient temperature range	Default	0		70	°C
		A version	-40		105	°C
T_J	Operating junction temperature range	Default	0		90	°C
		A version	-40		125	
$F_{SYSCLK1,6}$	DSP Operating Frequency (SYSCLK1,6)	-300 Device	0		300	MHz
		-200 Device	0		200	MHz

(1) These are preliminary pre-silicon design estimates and hence are subject to change.

3.1 Power Use Case Details

- **Use Case 1:** At room temperature (25 °C) with the core voltage (CVDD) set to 1.2V. 70% DSP CPU utilization (300 MHz); EMIFB active at 50% utilization (133 MHz/16-bit); 25 MHz McASP Receive; SPI master at 50% utilization (27MHz); GPIOs at 50 utilization (33MHz). The actual current draw varies across manufacturing processes and is highly application-dependent.

4 Tools and Software Support

The supports the following tools and software:

- Code Composer Studio™ 3.3
- DSP/BIOS™ 5.3
- DSP/BIOS™ 5.3 based Peripheral Device Drivers
- DSP Chip Support Library (CSL)
- TMS320C6747 Development Kit

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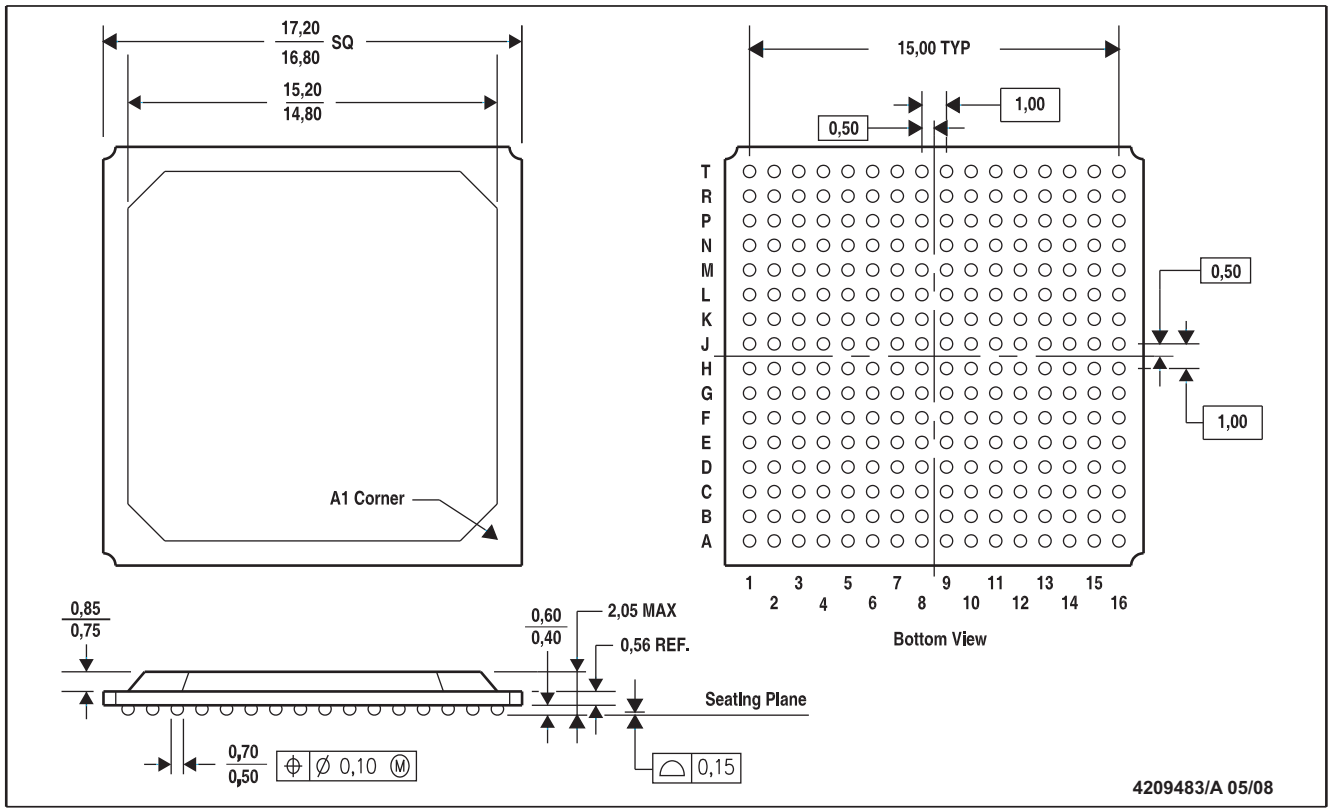
5 Mechanical Drawing

ZKB (S-PBGA-N256) **PLASTIC BALL GRID ARRAY**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This is a lead-free solder ball design.

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