TMS320DM36x DMSoC Analog to Digital Converter (ADC) Interface

User's Guide

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Read This First

About This Manual

This document describes the analog-to-digital converter (ADC) interface peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure designate a bit that is used for future device expansion.

Related Documentation From Texas Instruments

The following documents describe the TMS320DM36x Digital Media System-on-Chip (DMSoC). Copies of these documents are available on the internet at www.ti.com.

SPRUFG5— ***TMS320DM36x Digital Media System-on-Chip (DMSoC) ARM Subsystem Users Guide*** This document describes the ARM Subsystem in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The ARM subsystem is designed to give the ARM926EJ-S (ARM9) master control of the device. In general, the ARM is responsible for configuration and control of the device; including the components of the ARM Subsystem, the peripherals, and the external memories.

SPRUFG8— ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Video Processing Front End (VPFE) Users Guide*** This document describes the Video Processing Front End (VPFE) in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFG9— ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Video Processing Back End (VPBE) Users Guide*** This document describes the Video Processing Back End (VPBE) in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFH0— ***TMS320DM36x Digital Media System-on-Chip (DMSoC) 64-bit Timer Users Guide*** This document describes the operation of the software-programmable 64-bit timers in the TMS320DM36x Digital Media System-on-Chip (DMSoC). Timer 0, Timer 1, and Timer 3 are used as general-purpose (GP) timers and can be programmed in 64-bit mode, dual 32-bit unchained mode, or dual 32-bit chained mode; Timer 2 is used only as a watchdog timer. The GP timer modes can be used to generate periodic interrupts or enhanced direct memory access (EDMA) synchronization events and Real Time Output (RTO) events (Timer 3 only). The watchdog timer mode is used to provide a recovery mechanism for the device in the event of a fault condition, such as a non-exiting code loop.

SPRUFH1— ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Serial Peripheral Interface (SPI) Users Guide*** This document describes the serial peripheral interface (SPI) in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The SPI is a high-speed synchronous serial input/output port that allows a serial bit stream of programmed length (1 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI is normally used for communication between the DMSoC and external peripherals. Typical applications include an interface to external I/O or peripheral expansion via devices such as shift registers, display drivers, SPI EPROMs and analog-to-digital converters.

SPRUFH2— *TMS320DM36x Digital Media System-on-Chip (DMSoC) Universal Asynchronous Receiver/Transmitter (UART) Users Guide* This document describes the universal asynchronous receiver/transmitter (UART) peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The UART peripheral performs serial-to-parallel conversion on data received from a peripheral device, and parallel-to-serial conversion on data received from the CPU.

SPRUFH3— *TMS320DM36x Digital Media System-on-Chip (DMSoC) Inter-Integrated Circuit (I2C) Peripheral Users Guide* This document describes the inter-integrated circuit (I2C) peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The I2C peripheral provides an interface between the DMSoC and other devices compliant with the I2C-bus specification and connected by way of an I2C-bus. External components attached to this 2-wire serial bus can transmit and receive up to 8-bit wide data to and from the DMSoC through the I2C peripheral. This document assumes the reader is familiar with the I2C-bus specification.

SPRUFH4— TMS320DM36x Digital Media System-on-Chip (DMSoC) Memory Stick Controller Users Guide This document This document describes the memory stick controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC). Memory Stick cards are used in a number of applications to provide removable data storage. The memory stick controller provides an interface to external Memory Stick cards. The communication between the controller and the cards is performed by the Memory Stick protocol.

SPRUFH5— *TMS320DM36x Digital Media System-on-Chip (DMSoC) Multimedia Card (MMC)/Secure Digital (SD) Card Controller Users Guide* This document describes the multimedia card (MMC)/secure digital (SD) card controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The MMC/SD card is used in a number of applications to provide removable data storage. The MMC/SD controller provides an interface to external MMC and SD cards. The communication between the MMC/SD controller and MMC/SD card(s) is performed by the MMC/SD protocol.

SPRUFH6— *TMS320DM36x Digital Media System-on-Chip (DMSoC) Pulse-Width Modulator (PWM) Users Guide* This document describes the pulse-width modulator (PWM) peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFH7— *TMS320DM36x Digital Media System-on-Chip (DMSoC) Real-Time Out (RTO) Controller Users Guide* This document describes the Real Time Out (RTO) controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFH8— *TMS320DM36x Digital Media System-on-Chip (DMSoC) General-Purpose Input/Output (GPIO) Users Guide* This document describes the general-purpose input/output (GPIO) peripheral in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The GPIO peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an input, you can detect the state of the input by reading the state of an internal register. When configured as an output, you can write to an internal register to control the state driven on the output pin.

SPRUFH9— *TMS320DM36x Digital Media System-on-Chip (DMSoC) Universal Serial Bus (USB) Controller Users Guide* This document describes the universal serial bus (USB) controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The USB controller supports data throughput rates up to 480 Mbps. It provides a mechanism for data transfer between USB devices and also supports host negotiation.

SPRUFI0— *TMS320DM36x Digital Media System-on-Chip (DMSoC) Enhanced Direct Memory Access (EDMA) Controller Users Guide* This document describes the operation of the enhanced direct memory access (EDMA3) controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The EDMA controller's primary purpose is to service user-programmed data transfers between two memory-mapped slave endpoints on the DMSoC.

SPRUFI1— *TMS320DM36x Digital Media System-on-Chip (DMSoC) Asynchronous External Memory Interface (EMIF) Users Guide* This document describes the asynchronous external memory interface (EMIF) in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The EMIF supports a glueless interface to a variety of external devices.

SPRUFI2— ***TMS320DM36x Digital Media System-on-Chip (DMSoC) DDR2/Mobile DDR (DDR2/mDDR) Memory Controller Users Guide*** This document describes the DDR2/mDDR memory controller in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The DDR2/mDDR memory controller is used to interface with JESD79D-2A standard compliant DDR2 SDRAM and mobile DDR devices.

SPRUFI3— ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Multibuffered Serial Port Interface (McBSP) User's Guide*** This document describes the operation of the multibuffered serial host port interface in the TMS320DM36x Digital Media System-on-Chip (DMSoC). The primary audio modes that are supported by the McBSP are the AC97 and IIS modes. In addition to the primary audio modes, the McBSP supports general serial port receive and transmit operation.

SPRUFI4— ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Universal Host Port Interface (UHPI) User's Guide*** This document describes the operation of the universal host port interface in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

SPRUFI5— ***TMS320DM36x Digital Media System-on-Chip (DMSoC) Ethernet Media Access Controller (EMAC) User's Guide*** This document describes the operation of the ethernet media access controllerface in the TMS320DM36x Digital Media System-on-Chip (DMSoC).

Analog to Digital Converter (ADC) Interface

DM36x has a 6-channel, 10-bit analog-to-digital converter (ADC) interface. The CPU communicates to the ADC interface using 32-bit-wide control registers accessible via the internal peripheral bus.

1 Features

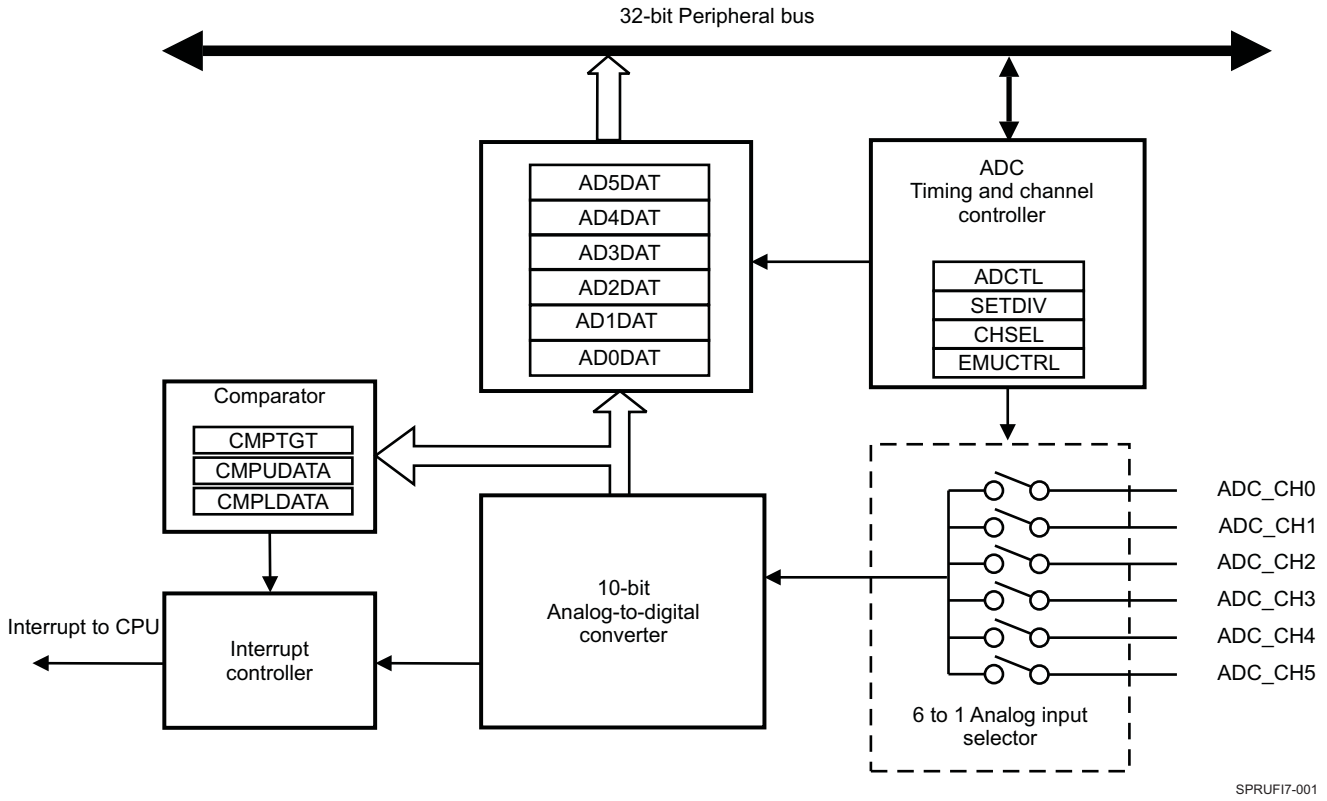
The DM36x ADC interface has following features:

- Supports six configurable analog Input
- Supports for successive approximation type 10-bit, A-D converter
- Programmable sampling / conversion time (base clock is AUXCLK)
- Supports channel select by auto scan conversion
- Supports mode select by one-shot mode or free-run mode
- Programmable setup (Idle) period to secure A/D sampling start time
- Supports the clock stop signals to connect the PSC

1.1 Block Diagram

Figure 1 shows the data path and control path of ADC interface.

Figure 1. ADC IF Block Diagram



1.2 Industry Compliance Statement

The ADC interface does not conform to any recognized industry standards.

2 Peripheral Architecture

2.1 Clock Control

The ADC interface is driven by the auxiliary clock of the PLL controller. The frequency of the auxiliary clock is equal to the input reference clock of the PLL controller, and therefore is not affected by the multiplier and divider values of the PLL controller. For more information on device clocking, refer to the *TMS320DM365 Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide* (SPRUFG5).

2.2 Signal Descriptions

The ADC interface receives analog inputs on six separate pins: ADC_CH [5:0]. Refer to the *TMS320DM365 Digital Media System-on-Chip Data Manual* (SPRS457) for more information on these pins.

2.3 Functional Operation

The ADC interface can operate in either one-shot mode or free-run mode. In both modes, the ADC peripheral has a Comparison A/D Lower data register (CMPLDAT) and a Comparison A/D Upper data register (CMPUDAT) to specify, respectively, the lower and upper data for comparison. The analog input channel to be used for scan conversion can be configured using the CHSEL registers and on the CMPTGT register, set the analog input data to be the target of comparator. For one-shot mode operation, see Section 2.3.1; for Free-Run mode operation, see Section 2.3.2.

2.3.1 One-Shot Mode Operation

In one-shot mode operation, the ADC interface does not run continuously and A/D conversion terminates when scanning is completed.

For one-shot mode operation, the ADC interface should first be configured for scan mode (SCNMD) and comparator mode (CMPMD) in ADC interface control register (ADCTL), along with other configuration options. The ADC interface sets the BUSY bit in ADCTL once it is started by writing a 1 to the START bit in the ADCTL register

Once started, the ADC interface genertaes the output after A/D conversion time. A/D conversion time is obtained by Analog switch setup time + ADC setup time + A/D conversion time.

- Analog switch setup time = Peripheral CLK period * (SET_DIV[5:0] + 3)*2
- ADC setup time = Peripheral CLK period * (SET_DIV[15:0] + 1)*2
- A/D conversion time = Peripheral CLK period* (SET_DIV[5:0] + 1)*24

When the A/D scan conversion is finished for all channels, the peripheral sends an interrupt to the system (if the interrupt is enabled in ADCTL register). The START bit will cleared automatically when A/D conversion in One-Shot mode terminates. The ADC interface then becomes inactive until the START bit is written a 1 again.

The ADC Interface is stopped during one-shot mode operation by changing the START bit to 0 in ADCTL. After START bit turns to '0', it will be stop at the completion of current sample conversion. If user change configuration, then user need to wait at least a time which defined by SETDIV register after writing '0' into START bit.

2.3.2 Free-Run Mode Operation

In free-run mode operation, the ADC interface performs A/D conversion continuously without stopping.

For free-run mode operation, the ADC interface should first be configured for scan mode(SCNMD), and comparator mode (CMPMD) in ADC interface control register (ADCTL), along with other configuration options. The ADC interface sets the BUSY bit in ADCTL once it is started by writing a 1 to the START bit in the ADCTL register.

Once started, the ADC interface genertaes the output after A/D conversion time. A/D conversion time is obtained by Analog switch setup time + ADC setup time + A/D conversion time.

- Analog switch setup time = Peripheral CLK period * (SET_DIV[5:0] + 3)*2
- ADC setup time = Peripheral CLK period * (SET_DIV[15:0] + 1)*2
- A/D conversion time = Peripheral CLK period* (SET_DIV[5:0] + 1)*24

When the A/D scan conversion is finished for all channels, the peripheral sends an interrupt to the system (if the interrupt is enabled in ADCTL register). Note that unlike normal one-shot mode operation, another write to the START bit is not required for the one-shot mode operation to start.Once A/D conversion of all the channels is finished A/D conversion re-start from CH0.

The ADC interface is stopped during the free-run mode operation by writing '0' into START bit. After START bit turns to '0', it will be stop at the completion of current sample conversion. If user change configuration, then user need to wait at least a time which defined by SETDIV register after writing '0' into START bit. The ADC interface can also stopped during the free-run mode operatioor by reconfiguring it to one-shot mode using the SCNMD bit in ADCTL register.

2.4 Reset Considerations

2.4.1 Software Reset Considerations

A software reset (such as a reset generated by the emulator) causes the ADC interface registers to return to their default state after reset.

2.4.2 Hardware Reset Considerations

A hardware reset of the processor causes the ADC interface registers to return to their default values after reset.

2.5 Interrupt Support

2.5.1 Interrupt Events and Requests

The ADC interface generates a single pulse interrupt. This interrupt is tied directly to the AINTC. ADC interface generates Scan Interrupt to CPU when A/D scan conversion is finished for all channels once.

The cause of comparator interrupt is selected according to the CMPMD bit in ADCTL register. A single common comparative data window has provided for every individual channel. Depending on the Comparator mode selected an interrupt occurs after the A/D conversion in each channel for either of the following condition.

- Conversion data is out of the range of the comparative data window
- Conversion data is within the range of the comparative data window

2.5.2 Interrupt Multiplexing

The ADC interface is supported by the ARM Interrupt Controller (AINTC) module. The ARM_INTMUX register in the system control module must be used to select the interrupt source for multiplexed interrupts. In particular, the ADC interface interrupt is multiplexed with other interrupts. Refer to the *TMS320DM365 Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide* (SPRUFG5) for more information on the System Control Module and ARM Interrupt Controller.

2.6 EDMA Event Support

The ADC interface module does not generate an EDMA event.

2.7 Power Management

The ADC interface can be placed in reduced-power modes to conserve power during periods of low activity. Power management of the ADC Interface is controlled by the power and sleep controller (PSC) processor. The PSC acts as a master controller for power management for all of the peripherals on the device. For detailed information on power management procedures using the PSC, see the *TMS320DM365 Digital Media System-on-Chip (DMSoC) ARM Subsystem Reference Guide* (SPRUFG5)

2.8 Emulation Considerations

ADC interface supports the emulation suspend function. At the enable emulator suspend, this module keep the following condition and restart.

- Stop after a A-D convert
- Bus access is available under the suspend time
- Restart with the setting condition after the suspend time

3 Registers

Table 1 lists the memory-mapped registers for the analog-to-digital Controller (ADC) interface. See the device-specific data manual for the memory address of these registers

Table 1. ADC interface Memory Map Registers

Offset	Register	Description	Location
0x0	ADCTL	Control register	Section 3.1
0x4	CMPTGT	Comparator target channel	Section 3.2
0x8	CMPLDAT	Comparison A/D Lower data	Section 3.3
0xC	CMPUDAT	Comparison A/D Upper data	Section 3.4
0x10	SETDIV	SETUP divide value for start A/D conversion	Section 3.5
0x14	CHSEL	Analog Input channel select	Section 3.6
0x18	AD0DAT	A/D conversion data 0	Section 3.7
0x1C	AD1DAT	A/D conversion data 1	Section 3.8
0x20	AD2DAT	A/D conversion data 2	Section 3.9
0x24	AD3DAT	A/D conversion data 3	Section 3.10
0x28	AD4DAT	A/D conversion data 4	Section 3.11
0x2C	AD5DAT	A/D conversion data 5	Section 3.12
0x30	EMUCTRL	Emulation Control	Section 3.13

3.1 ADCTL

The ADC control register (ADCTL) is shown in Figure 2 and described in Table 2.

Figure 2. ADC Control (ADCTL) Register

31	30	29	28	27	26	25	24
Reserved							
R-0							

23	22	21	20	19	18	17	16
Reserved							
R-0							

15	14	13	12	11	10	9	8
Reserved							
R-0							

7	6	5	4	3	2	1	0
BUSY	CMPFLG	CMPIEN	CMPMD	SCNFLG	SCNIEN	SCNMD	START
R-0	R/C-0	R/W-0	R/W-0	R/C-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 2. ADC Control (ADCTL) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved		Any writes to these bit(s) must always have a value of 0.
7	BUSY		Busy flag
6	CMPFLG		Comparator interrupt flag clear bit. Writing ‘1’ into this bit clears the comparator interrupt flag and then it will be cleared automatically. At read time, comparator interrupt status can be read.
		0	No interrupt
		1	Interrupt
5	CMPIEN		Comparator interrupt enable bit
		0	Disable
		1	Enable
4	CMPMD		Comparator mode select bit
		0	If the value of A/D input data is larger or smaller than the comparative data, a comparator interrupt is generated. ADC input data < CMPLDAT or ADC input data > CMPUDAT
		1	If the value of A/D input data is within the range of the comparative data, a comparator interrupt is generated. CMPLDAT ≤ ADC input data ≤ CMPUDAT
3	SCNFLG		Scan interrupt flag clear bit. Writing '1' into this bit clears the scan interrupt flag then it will be cleared automatically. At read time, scan interrupt status can be read.
		0	No interrupt
		1	Interrupt
2	SCNIEN		Scan interrupt enable bit
		0	Disable
		1	Enable
1	SCNMD		Scan mode selection
		0	One shot
		1	Free run
0	START		A/D conversion start bit The status is cleared automatically when A/D conversion in One-Shot mode terminates. Writing '0' into this bit in Free-Run mode terminates A/D conversion.'0' can be read at the time of read-access if no analog channel is selected on the CHSEL register. ('1' can be read only at the time of A/D conversion.)

3.2 CMPTGT

The comparator target channel (CMPTGT) register is shown in Figure 3 and described in Table 3.

Figure 3. Comparator Target Channel (CMPTGT) Register

31	6	5	0
Reserved		CMPTGT	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 3. Comparator Target Channel (CMPTGT) Field Descriptions

Bit	Field	Value	Description
31-6	Reserved	1 0	Any writes to these bit(s) must always have a value of 0.
5-0	CMPTGT		Comparator target channel at A/D conversion The analog input that has written '1' into CMPTGT is the target of the comparator.

3.3 CMPLDAT

The comparison A/D lower data (CMPLDAT) register is shown in Figure 4 and described in Table 4.

Figure 4. Comparison A/D Lower Data (CMPLDAT) Register

31	10	9	0
Reserved		CMPLDAT	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 4. Comparison A/D Lower Data (CMPLDAT) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Any writes to these bit(s) must always have a value of 0.
9-0	CMPLDAT		Comparative data (lower) value of CMPLDAT should be the same as or smaller than that of CMPUDAT.

3.4 CMPUDAT

The comparison A/D Upper data (CMPUDAT) register is shown in Figure 5 and described in Table 5.

Figure 5. Comparison A/D Upper Data (CMPUDAT) Register

31	10	9	0
Reserved		CMPUDAT	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 5. Comparison A/D Upper Data (CMPUDAT) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved	0	Any writes to these bit(s) must always have a value of 0.
9-0	CMPUDAT		Comparativer data (upper) value of CMPUDAT should be the same as or larger than that of CMPLDAT.

3.5 SETDIV

The SETUP divide value for start A/D conversion (SETDIV) register is shown in Figure 6 and described in Table 6.

A/D conversion time is obtained by Analog switch setup time + ADC setup time + A/D conversion time.
Analog switch setup time = Peripheral CLK period * (SET_DIV[5:0] + 3)*2
ADC setup time = Peripheral CLK period * (SET_DIV[15:0] + 1)*2
A/D conversion time = Peripheral CLK period* (SET_DIV[5:0] + 1)*24.

Note: A/D conversion time can't be less than 6us.

Figure 6. Setup Divide Value for Start A/D (SETDIV) Register

31	16
Reserved	
R-0	

15	0
SETDIV	
R/W-0xFFFF	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 6. Setup Divide Value for Start A/D (SETDIV) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Any writes to these bit(s) must always have a value of 0.
15-0	SETDIV		SETDIV bits set the Analog switch setup time, ADC setup (Idle) time and A/D conversion time. Analog switch setup time = Peripheral CLK period * (SET_DIV[5:0] + 3)*2 ADC setup time = Peripheral CLK period * (SET_DIV[15:0] + 1)*2 A/D conversion time = Peripheral CLK period* (SET_DIV[5:0] + 1)*24.

3.6 CHSEL

The analog Input channel select (CHSEL) register is shown in Figure 7 and described in Table 8. CHSEL setting for the selection of different channel is shown in Table 7. In order to select two or more channels, ORing of these setting is needed.

Table 7. CHSEL setting for Channel selection

CHSEL	Selected Channel
000001b	Channel 0
000010b	Channel 1
000100b	Channel 2
001000b	Channel 3
010000b	Channel 4
100000b	Channel 5

Figure 7. Analog Input Channel Select (CHSEL) Register

31	6	5	0
Reserved		CHSEL	
R-0		R/W-0x3F	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 8. Analog Input Channel Select (CHSEL) Field Descriptions

Bit	Field	Value	Description
31-6	Reserved	0	Any writes to these bit(s) must always have a value of 0.
5-0	CHSEL		A/D conversion select bit
		0	Analog Input unselected
		1	Analog Input selected

3.7 AD0DAT

The A/D conversion data 0 (AD0DAT) register is shown in Figure 8 and descried in Table 9.

Figure 8. A/D Conversion Data 0 (AD0DAT) Register

31	10	9	0
Reserved		AD0DAT	
R-0		R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 9. A/D Conversion Data 0 (AD0DAT) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved		Any writes to these bit(s) must always have a value of 0.
9-0	AD0DAT		A/D conversion data for channel 0

3.8 AD1DAT

The A/D conversion data 1 (AD1DAT) register is shown in Figure 9 and described in Table 10.

Figure 9. A/D Conversion Data 1 (AD1DAT) Register

31	10	9	0
Reserved		AD1DAT	
R-0		R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 10. A/D Conversion Data 1 (AD1DAT) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved		Any writes to these bit(s) must always have a value of 0.
9-0	AD1DAT		A/D conversion data for channel 1

3.9 AD2DAT

The A/D conversion data 2 (AD2DAT) register is shown in Figure 10 and described in Table 11.

Figure 10. A/D Conversion Data 2 (AD2DAT) Register

31	10	9	0
Reserved		AD2DAT	
R-0		R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 11. A/D Conversion Data 2 (AD2DAT) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved		Any writes to these bit(s) must always have a value of 0.
9-0	AD2DAT		A/D conversion data for channel 2

3.10 AD3DAT

The A/D conversion data 3 (AD3DAT) register is shown in Figure 11 and described in Table 12.

Figure 11. A/D Conversion Data 3 (AD3DAT) Register

31	10	9	0
Reserved		AD3DAT	
R-0		R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 12. A/D Conversion Data 3 (AD3DAT) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved		Any writes to these bit(s) must always have a value of 0.
9-0	AD3DAT		A/D conversion data for channel 3

3.11 AD4DAT

The A/D conversion data 4 (AD4DAT) register is shown in Figure 12 and described in Table 13.

Figure 12. A/D Conversion Data 4 (AD4DAT) Register

31	10	9	0
Reserved		AD4DAT	
R-0		R-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 13. A/D Conversion Data 4 (AD4DAT) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved		Any writes to these bit(s) must always have a value of 0.
9-0	AD4DAT		A/D conversion data for channel 4

3.12 AD5DAT

The A/D conversion data 5 (AD5DAT) register is shown in and described in .

Figure 13. A/D Conversion Data 5 (AD5DAT) Register

31	10	9	0
Reserved		AD5DAT	
R-0		R-0	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 14. A/D Conversion Data 5 (AD5DAT) Field Descriptions

Bit	Field	Value	Description
31-10	Reserved		Any writes to these bit(s) must always have a value of 0.
9-0	AD5DAT		A/D conversion data for channel 5

3.13 EMUCTRL

The emulation control (EMUCTRL) register is shown in Figure 14 and described in Table 15.

Figure 14. Emulation Control (EMUCTRL) Register

31	16
Reserved	
R-0	

15	3	2	1	0
Reserved		RT_SEL	SOFT	FREE
R-0		R-0	R-1	R/W-1

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 15. Emulation Control (EMUCTRL) Field Descriptions

Bit	Field	Value	Description
31-2	Reserved		Any writes to these bit(s) must always have a value of 0.
2	RT_SEL	0	Support only emulation suspend
1	SOFT		Support only soft stop
		1	Soft stop: Stop peripheral operations gracefully at the earliest opportunity after the current application specific processing task is completed.
0	FREE		This bit controls whether or not the peripheral will respond to the emulation suspend signal that it has been programmed to monitor
		0	Peripheral suspends according to mode specified by the SOFT bit
		1	Peripheral ignores suspend and operates normally

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